Suthinan Limthong 2007: Design of n Bit Adder Cell for Low Power Application. Master of Engineering (Electrical Engineering), Major Field: Electrical Engineering, Department of Electrical Engineering. Thesis Advisor: Assistant Professor Chugiat Garagate, Ph.D. 111 pages.

This paper presents the design of low-power n-bit adder cell in 3 different adder topologies. The adder circuits include Ripple Carry Adder, Carry Lookahead Adder and Carry Select Adder. Experimental Pass-transistor is employed in the design. The designed circuits are compared to Static Complementary CMOS circuits, which are logic gates normally used in MOS integrated circuit. The result shows that there are no significant difference in functionality has performance of both systems under the 5-volt power supply. However, it was found that some circuit of Pass- transistor design circuit can reduced the maximum power usage by 80 % and some circuit of Pass- transistor design circuit can reduced the minimum power usage by 54 % lower than Static CMOS.

In addition, this paper also demonstrate the power supply reduction technique. The minimum power supply required for the circuit to operate correctly is 3.3 V. It was also found that the some circuit of Pass- transistor design circuit can reduced the maximum power usage by 72 % and some circuit of Pass- transistor-design circuit can reduced the minimum power usage by 33 % when the power supply is changed from 5 to 3.3 V. Further more, the delay time and noise margin which are the factors in the circuit performance investigated. It was found that both delay time and noise margin are in acceptable range for applications.

In conclusion, n-bit adder cell can be designed for low power application by the combination of Pass-transistor design and power supply reduction technique. The power consumption can be reduced up to 80 % depended on the types and topologies. Noise margin and delay time are still in an acceptable range.

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