JESDA LOHAVIVATTANAKUL : MULTI-BIT CONSTRAINED SECOND-ORDER POWER CONTROL AND
QUADRATIC EQUATION LINK GAIN PREDICTION IN CDMA CELLULAR MOBILE COMMUNICATION
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This thesis proposes two uplink power control schemes in DS-CDMA cellular mobile radio systems. The proposed power control schemes are the modified versions of Constrained Second-Order Power Control (CSOPC), which is a scheme to control the mobile station power to converge to the desired power, combining with link gain prediction using Quadratic Equation (Proposed Scheme 1) and Recursive Least Square (RLS) criterion (Proposed Scheme 2). The calculation for power control is done at the base station and then the power control command (cmd) (multi-bit power control) is sent to the mobile station. The performance of the proposed schemes is compared to those of CSOPC with no link gain prediction and SIR-based Pulse-Code-Modulation (PCM) Power Control which is a multi-bit power control scheme, the same as the proposed schemes.

The simulation results show that the proposed schemes give lower outage probability than PCMPC and CSOPC in all cases of the desired SIR (-12, -11.5, ..., -8 dB) , all cases of the number of mobile stations (8 to 13 stations) and all cases of the number of desired power control bits (2 to 8 bits). However, the proposed schemes give higher outage probability than PCMPC when the number of power control bits is 1. The proposed scheme 2 gives the lowest outage probability in all cases of the desired SIR (-12, -11.5, ..., -8 dB) , all cases of the number of mobile stations (8 to 13 stations) and all cases of the desired power control bits (2 to 8 bits) when compared to PCMPC, CSOPC and the Proposed Scheme 1, but gives higher outage probability (1.60×10^{-1}) than PCMPC (3.06×10^{-2}) when the number of power control bits is 1. The Proposed Schemes 1 and 2 reduce outage probability compared to PCMPC for 63.85 and 82.21 % respectively. Large reduction in outage probability obtained from the Proposed Schemes 1 and 2 are tradeoff with an increase in their calculation time. Application of the Proposed Schemes 1 and 2 in practical system are possible by using new high-speed processor and parallel processing architecture.