วิศวกรรมสาร มข. ปีที่ 38 ฉบับที่ (211 -218) เมษายน - มิถุนายน 2554 บทความวิชาการ
KKU Engineering Journal Vol.38 No.2 (211 -218) April - June 2011

On-Chip Transformer: Overview, Apllications and Modeling

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Abstract

According to the chronological literature survey, there exist three types of the on-chip transformer i.e the traditional on-chip passive transformer, the Distributed active transformer (DAT), and the CMOS gyrator-C active transformer (Yuan 2007). Formerly, there exist many review articles on the on-chip transformer. However, these articles focus on the on-chip passive transformer due to its renowns where as DAT and CMOS gyrator-C are overlooked.

Hence, the review on the on-chip transformer with the formerly overlooked DAT and CMOS gyrator-C active transformer also focused has been proposed in this study. The overviews, applications and modelings of all three types of the on-chip transformer have been discussed. Furthermore, an interresting open research issue is also suggested.

Keywords: On-chip transformer, On-chip passive transformer, DAT, CMOS gyrator-C active transformer

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1. Introduction

On-chip transformer is an important building block in various applications for example, amplifier, mixer and filters. Traditionally, it can be constructed by using only the passive elements i.e. the metal conductors on the silicon substrate. This traditional on-chip transformer can be regarded as on-chip passive transformer. On the other hand, there exist the Distributed active transformer (DAT), which contains both passive and active elements i.e. metal conductors and transistors. Finally, the active element based on-chip transformer has been recently proposed in (Yuan, 2007). This active on-chip transformer is entitled the CMOS gyrator-C active transformer because it contains only MOS transistors without any intrinsic passive element.

Formerly, there exist many review articles on the on-chip transformer for example (Long, 2000). However, these articles focus on the traditional on-chip passive transformer due to its renowns where as those issues on DAT and CMOS gyrator-C active transformer are overlooked even though they are also remarkable.

In this paper, the review on the on-chip transformer has been proposed with the formerly overlooked issues which are DAT and CMOS gyrator-C active transformer also considered together with the often cited traditional on-chip passive transformer. The overviews, applications and modelings of the tradional on-chip passive transformer, DAT and the recently proposed CMOS gyrator-C active transformer, have been discussed. Furthermore, an interresting open research issue is also suggested at the end of this paper.

2. On-Chip Passive Transformer

On-chip passive transformer can be constructed by the magnetic coupling of the spirally wounded metal conductors which can be laid out on the silicon substrate. Obviously, the on-chip passive transformer is a purely passive element without any intrinsic active component. The coupling coefficient, k_m which defines the strength of the magnetic coupling between the windings can be defined accoring to (Rapulo 2008) as

$$k_m^2 = \frac{M^2}{L_p L_s} \quad (1)$$

where M, L_p and L_s denote the mutual, primary and secondary self inductances respectively. For the on-chip passive transformer, $0 \leq k_m \leq 1$ since the magnetic flux linkage is low.

According to the layout of the windings, the on-chip passive transformer can be widely classified in to two folds entitled staked transformer and interleaved transformer (Rapulo, 2008) which will be discussed in the following subsections

2.1 Stacked transformer

For the stacked transformer, both primary and secondary windings are stacked over each other as can be seen in the following figure (Rapulo, 2008)

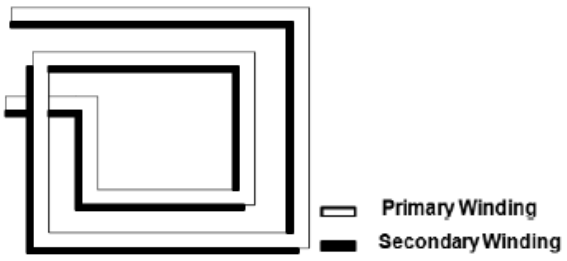

Figure 1 *Stacked Transformer (Rapulo, 2008)*

Since one of the windings is closer to the substrate, the stacked transformer is considered to be asymmetric. Furthermore, the mutual inductance and the occupied area are relatively large compared to that of the interleaved transformer.

2.2 Interleaved transformer

For the interleaved transformer, both windings are laid out on the same plane as depicted below

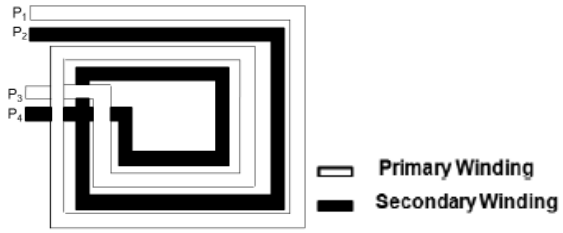

Figure 2 *Interleaved Transformer (Rapulo 2008)*

As both windings are laid out symmetrically on the same plane, the interleaved transformer is considered to be symmetric. The mutual inductance is lower than that of the stacked transformer due to smaller flux linkage between both windings.

Practically, various nonidealities for example, finite conductivity of the windings, finite resistivity of the subsrate, eddy currents in the windings and substrate and lateral electric field between windings, exist. It should be mentioned here that the interwinding capacitances caused by the lateral electric field between windings of the interleaved transformer are smaller than those of the stacked transformer.

Due to the existence of these nonidealities, the behaviors of the on-chip passive transformer deviate from those of the ideal transformer. Hence, the model which simulates these deviated behaviors is necessary for convenience in the design and analysis of various on-chip passive transformer based applications for example, low voltage VCOs (Kwok, Luong, 2005), low power/low noise mixers (Long, Copeland, 1995), low power LNA (Zhou, Allstot, 1998), high Q BP filter (Kulyk, Haslett, 2006) and integrated baluns (Kaczman et.al, 2006). The cited model can be derived as the equivalent circuit model which can be either lumped or distributed (Rapulo, 2008). An example of the lumped equivalent circuit model has been proposed in (El-Gharniti et.al, 2006) and can be depicted below

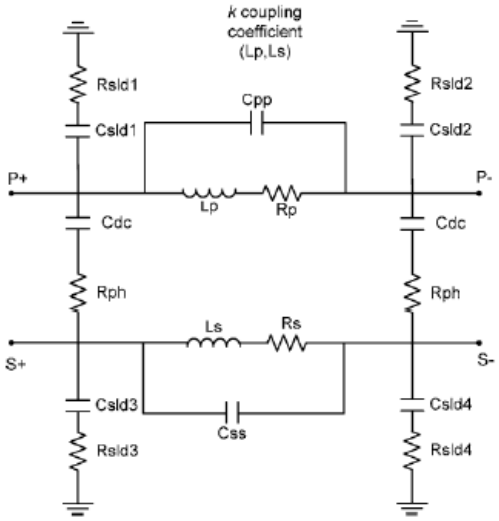

Figure 3 *On-chip passive transformer's lumped equivalent circuit model proposed in (El-Gharniti et.al., 2006)*

The analytical expressions of the circuit elements within this model which shown in (El-Gharniti et.al., 2006), are derived based on the geometry of the transformer along with the physical properties of the windings and substrate. Hence, this model is derived with the analytical/empirical modeling (Rapulo, 2008).

On the other hand, an example of the distributed equivalent circuit model has been proposed in (Klemen et.al, 2004) and can be depicted in Fig.4. The analytical expressions of the circuit elements within this model which shown in (Klemen et.al, 2004), are derived based on the S-parameters of the on-chip passive transformer which is one of the behavior of the transformer it self. Hence, this model is derived with the behavioral modeling (Rapulo, 2008). This model contains a large number of mutual inductances which may corrupt the passivity of the model.

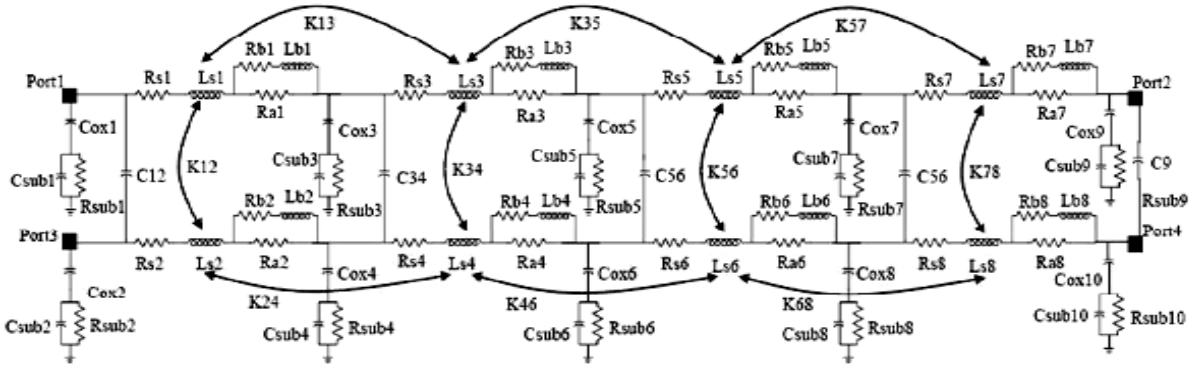

Figure 4 *On-chip passive transformer's distributed equivalent circuit model proposed in (Klemen et.al, 2004)*

One remarkable application of the on-chip passive transformer is the bandwidth enhancement of the CMOS amplifier based upon the inductive peaking techniques (Allstot et.al, 2006). A conventional approach is the bridge T-coil peaking which requires a symetric transformer for example, interleaved transformer. An improved approach is the asymetric T-coil peaking which gives higher BW extension ratio than the conventional approach by utilizing an asymetric transformer for example, stackted transformer. This approach has been used in the extended BW differrential amplifier proposed in (Klemen et.al, 2004). The bridge T-coil (BTC) peaked and asymetric T-coil (ATC) peaked CMOS amplifiers can be depicted in Fig. 5 and 6 respectively (Allstot et.al, 2006).

Apart from stacked and interleaved transformers, various improved on-chip passive transformer with differrent layout schemes have been proposed for example, centertapped interleaved transformer, laterally shifted stacked transformer, diagonally shifted stacked transformer and stacked interleaved transformer (Pan et.al, 2004) which various trade-offs are attemped among them.

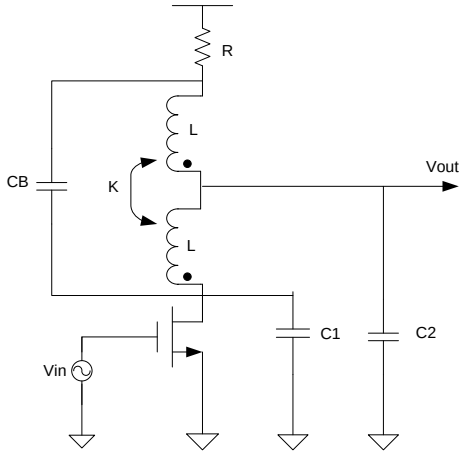

Figure 5 *BTC-peaked CMOS amplifier* (*Allstot et.al, 2006)*

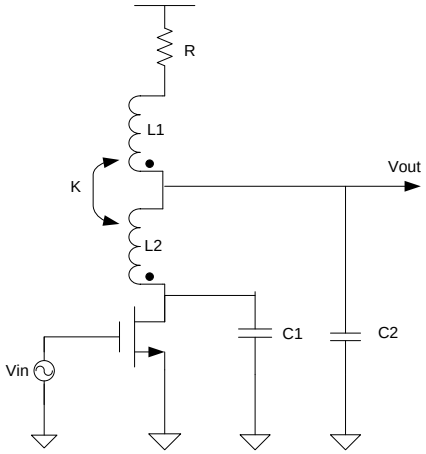

Figure 6 *ATC-peaked CMOS amplifier* (Allstot et.al, 2006)

3. Distributed Active Transformer (DAT)

DAT is originally proposed in (Aoki et.al, 2002) Major applications of DAT are the impedance transformation and power combining which are significant issues in the power amplifier design. The

foundation concept of DAT is the combination of many 1:1 transformers by connecting their secondary terminals in series in order to efficiently perform the impedance transformation. By using the circular shape based combination, both impedance transformation and power combining can be achieved simultaneously. In order to achieve the cited circular shape based combination, many on-chip slab inductor based CMOS push-pull power amplifiers connected in the circular geometry are used for the independent primary windings where as a single turn spiral inductor is used as an output which is equivalent to the series connection of the secondary windings. The gates of the transistors within each push-pull power amplifier are connected by a curl inductive metal. Furthermore, the cross connected drain capacitors are also included.

By using four push-pull power amplifiers which obviously contain eight transistors, DAT can be realized as proposed in (Aoki et.al, 2002) and can be depicted as follows

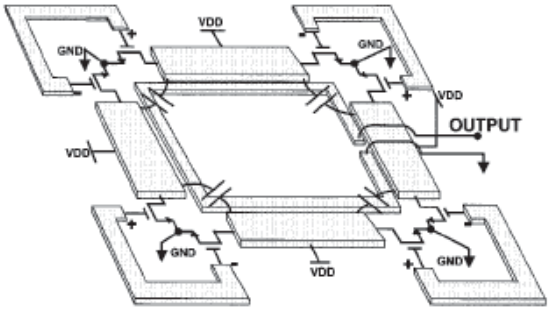

Figure 7 *DAT with 4 CMOS push-pull power amplifiers (Aoki et.al, 2002)*

Generally, If n transistors (n/2 push-pull amplifiers) are used then simultaneous 1:n impedance transformation and n transistors power combining can be obtained. A remarkable feature of DAT is that both passive and active components i.e. inductive metals and transistors respectively are utilized.

An example of the improved DATs has been proposed in (Kim et.al, 2005). This improved DAT which implemented on the GaAs substrate gives significant reduction in both loss and coupling from the DAT to the feed line due to the reduced metal resistance and tighter coupling between the primary and secondary windings. Furthermore, the occupied area of this improved DAT is not larger than that of the conventional one. The top view of this improved DAT can be depicted as follows

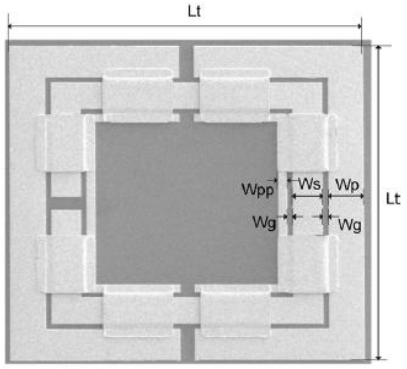

Figure 8 *Top view of the improved DAT proposed in (Kim et.al, 2005)*

For the modeling of DAT, it has been proposed in (Kim et.al, 2005) that the standard transformer model is adequate for the modeling of DAT since DAT is equivalent to a single-turn coupled-inductor transformer. On the other hand, an equivalent circuit model for a quarter of the DAT which serves as the basis of the simulation has been proposed in (Jeon, Rutledge, 2005). This model is depicted as follows.

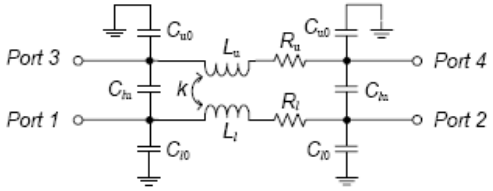

Figure 9 *Equivalent circuit model for a quarter of the DAT proposed in (Jeon, Rutledge, 2005)*

The parameter extraction of this model has been performed based on the measured 4-port S-parameters of the DAT. So, it can be seen that this model is derived by the behavioral modeling. Unlike the on-chip passive transformer, DAT has not been applied to various applications but the impedance transformation and the power combining.

4. CMOS Gyrator-C Active Transformer

An on-chip active transformer without any inductive metal, has been proposed in (Yuan, 2007). This on-chip active transformer was constructed by using the active coupling of the gyrator-C based active inductors via the transconductors. There are two topologies for the gyrator-C active transformer entitled topology 1 and topology 2 which the active coupling transconductor currents flow oppositely. Their conceptual circuit diagrams can be depicted as follows (Yuan, 2007).

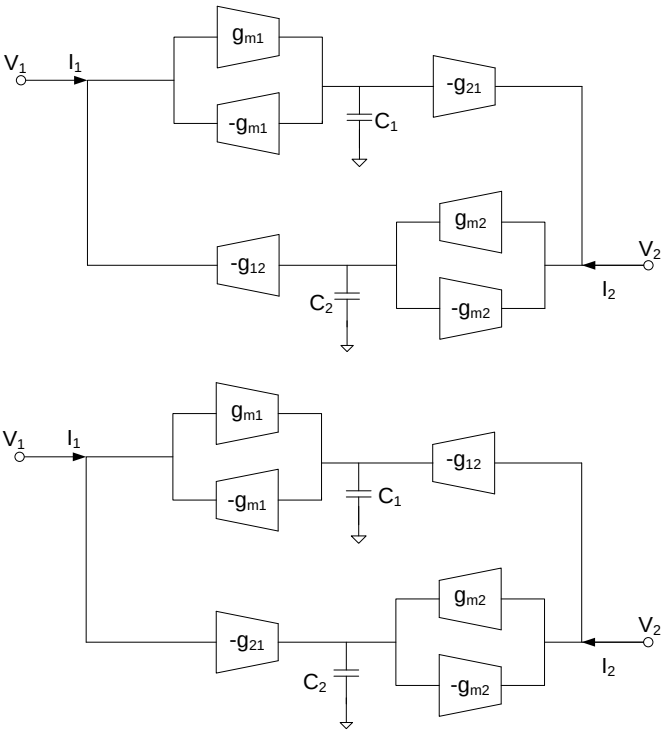

Figure10 *Conceptual circuit diagrams of topology 1 (above) and topology 2 (below) gyrator-C active transformer (Yuan, 2007)*

According to ((Tang et.al, 2009)-(Tang et.al, 2008)), each transconductor within the active transformer has been simply realized by a MOS transistor. So, the resulting active transformer can be entitled CMOS gyrator-C active transformer. Here, the realizations of both topologies of the CMOS gyrator-C active transformers which proposed in (Yuan, 2007) are now depicted in fig 11. According to (Tang, et.al 2009), the CMOS gyrator-C active transformer has many far superior characteristics to the conventional on-chip passive transformer for example, electronically tunable coupling ratio and voltage transfer ratio, larger/electronically tunable self/mutual inductances, higher/electronically tunable quality factors and a smaller chip area.

As an example of these electronically tuning capabilities, the coupling factors of the topology 1 CMOS gyrator-C active transformer is given according to (Yuan, 2007) by

$$k_{21}^2 = \left(\frac{g_{21}}{g_{m1}}\right)^2 \frac{C_1}{C_2} \tag{2}$$

$$k_{12}^2 = \left(\frac{g_{12}}{g_{m2}}\right)^2 \frac{C_2}{C_1} \tag{3}$$

It should be mentioned here that g_{m1} and g_{m2} denote the transconductances of the winding transistors (M1-M4) where as g_{12} and g_{21} denote the transconductances of the coupling ones (M5 and M6). Obviously, both k_{12} and k_{21} can be electronically tuned via g_{m1}, g_{m2}, g_{12} and g_{21} which are functions of the bias currents supply to M1-M6. Other parameters for example, self and mutual inductances can also be electronically tuned in the similar fashion.

Since the CMOS gyrator-C active transformer can be employed in various applications such as quadrature oscillators (Tang, et.al 2009), VCO

(Tang, et.al 2007), current-mode phase-lock loops (Diclemente, et.al 2008)and QPSK modulators (Tang, et.al 2008), it has been found to be a powerful up coming rival of the on-chip passive transformer.

For the modeling, the effects of both major nonidealities of the CMOS gyrator-C active transformer which are unwanted parasitic elements and finite transition frequency of the basis MOS transistor must be captured. Unlike, the on-chip passive transformer, only a few model of the CMOS gyrator-C active transformer have been proposed in (Yuan, 2007) and (Tang, et.al 2007). As an example, the model proposed in (Tang, et.al 2007) can be depicted in Fig. 12. Unfortunately, these models take only parasitic elements into account and overlook the finite transition frequency. So, these models are incomplete and a complete model which takes both major nonidealities into account is strongly demaned.

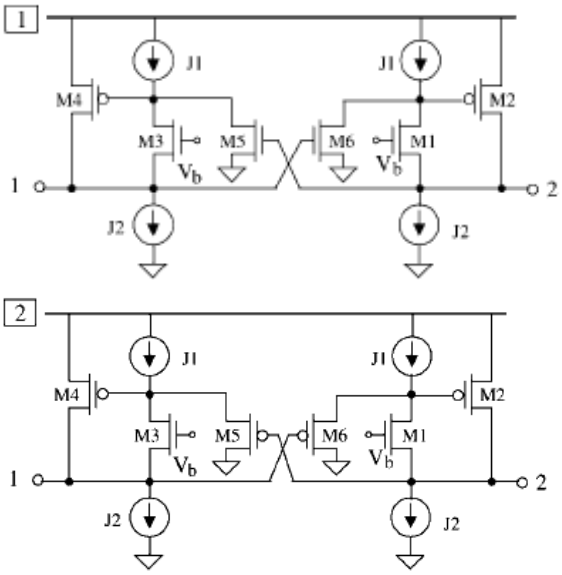

Figure11 *Realization of CMOS-gyrator-C active transformer: Topology 1 (above) and Topology 2 (below) (Yuan, 2007)*

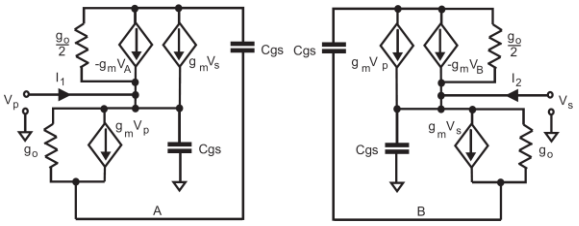

Figure12 *CMOS gyrator-C active transformer model proposed in (Tang, et.al 2007)*

5 Conclusion

In this paper, the overviews, applications and modelings of the tradional on-chip passive transformer, DAT and the recently proposed CMOS gyrator-C active transformer, have been discussed. Similarly to the on-chip passive transformer, there exist various applications of the CMOS gyrator-C active transformer while those of DAT are almost limitted to the impedance transformation and power combining. Unlike the on-chip passive transformer which many efficient models have been proposed, there exist only a few incomplete models of the CMOS gyrator-C active transformer even though it is very applicative. Hence, the complete modeling of the CMOS gyrator-C active transformer has been suggested as an interresting open research issue.

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