

CHAPTER 5

Conclusions

In this thesis, the simple integrable analog integrated circuit building blocks: a Simple Integrable CMOS True RMS-to-DC Converter and an electronically and linearly tunable CMOS OTA (EOTA) were designed. These design techniques are suitable for integrated in CMOS technology. The performances of the proposed circuits are verified through the PSPICE simulation and the experimentation.

5.1 Main achievements and contribution

A simple integrable CMOS true RMS-to-DC converter is presented in chapter 3. The implicit computation method was used in order to design the simple CMOS True RMS-to-DC Converter. This method can achieve great accuracy, wide bandwidth, high input swing, and low cost. The circuit can be operated from a single supply. The device draws less than 0.1mW for the supply voltage of 5 volts. The circuit has been developed based on the characteristic of a CMOS squaring circuit, where all the transistors are biased in the saturation region. This proposed true RMS-to-DC converter accept complex input waveforms containing AC and DC component. The characteristics of the proposed RMS-to-DC converter are studied through the use of discrete CMOS complementary pairs CD4007 that implemented on bread-board. The transient response, DC transfer characteristic and the error versus crest factor are experimentally tested. The high frequency response capability was not measured directly since the stray capacitances in the bread boarding circuit. Therefore, PSPICE simulation result is used to study the high frequency performance. The high frequency limitation of the proposed true RMS-to-DC converter is 100MHz for $I_{in} = 1.5\text{mA}$. This result demonstrate that the frequency is limited by the finite bandwidth of the circuit structure which in this circuit is limited by the current mirror CM₅ [Appendix B].

In addition, to confirm that this proposed circuit is suitable for implementing in monolithic integrated form, the circuit is also layouted and fabricated based on 0.5 microns CMOS technology AMIS process. The chip performances are tested by the measurement setup. There chip performances are agree with the simulation results and the performances of the circuit

that implemented by CMOS complementary CD4007. The simulation and experimental results also agree with the theoretical prediction.

In chapter 4, an Electronically and Linearly Tunable CMOS OTA (EOTA) is presented. This circuit composes of three balanced CMOS OTAs. The realization technique is achieved by squaring the transconductance gain of the balanced CMOS OTA. This circuit is suitable for implementing in CMOS integrated form. The achieved characteristics of the transconductance gain (g_m) is dependent upon the bias current I_b over the range of $1\mu\text{A}$ to 1mA (three decades) with the conversion error from simulation result is about 0.68%. The EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of -1V to 1V . The frequency response of the EOTA was also studied, where the -3dB bandwidth of about 120MHz is achieved. However the circuit can be operated in a wider bandwidth by increasing the dc bias currents of the circuit.

The current-mode multiplier circuit, and both of current-controlled and voltage controlled current amplifier were used to display the performances and the advantage of the proposed EOTA. The current-mode multiplier circuit using the proposed EOTA can be function as a four-quadrant current multiplier which use only active circuit elements but not require external passive circuit elements. The simulation results can confirm that the circuit can accurately modulate two different input signal currents. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of $\pm 190\mu\text{A}$ with the error of less than 1%. The high frequency characteristic of the multiplier circuit is also studied. The simulated -3dB bandwidth of the current multiplier is about 71MHz . For the voltage-controlled current amplifier that designed based on the proposed EOTA, its current gain can be electronically and linearly tune by the control voltage V_c . The current gain can be tuned for the range of 0.1 to 1 times. In the case of the current-controlled current amplifier its current gain can be electronically and linearly tune for the range of 0.1 -20 times by the DC bias current.

In summary, the goal of this work is to design the new analog integrated circuit building blocks: A true RMS-to-DC converter and an electronically and linearly tunable OTA which suitable to implement in CMOS technology. Moreover some applications were used to demonstrate the design flexibility of the approaches. Although they have some disadvantages, however they can be improved on the future work.

5.2 Suggestions for future work

From this work, we can suggest for future work based on the experience and the knowledge acquired. We found that the performances of the proposed true RMS-to-DC converter and the EOTA that studied from the simulation and the experimental results still provide the error of about 10%. Due to the circuit structure of the proposed true RMS-to-DC converter and the proposed EOTA are composed of the basic current mirrors, the current mirror mismatch causes the DC off-set current which will effects to the accuracy of the circuits. For the proposed true RMS-to-DC converter that designed by feedback the output current (I_{RMS}) to be the DC bias current of the circuit, if the current mirrors have the DC off-set current the error of the output current will occur. For the proposed EOTA, the error of the circuit is also cause by the current mirror mismatch. From this result both circuit accuracy can be improve by using the topology that improve the current mirror, such as, the cascode current mirror.

Since the proposed circuits are designed based on square law characteristics that the MOS transistors are operated in saturation region, therefore to maintain the circuit that still operate in the linear range and low total harmonic distortion, the MOS transistors should be biased in saturation region.

For the proposed voltage-controlled current amplifier that designed and restricted by using the proposed EOTA, the gain current is not high due to the current gain, $A_i = 2K_T V_C$, which depend on the K_T where K_T is a small value. However, we can improve the current amplifier for higher gain by given the current gain ratio of the current mirrors of the balanced CMOS OTA much more than the unity. By the OTA schematic diagram in Fig.2.9, if we assume that the current mirrors M_3 - M_4 , M_5 - M_6 and M_7 - M_8 have current gain ratios equal to $1:n$, $1:n$ and $n:n$, respectively. The current gain of the voltage-controlled current amplifier can be obtained by $A_i = 2nK_T V_C$. We can found that if we set n much more that unity, the current gain can be tuned for the wide range.

Moreover the proposed EOTA should be developed by designing a new transconductance cell for reducing the number of transistors that will be reduces the power consumption of both proposed circuits and that wider signal dynamic range may be possible at the low power supply voltage.