CHAPTER 4

Electronically and Linearly Tunable CMOS OTA

4.1 Introduction

Linear transconductors or voltage-to-current converter circuits are fundamental building blocks of analog circuits and systems. They are found useful in interface circuits, instrumentation amplifiers, continuous-time-filters and oscillators. In addition, when the transconductance gain of the transconductor can be electronically varied, they can also be applied in automatic gain control circuits and in analog multipliers. In the last two decades, it is well accepted that a linear transconductor, which is constructed from a bi-polar differential pair and current mirrors, called as an operational transconductance amplifier (OTA), is one of the essential active building blocks in the design of analog circuits [67]-[69]. This is due to the fact that the OTA is a low-cost device that has only a single high-impedance node and its transconductance gain g_m can be linearly controlled over more than four decades by means of an external bias current. Moreover, the implementation of analog circuits in such a way that employs only OTA as standard cells will not only be easily constructed from readily commercial available IC, but also significantly simplified the design.

The main objective of this chapter is, therefore, to present a circuit design technique for the synthesis of a linear electronically tunable CMOS OTA, called as an EOTA. Since, the realization method is achieved by squaring the transconconductance gain of the CMOS OTA, the transconductance gain of the EOTA is directly depend on the DC bias current. To provide a maximum output voltage swing and wide linearly tunable transconductance range, a balanced CMOS OTA or voltage to current transducer will be employed as basic active circuit elements to realize the EOTA, whereas the completed EOTA requires 3 balanced CMOS OTAs. Since it is generally assume that all MOS transistors are operating in the saturation region, hence the individual functions of the circuits are derived from the approximate square-law characteristic of MOS transistors in saturation. In addition, it is well accepted that the design and implementation of electronically tunable analog circuits using bipolar-based OTA as active circuit elements are well established and well tabulated. Then, having access to such a linear electronically tunable CMOS OTA, it would enable us to realize CMOS analog circuits with their property can be electronically tuned by simply replace a bipolar OTA with an EOTA. This kind of advantage will be

demonstrated through application examples. For the first example, the proposed EOTA is employed to implement a current multiplier circuit, that using only active elements and without the requirement of external passive elements and the current amplifier, a linearly voltage-controlled current amplifier and a linearly current-controlled CMOS current amplifier, are illustrated in the second application example. The circuit performances are studied through PSPICE simulation results.

4.2 The available electronically tunable CMOS OTA

In CMOS technology, several linearly tunable transconductors based on the use of MOS transistors operating in saturation region have been proposed in the literatures [70]-[73]. Most of them are functioning in voltage controlled mode. The method of source-follower of the reference [70] is operated in square law characteristic with constant source-bulk voltages, where the control voltage is applied to the gate. Whereas for the cross coupled connection methods [71]-[73], the transconductance control voltages are applied through voltage level shifters. However, their controllable voltage ranges are rather limited and only narrow linearly tunable transconductance ranges are available. In some applications, such as, an analog multiplier circuit, a frequency divider/multiplier circuit and an arbitrary power-law circuit, current controlled transcondcutors that this trasconductance gain can be linearly controllable by a DC bias current are preferable [74]-[76]. In the past, a current controlled CMOS transconductor was presented in [77]. But the linearly tunable transconductance range is narrow due to the MOS transistors are working in the weak-inversion region.

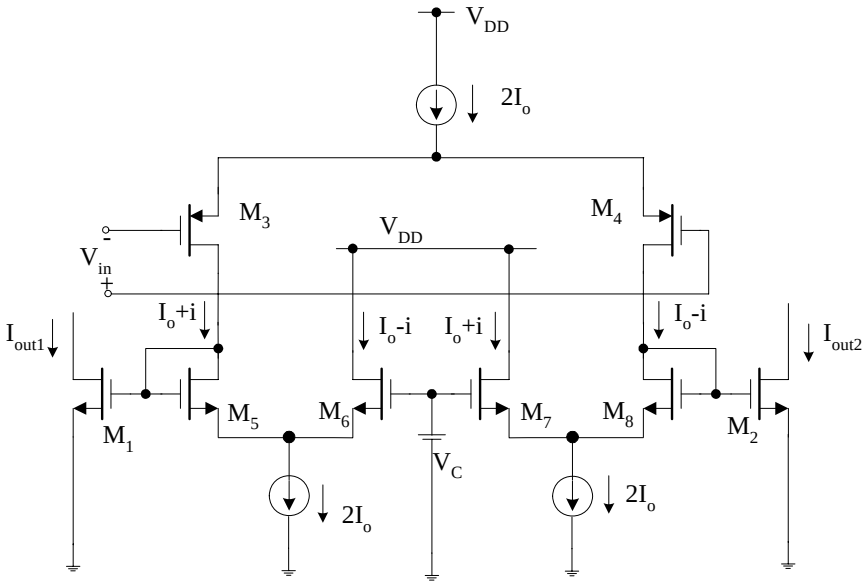

Fig. 4.1 A linear transconductor circuit [70]

In Fig. 4.1, the linear CMOS trasconductor circuit which proposed by *S.-C. Huang and M. Ismail* [70] has a transconductance linearly variable by a gate voltage (V_C). From this proposed circuit, the circuit is based on the square-law behavior of MOS transistors are biased in saturation regions

$$I_d = K\left(V_{GS} - V_{TH}\right)^2 \qquad (4.1)$$

Transistors M_1 and M_2 are the square-law transistors that perform the actual transconductor function. Transistor M_3-M_8 constitute three differential matched pairs with equal tail current $2I_o$. This pairs are connected in such a way that M_5-M_6 and M_7-M_8 carry the same currents as M_3-M_4. As a result of this, voltage V_{in} is copied to the transconductor transistors M_1 and M_2. This is shown as follows: presume that M_3 and M_4 are characterized by K_3 and V_{th3}, M_5-M_8 by K_5 and V_{th5}. Using equation (4.1) and referring to Fig. 4.1, the following relation may be written

$$V_{in} = \left(\sqrt{I_o + i} - \sqrt{I_o - i}\right) \Big/ \sqrt{K_3} \qquad (4.2)$$

$$V_{GS5} - V_{GS6} = V_{GS7} - V_{GS8} = \left(\sqrt{I_o + i} - \sqrt{I_o - i}\right) \Big/ \sqrt{K_3}$$

$$= \sqrt{K_3 / K_5}\, V_{in} \qquad (4.3)$$

From eqn. (4.3) that two proportional copies of V_{in} arise across the lower differential pairs. These voltages are added to and subtracted from transconductance control voltage V_C. Using eqn. (4.1) and presuming that M_1 and M_2 are charzcterised by K_1 and V_{TH1}, the output currents I_{out1} and I_{out2} can be calculated:

$$I_{out1} = K_1\left(V_C + \sqrt{K_3/K_5}V_{in} - V_{TH1}\right)^2 \tag{4.4}$$

$$I_{out2} = K_1\left(V_C - \sqrt{K_3/K_5}V_{in} - V_{TH1}\right)^2 \tag{4.5}$$

the differential output current (I_{out1}-I_{out2}) is in the function of the control voltage V_C as expressed in eqn. (4.6)

$$I_{out1} - I_{out2} = 4K_1(V_C - V_{TH1})\sqrt{K_3/K_5}V_{in} \tag{4.6}$$

eqn. (4.6) describes the transfer function of a linear transconductor. Its transconductance value is linearly variable by voltage V_C.

However the controllable range of this circuit is narrow due to V_C must be bias the MOS transistors keep operate in saturation region.

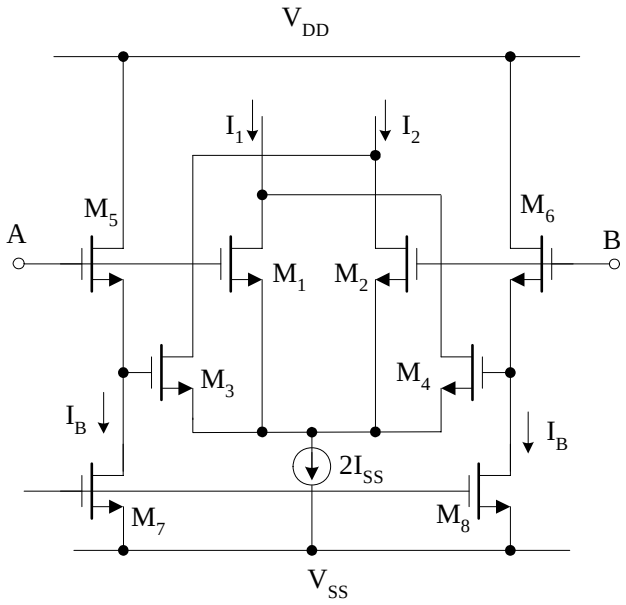

Fig. 4.2 Linear Transconductor circuit based on cross-coupled technique [72]

Fig. 4.2 shows the linear CMOS trasconductor circuit which was proposed by *Z. Wang and W. Gugenbuhl* [72] . The linear transfer characteristic is obtained by two cross-coupled differential transistor pairs operating in saturation pairwise at unequal bias, offering offset-free operation with both differential or single-ended input and differential output. From the figure, the MOS transistors M_1-M_4 and M_5-M_8 have the same dimensions operating in saturation regions. Therefore the control voltage V_B , which is applied to the gates of M_7 and M_8, is identical to the gate-source voltage of M_5 and M_6 and acts as a voltage shift from the inputs to the gate of M_3 and M_4. Applying the square law characteristics, the differential output current of this circuit can be expressed as

$$I_o = I_1 - I_2 = 2KV_B(V_P - V_N) \tag{4.7}$$

where V_P and V_N are the gate source voltage of M_1 and M_2.
Since the differential input voltage V_{in}=V_P-V_N eqn. (4.7) , yields

$$I_o = I_1 - I_2 = 2KV_BV_{in} \tag{4.8}$$

The transconductance is $G=2KV_B$, which is linearly controllable by the voltage V_B. However, its controllable voltage range is rather limited and only narrow linearly tunable transconductance range.

4.3 An Electronically and Linearly Tunable CMOS OTA (EOTA)

In this section, the realization method of an electronically and linearly tunable CMOS OTA is proposed. The proposed EOTA is achieved by squaring the transconductance gain of the balanced CMOS OTA. The EOTA transconductance gain can be linearly tuned by an external bias current for wide range (3 decades).

4.3.1 Circuit description the EOTA

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. It means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ \ V_{GS} > V_T \\ 0 & , \ for \ \ V_{GS} \le V_T \end{cases} \tag{4.9}$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

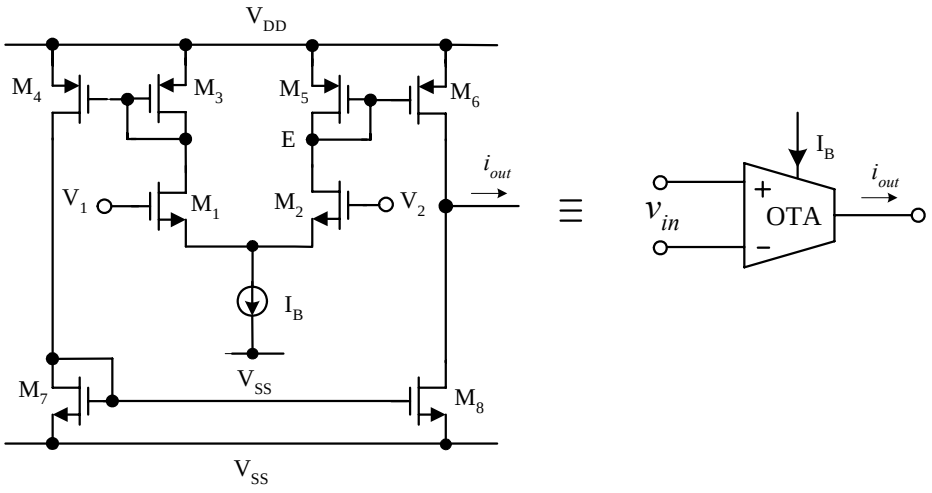

Fig. 2.11 Schematic diagram of a balanced CMOS OTA

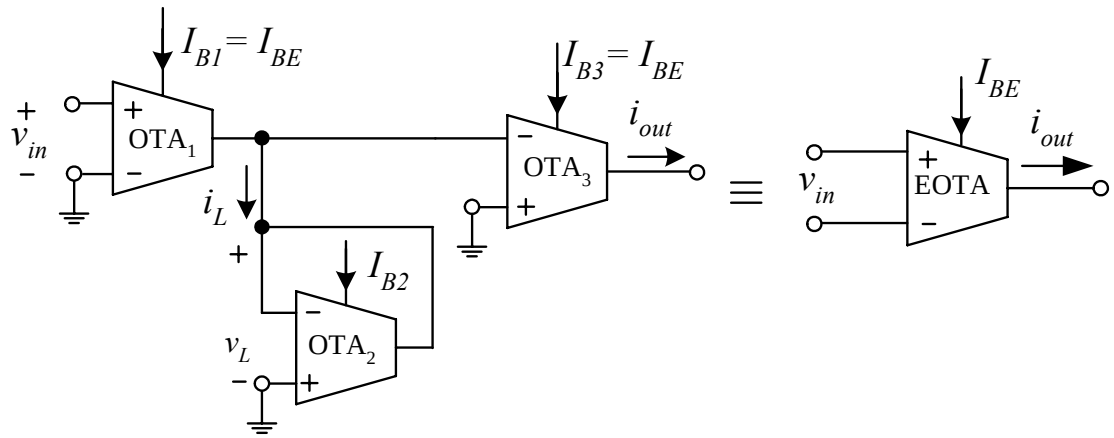

Fig. 4.3 The proposed electronically and linearly tunable CMOS OTA

Through the use of three balanced single-output CMOS OTAs, a CMOS-based electronically and linearly tunable OTA, called as an EOTA, can be realized by the circuit diagram shown in Fig. 4.3. The OTA_1 converts a differential input signal voltage $v_{in} = v_1 - v_2$ into a signal current i_L to flow into an active resistor R_L, formed by the OTA_2, where $R_L = 1/g_{m(OTA2)}$ and $g_{m(OTA2)}$ represents the transconductance gain of the OTA_2. Since the current signal $i_L = g_{m(OTA1)}V_{in}$, the voltage drop across the active resistor (OTA_2) becomes

$$v_L = i_L Z_L = g_{m(OTA1)} v_{in} \cdot \frac{1}{g_{m(OTA2)}} \tag{4.10}$$

The OTA_3 will convert the voltage v_L, with the transconductance gain of $g_{m(OTA3)}$, into the output current i_{out} as

$$i_{out} = g_{m(OTA3)} v_L \tag{4.11}$$

From eqns. (4.10) and (4.11), the current i_{out} can be rewritten as

$$i_{out} = \frac{g_{m(OTA1)} g_{m(OTA3)}}{g_{m(OTA2)}} v_{in} \tag{4.12}$$

Since $g_{m(OTA1)} = \sqrt{2I_{B1}K_1}$, $g_{m(OTA2)} = \sqrt{2I_{B2}K_2}$ and $g_{m(OTA3)} = \sqrt{2I_{B3}K_3}$, if we set $I_{B1}=I_{B3}=I_{BE}$, then from eqn. (4.12) we obtain

$$i_{out} = \frac{2I_{BE}\sqrt{K_1 K_3}}{\sqrt{2I_{B2}K_2}} V_{in} = g_{mT} v_{in} \tag{4.13}$$

where g_{mT} represents the transconductance gain of the proposed EOTA and can be expressed as

$$g_{mT} = 2I_{BE}K_T \tag{4.14}$$

and $K_T = \sqrt{K_1 K_3 / 2I_{B2}K_2}$, which can usually be kept to be constant. The eqn. (4.14) clearly indicted that the transconductance gain of the proposed EOTA can be electronically and linearly tuned by the bias current I_{BE}. This linear relationship is in the form that similar to the

transconductance gain of the bipolar based OTA that found useful in many applications [78]. Since the balanced CMOS OTA is formed by MOS coupled pair and current mirrors, therefore, the proposed EOTA is very suitable for fabricating in CMOS integrated form.

4.3.2 Circuit Performances

4.3.2.1 Operating range

It is well accepted that the prediction of the eqn. (4.14) will be valid only for a small value of V_{in}. From the eqn. (2.44), since OTA_1 and OTA_3 are formed by MOS coupled pairs, to maintain in the linear range and low total harmonic distortion, the voltages V_{in} and V_L should respectively be restricted to the ranges of [79]

$$\left|V_L\right|_{MAX} = 0.4/\sqrt{2}K \cdot Z_L \text{ and } \left|V_{in}\right|_{MAX} = 0.4\sqrt{I_{BB}/K} \qquad (4.15)$$

where it should be noted from the eqn. (4.15) that the maximum usable voltage range is limited by $\left| V_L \right|_{MAX}$ if $g_{m(OTA1)}/g_{m(OTA2)} > 1$ and it is limited by $\left| V_{in} \right|_{MAX}$ if $g_{m(OTA1)}/g_{m(OTA2)} < 1$. For example, for I_{BE} = 1mA and I_{B2} = 700μA, the maximum usable range is determined by $\left| V_L \right|_{MAX}$ and $\left| V_L \right|_{MAX}$ is about 0.94 volts, for $K = \mu_n C_{ox} W/2L = 1.27 \times 10^{-4}$ A/V^2, $\mu_n C_{ox} = 5.08 \times 10^{-5}$ V and $W/2L = 2.5$.

4.3.2.2 Conversion Errors

4.3.2.2.1 Error analysis

The transconductance gain error that results from in the inaccuracy of the EOTA can be determined from a large signal analysis. Consider the balanced CMOS OTA, the transconductance gain G_m of the eqn. (2.45) can be written as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}} \text{ , } for - \sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \qquad (4.16)$$

If we set the transconductance error of the balanced CMOS OTA of the Fig. 4.3 as $E=\frac{KV_{in}^2}{2I_{BB}}$, then eqn. (4.16) can be rewritten as

$$G_m = \frac{i_{out}}{V_{in}} = \sqrt{2I_B K}\cdot\sqrt{1-E} \tag{4.17}$$

We found that the G_m will equal to the g_m of eqn. (2.46) in the condition that $KV_{in}^2/2I_B$ <<1. This can be achieved by keeping the input voltage signal V_{in} small or set the DC bias current I_B to a large value.

By applying the G_m of the eqn. (4.17) to the circuit of Fig. 4.3, we obtain the transconductance gain of the proposed EOTA for large signal as

$$G_{mT} = 2I_{BE}K_T\left(1+\frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}}\right) \tag{4.18}$$

where the errors $E_1=\frac{K_1V_{in1}^2}{2I_{B1}}$, $E_2=\frac{K_2V_{in2}^2}{2I_{B2}}$ and $E_3=\frac{K_3V_{in3}^2}{2I_{B3}}$ are the transconductance errors due to the OTA_1, OTA_2 and OTA_3 respectively. Given that E_T is the transconductance error of the EOTA from the linear transconductance gain, we can write

$$E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}} \tag{4.19}$$

Thus, we have the percent of the conversion error as

$$\%E_T = \frac{\sqrt{1-E_1}\sqrt{1-E_3}-\sqrt{1-E_2}}{\sqrt{1-E_2}}\times 100\% \tag{4.20}$$

For example, if V_{in1} = 0.5V, V_{in2}= V_{in3}= 0.751V, I_{B1}= I_{B3}= I_{BE} = 1mA, I_{B2}= 700μA and K_1= K_2= K_3= 1.27×10^{-4}, the resulting transconductance error ($\%E_T$) is equal to 0.54%

4.3.2.3 High frequency response

Due to the proposed electronically and linearly tunable CMOS OTA as shown in Fig. 4.3 is composed of three balanced CMOS OTAs, the high frequency response of this circuit can be verified by treated as the balanced CMOS OTAs that are connected in cascade. Using of the Fig. 2.11, the transconductance gain $g_{m(OTA)}$ of the CMOS OTA is now model as a single dominant pole as [80][84]

$$g_{m(OTA)} = g_{m2} \Big/ \left[1 + \left(sC_p / g_{m5}\right)\right] \tag{4.21}$$

where g_{m2} and g_{m5} denote the transconductance of the transistor M_2 and M_5 of the OTA, respectively. From the Fig. 2.11, we denote C_p as the capacitance that associated with the node E of the current mirror M_5-M_6 and $C_p = C_{gs2}+C_{gd2}+C_{gs5}+C_{gd5}+C_{gs6}$ where C_{gs} represents the gate-source capacitance of the transistor and C_{gd} represent the gate-drain capacitance of the transistor.

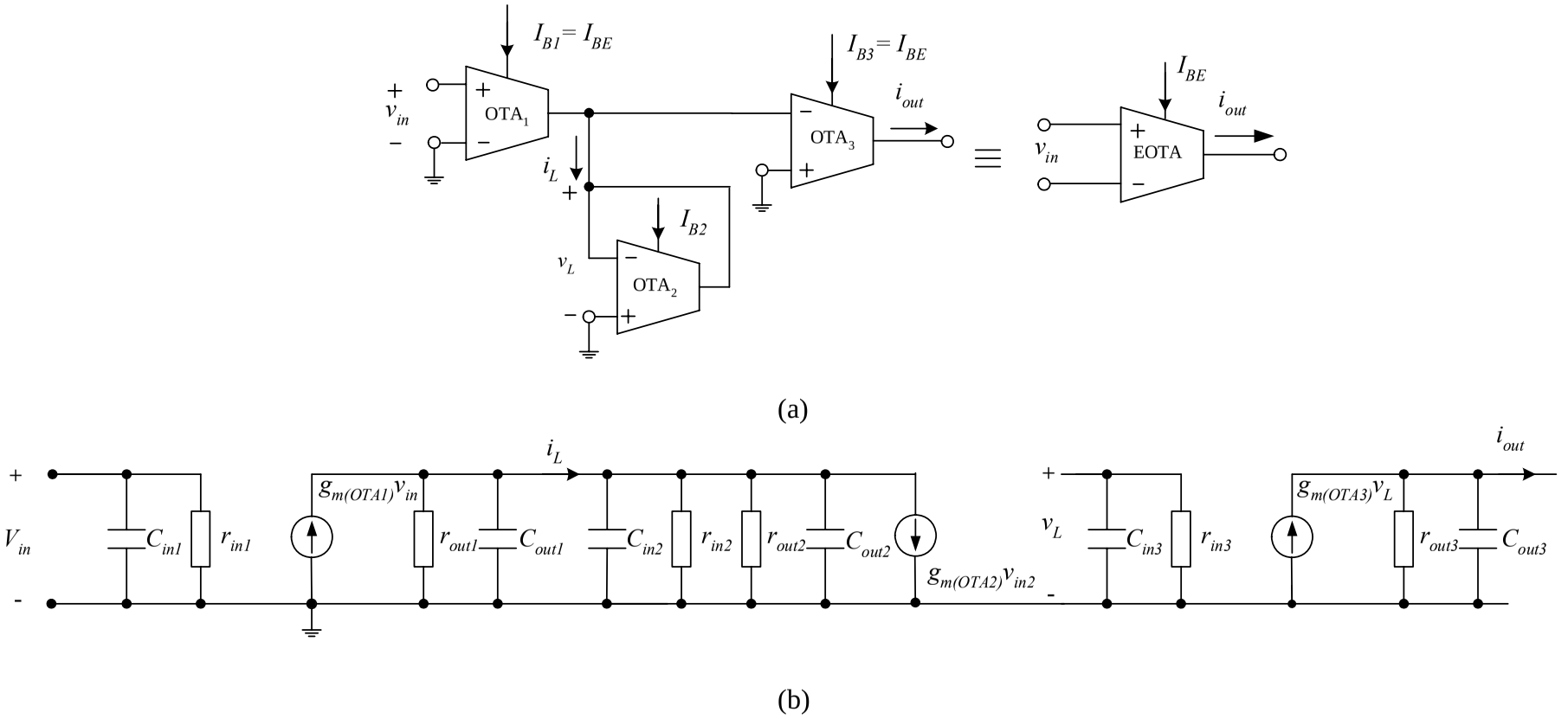

Fig. 4.4 The electronically and linearly tunable CMOS OTA

(a) building block diagram
(b) small signal equivalent circuit

From the Fig. 4.4, the active resistor R_L which is formed by OTA_2 can be expressed as

$$R_L = \frac{1}{g_{m(OTA2)} + g_{in(2)} + g_{out(2)} + s(C_{in(2)} + C_{out(2)})} \qquad (4.22)$$

Where $g_{m(OTA2)}$ is transconductance gain of the OTA_2

$g_{in(2)} = 1/r_{in(2)}$ where $r_{in(2)}$ is the input resistance of OTA_2

$g_{out(2)} = 1/r_{out(2)}$ where $r_{out(2)}$ is the output resistance of OTA_2

$C_{in(2)}$ is the input capacitance of the OTA_2

$C_{out(2)}$ is the output capacitance of the OTA_2

If $g_{m(OTA2)} >> g_{in(2)}$, $g_{out(2)}$ and $C_{p(2)} >> C_{out(2)}$ and $C_{in(2)} = C_{gs1}+C_{gs2}$, therefore eqn.(4.22) can be approximately expressed as

$$R_L = \frac{1}{g_{m(OTA2)} + sC_{in(2)}} \qquad (4.23)$$

Through circuit analysis using eqn.(4.23), the transfer function of the EOTA can be expressed as

$$\frac{i_{out}(s)}{V_{in}(s)} = \frac{g_{m(OTA1)}g_{m(OTA3)}}{g_{m(OTA2)}} \frac{(s+z_2)}{(s+p_1)(s+p_3)(s+p_{L1})(s+p_{L2})} \qquad (4.24)$$

Then from eqn. (4.24), the zero and poles z_2, p_1, p_3, p_{L1} and p_{L2} can be respectively expressed as

$$p_1 = \frac{g_{m5(1)}}{2\pi C_{p(1)}},\ p_3 = \frac{g_{m5(3)}}{2\pi C_{p(3)}},\ z_2 = \frac{g_{m5(2)}}{2\pi C_{p(2)}},\ p_{L1}, p_{L2} = \frac{-\frac{C_{in(2)}}{g_{m2(2)}} \pm \sqrt{\left(\frac{C_{in(2)}}{g_{m2(2)}}\right)^2 - 4\frac{g_{m5(2)}C_{in(2)}C_{p(2)}}{g_{m2(2)}}}}{2\frac{g_{m5(2)}C_{in(2)}C_{p(2)}}{g_{m2(2)}}} \qquad (4.25)$$

Note that the poles due to the active resistor R_L, p_{L1} and p_{L2}, are always real poles since $\left(C_{in(2)}/g_{m2(2)}\right)^2 > -4\left(g_{m5(2)}C_{in(2)}C_{p(2)}\right)/g_{m2(2)}$, where $g_{m(OTA1)} = g_{m2(1)}$, $g_{m(OTA2)} = g_{m2(2)}$ and $g_{m(OTA3)} = g_{m2(3)}$. The $g_{mi(1)}$, $g_{mi(2)}$ and $g_{mi(3)}$ represent the transconductance of transistor M_i of OTA_1, OTA_2 and OTA_3 respectively, for $i = 1, 2, 3,...$ and $C_{p(1)}$, $C_{p(2)}$, and $C_{p(3)}$ represent the total capacitances at nodes E

of the OTA_1, OTA_2 and OTA_3, respectively. For example, the following data have been used; V_{in} = 0.1V, I_{BE} = 100μA and I_{B2} = 40μA, $g_{m(OTA1)} = g_{m2(1)} = 1.66\times10^{-4}AV^{-1}$, $g_{m(OTA2)} = g_{m2(2)} = 9.44\times10^{-5}AV^{-1}$, $g_{m(OTA3)} = g_{m2(3)} = 1.56\times10^{-4}\ AV^{-1}$, $g_{m5(1)} = 1.96\times10^{-4}\ AV^{-1}$, $g_{m5(2)} = 1.18\times10^{-4}AV^{-1}$, $g_{m5(3)} = 1.96\times10^{-4}\ AV^{-1}$, $C_{gs1} = C_{gs2}$ = 0.268 pF, $C_{gs5} = C_{gs6}$ = 0.54 pF and $C_{gd2} = C_{gd5}$ = 0pF (at saturation region C_{gd}=0). $C_{in(2)} = C_{gs1(2)}+C_{gs2(2)}$ = 0.536pF.

The poles and zero frequencies are located as p_1 = 23 MHz, p_3 = 23 MHz , p_{L1} = 88 MHz, $p_{L2}= 1.26\times10^{6}$ MHz and z_2 = 14 MHz. We found that the high frequency limitation is due to the zero (z_2) that associated with the OTA_2. Since these poles and zero locations depend on the DC bias current of the OTAs which can be expressed in eqn.(4.25), therefore the circuit can be operated in a wider bandwidth by increasing the dc bias currents (higher resistance value) of the circuit. For example, in the case of, V_{in} = 0.1V, I_{BE} = 1mA and I_{B2} = 400μA, the high frequency limitation is located at 38MHz.

4.3.3 Application examples

4.3.3.1 Current Multiplier

In this section, we will propose the use of the EOTA to realize a current-mode multiplier, which use only active circuit elements and not require external passive circuit elements. The proposed current-mode multiplier circuit is shown in Fig. 4.2 which this structure has been proposed by the author in [81]. It should be noted from the eqn. (4.14) that if the EOTA is operated in the linear range, the transconductance is $g_{mT} = 2I_{BE}K_T$, which g_{mT} can be tuned by the DC bias current I_{BE}.

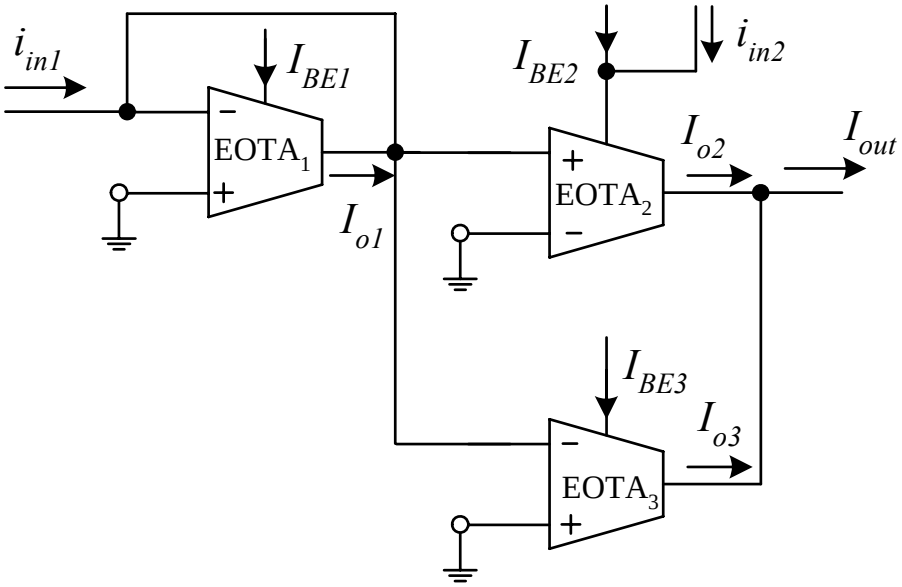

Fig. 4.5 The current-mode multiplier circuit using the proposed EOTA.

From the Fig. 4.5, the input signal current i_{in1} is injected into the EOTA$_1$, which is connected as a current controlled grounded resistor. The voltage across the EOTA$_1$ is then used as the input voltage for the EOTA$_2$ and EOTA$_3$. The input signal current i_{in2} is added with the bias current I_{BE2} of the EOTA$_2$. Let g_{mT1}, g_{mT2} and g_{mT3} be the transconductance gains of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively. Then from the eqn. (4.14) and from routine circuit analysis the output currents I_{o2} and I_{o3} of the EOTA$_2$ and EOTA$_3$, respectively, can be written as

$$I_{o2} = \frac{g_{mT2}}{g_{mT1}} i_{in1} = \frac{(I_{BE2} + i_{in2})}{I_{BE1}} i_{in1} \tag{4.26}$$

and

$$I_{o3} = -\frac{g_{mT3}}{g_{mT1}} i_{in1} = -\frac{I_{BE3}}{I_{BE1}} i_{in1} \tag{4.27}$$

where I_{BE1} , I_{BE2} and I_{BE3} represent the DC bias currents of the EOTA$_1$, EOTA$_2$ and EOTA$_3$, respectively, and the transconductance gains $g_{mT1} = 2I_{BE1}K_{T1}$, $g_{mT2} = 2(I_{BE2} + i_{in2})K_{T2}$ and $g_{mT3} = 2I_{BE3}K_{T3}$. Noting from the Fig. 2.11 and Fig. 4.5, that the DC bias current of the EOTA (I_{BE}) of the multiplier circuit can be achieved by setting the DC bias currents of the OTA$_1$ and the OTA$_3$ to $I_{B1} = I_{B3} = I_{BE}$. If we set $I_{BE2} = I_{BE3} = I_b$, the output current I_{out} of the circuit that is the summation of the currents I_{o2} and I_{o3} can be expressed as

$$I_{out} = I_{o2} + I_{o3} = \frac{i_{in1} i_{in2}}{I_{BE1}} \tag{4.28}$$

which is in the form of a current-mode multiplication function.

4.3.3.2 Current Amplifiers

In this section, the realization of the current amplifiers by using EOTA, which use only active circuit elements, are described.

4.3.3.2.1 Linearly voltage-controlled current amplifier

The proposed voltage-controlled tunable current amplifier is constructed as the circuit diagram in Fig. 4.6. Where the input signal current (i_{in}) is added to the DC bias current (I_{BE}). The control voltage (V_C) is supplied to the input of EOTA. From the routine circuit analysis of Fig. 4.3, the output current (i_{out}) can be expressed as

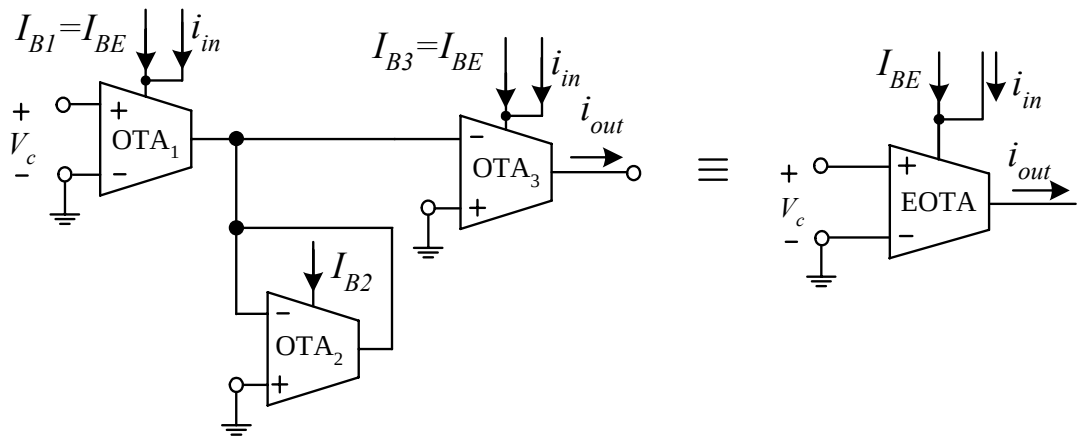

Fig. 4.6 A linearly voltage-controlled current amplifier

$$i_{out} = 2K_T V_C \left(i_{in} + I_{BE} \right) \tag{4.29}$$

$$i_{out} = \left(2K_T V_C \right) i_{in} + \left(2K_T V_C \right) I_{BE} \tag{4.30}$$

From the eqn. (4.30), we found that the output current consists of the AC signal and DC current ($2K_T V_C \cdot I_{BE}$). If we can compensate this DC current, the output current of the voltage controlled current amplifier can be rewritten as

$$i_{out} = \left(2K_T V_C \right) i_{in} = A_i i_{in} \tag{4.31}$$

Where A_i is the current gain of the proposed voltage controlled current amplifier and can expressed as

$$A_i = 2K_T V_C \tag{4.32}$$

and $K_T = \sqrt{K_1 K_3 / 2 I_{B2} K_2}$. It shows that the output current can be linearly tuned by the DC voltage V_C.

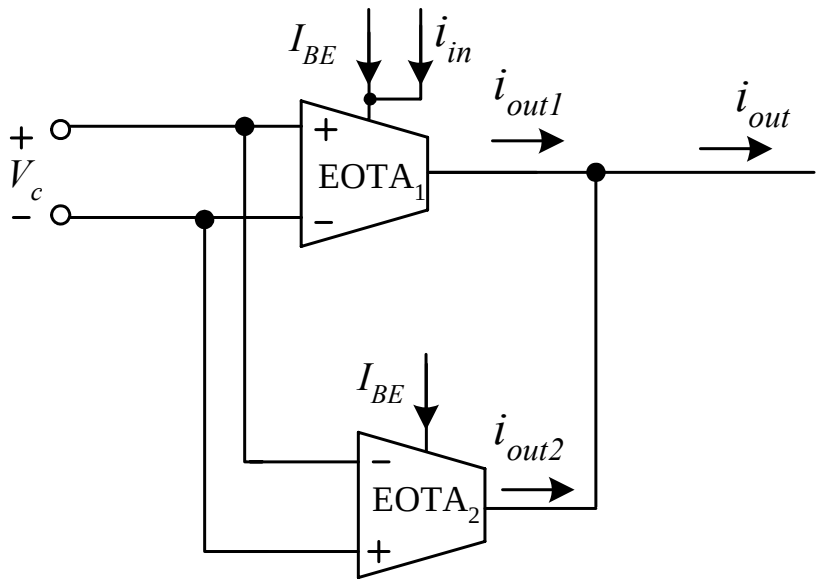

Fig. 4.7 Schematic diagram of the current amplifier with DC gain compensated

Fig. 4.7 shows the circuit building block to eliminate the DC current of Fig. 4.6 where i_{out1} and i_{out2} are given as,

$$i_{out1} = \left(2K_T V_C\right) i_{in} + \left(2K_T V_C\right) I_{BE} \tag{4.33}$$

and

$$i_{out2} = -\left(2K_T V_C\right) I_{BE} \tag{4.34}$$

The output current i_{out} of the circuit, that is the summation of the currents i_{out1} and i_{out2}, can be expressed as

$$i_{out} = i_{out1} + i_{out2} = \left(2K_T V_C\right) i_{in} \tag{4.35}$$

From eqn. (4.35) it is clearly seen that the circuit can operate as a current amplifier, the gain of which can be linearly tuned by the control voltage (V_C).

4.3.3.2.2 Linearly current-controlled CMOS current amplifier

A current amplifier design based by on EOTA that can electronically and linearly be tunable is proposed in Fig. 4.8 which is composed of one balanced single-output CMOS OTA and one EOTA.

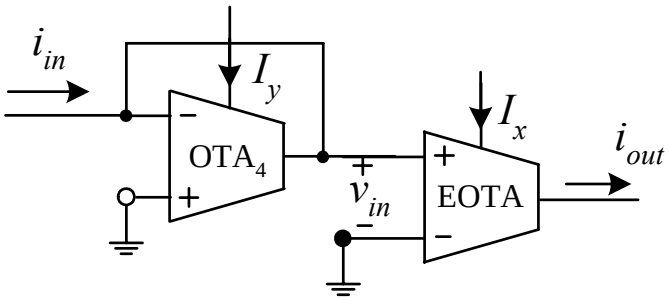

Fig. 4.8 A linearly current-controlled tunable current amplifier

The input current (i_{in}) is injected into the OTA$_4$, which is formed as an active resistor ($1/g_{m(OTA4)}$). The voltage drop across the active resistor (OTA$_4$) is then used as an input voltage (v_{in}) for EOTA and can be expressed as

$$v_{in} = \frac{i_{in}}{g_{m(OTA4)}} \tag{4.36}$$

The EOTA will convert the voltage v_{in} into the output current i_{out} as

$$i_{out} = g_{mT} v_{in} \tag{4.37}$$

From eqns. (4.36) and (4.37), the current i_{out} of the proposed current-controlled current amplifier can be written as

$$i_{out} = \frac{g_{mT}}{g_{m(OTA4)}} i_{in} \tag{4.38}$$

where $g_{mT} = g_{m(OTA1)} g_{m(OTA3)} / g_{m(OTA2)}$, $g_{m(OTA1)} = \sqrt{2 I_{B1} K_1}$, $g_{m(OTA2)} = \sqrt{2 I_{B2} K_2}$, $g_{m(OTA3)} = \sqrt{2 I_{B3} K_3}$ and $g_{m(OTA4)} = \sqrt{2 I_{B4} K_4}$. If we set $K_1 = K_2 = K_3 = K_4 = K$ and $I_{B4} = I_{B2} = I_y$, $I_{B1} = I_{B3} = I_{BE} = I_x$, then from eqn. (4.38) we obtain

$$i_{out} = \frac{g_{m(OTA1)} g_{m(OTA3)}}{g_{m(OTA2)} g_{m(OTA4)}} i_{in} \tag{4.39}$$

Since

$$i_{out} = \frac{I_x}{I_y} i_{in} = A_C i_{in} \tag{4.40}$$

where A_C is the current gain of the proposed current amplifier and can be expressed as

$$A_C = \frac{I_x}{I_y} \tag{4.41}$$

We can see that the output current can be tuned by the DC bias current I_x and I_y. If indicates that the gain is direct proportional to I_x and inverse proportional to I_y.

4.4 Simulation results

The performance of the proposed electronically and linearly tunable CMOS OTA was verified through the use of PSPICE simulation results. All the OTA was simulated by using CMOS transistor parameters of the SCN2 level 2 of MOSIS. The transistor dimensions of the circuit in Fig. 2.11 are in micron, where the dimensions of the transistors M_1 and M_2 are W=50μm and L=10μm, the dimensions of the transistor M_3-M_8 are W=100μm and L=10μm. The power supply voltage were set to $V_{DD} = -V_{SS} = 5V$.

To demonstrate that the circuit can linearly converted voltage signal into current signal, Fig. 4.9 shows the simulated transfer characteristic of the EOTA of the Fig. 4.3. The plots of the output current I_{out} versus the input voltage V_{in} show that, for the dc bias current (I_{BE}) in the cases of 1mA, 800μA and 400μA, the EOTA can linearly convert the input voltage into output signal current with nonlinearity of less than 1% for the input voltage (V_{in}) in the ranges of -1V to 1V, -0.86V to 0.86V and -0.66V to 0.66V, respectively. These results were agreed with the prediction value from the eqn. (4.14). The conversion error in the case of I_{BE}=1mA is plot in Fig. 4.10. For example, for the case of the DC bias current I_{BE} = 1mA and for V_{in} = 0.86V, I_{B2} = 700μA, the transconductance gain $g_{mT} = 5.398 \times 10^{-4}$ AV^{-1}, where the conversion error is about 0.6%. The frequency response of the EOTA was also studied, where the -3 dB bandwidth of about 120 MHz is achieved.

The relation between the transconductance and the bias current I_{BE} was measured by fixing V_{in} = 0.1V and varying I_{BE} from 10nA to 1mA. The results are plot in Fig. 4.11. From this, it can be seen that the transconductance is linearly dependent upon the bias current I_{BE} over the range of 1μA to 1mA (three decades). It found that the transconductace can be tune linearly by I_{BE}, where at I_{BE} =1mA the conversion error from simulation result is about 0.68%, where its conversion error of g_{mT} versus I_{BE} is plot in Fig. 4.12.

The lower limit of the circuit is due to condition in eqn. (2.44) that transistors must be operating in saturation region. In the cases of V_{in} = 0.1V, 0.2V and 0.5V, respectively, we found that the DC bias current I_{BE} must be more than 1μA, 5μA and 32μA, respectively.

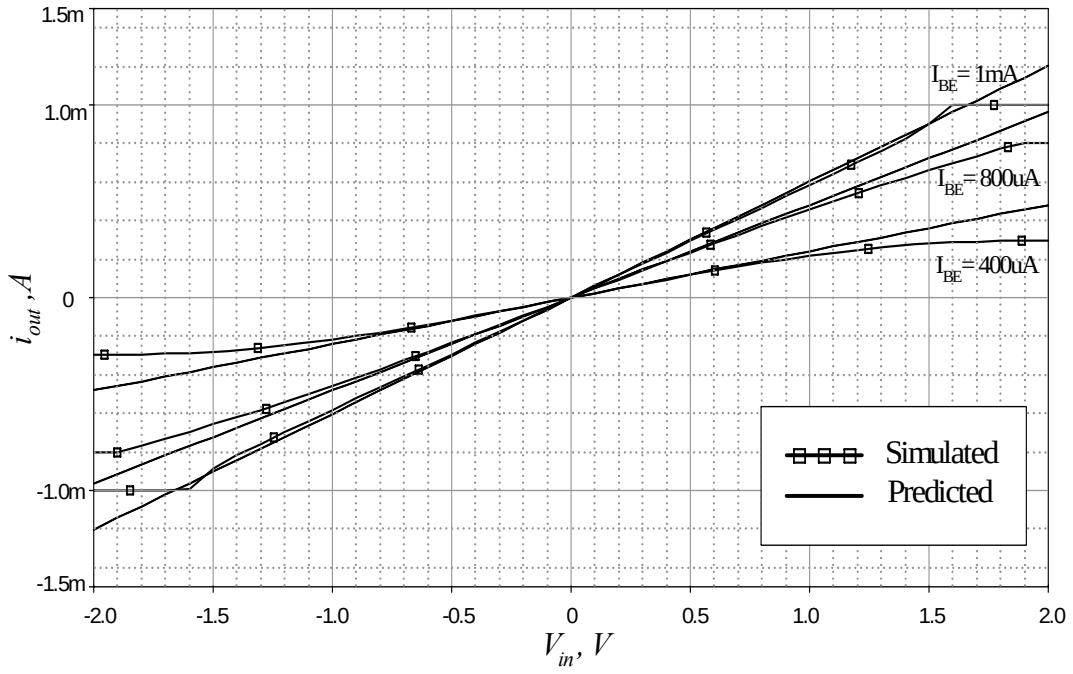

Fig. 4.9 DC transfer characteristics of the EOTA

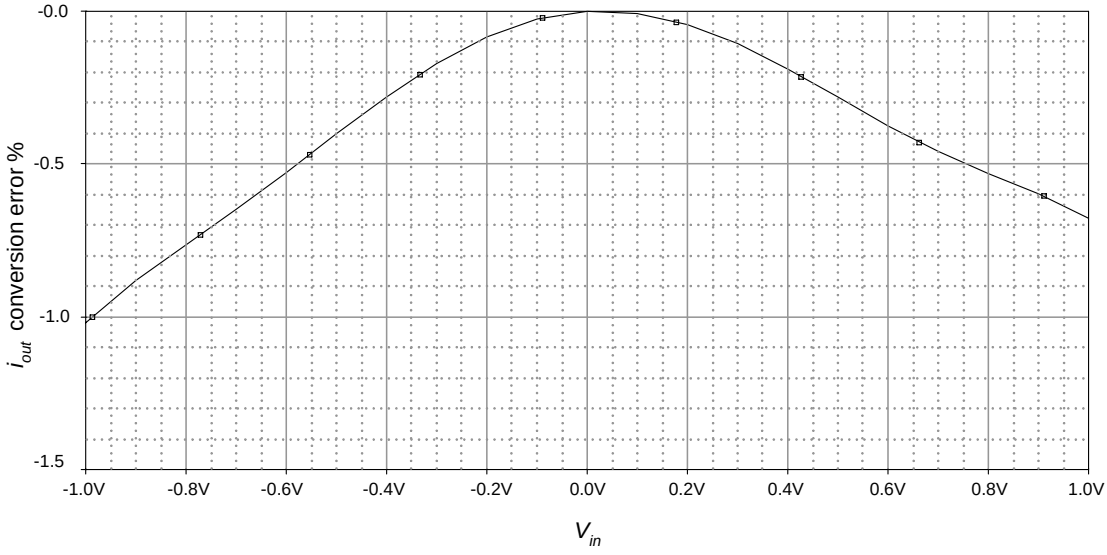

Fig. 4.10 Conversion error of i_{out} versus V_{in} of the EOTA

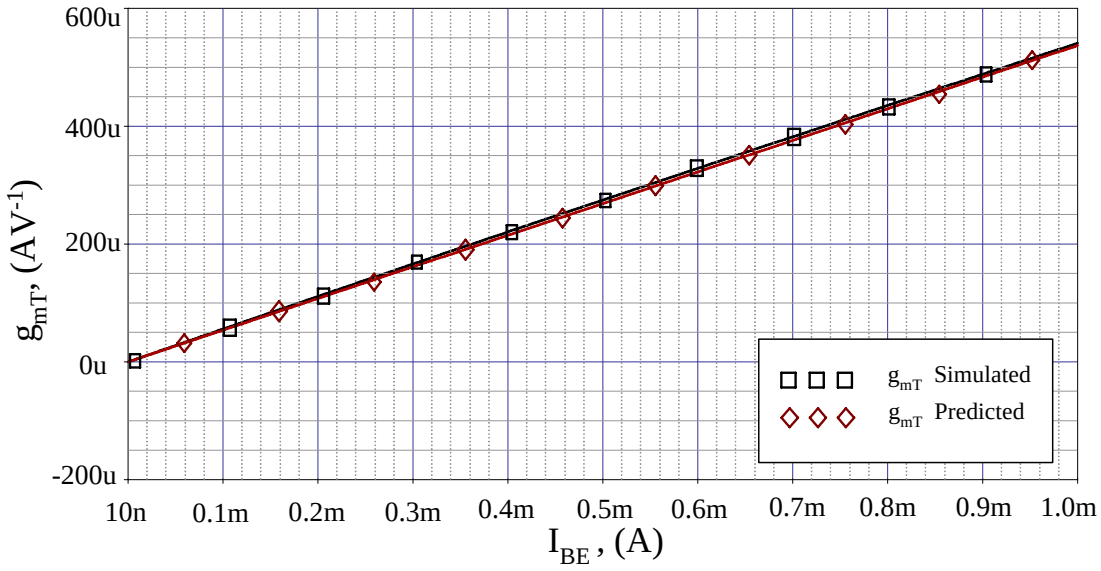

Fig. 4.11 Linear transconductance tunable range

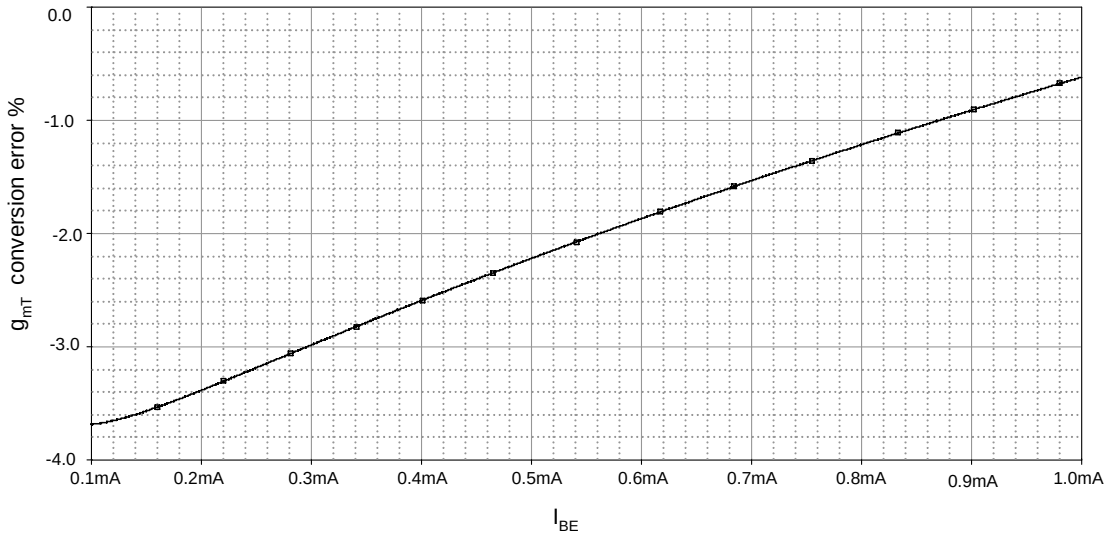

Fig. 4.12 Conversion error of g_{mT} versus I_{BE} of the EOTA

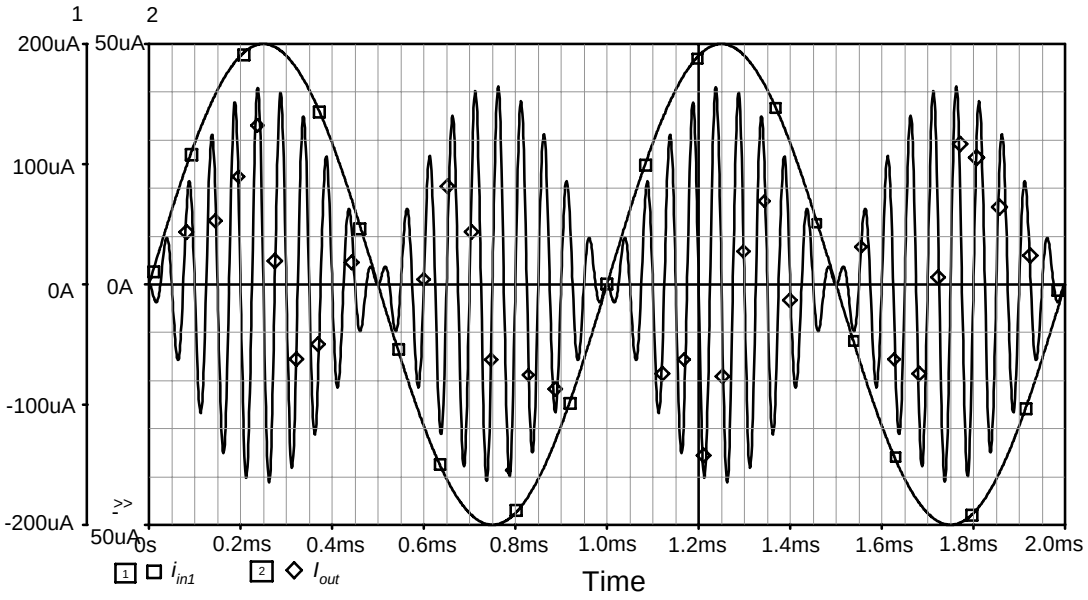

Fig. 4.13 Simulated transient response for the multiplier circuit

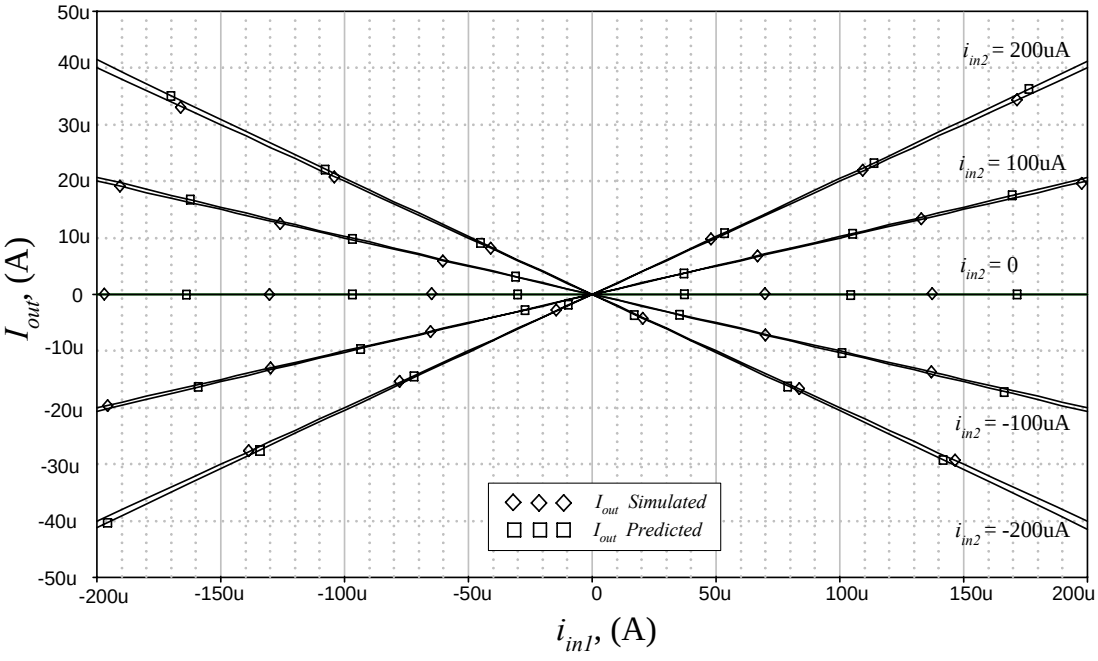

Fig. 4.14 Simulated DC transfer characteristic of the multiplier

Accordingly these limits were agreed very well with the prediction that the of CMOS transistors are operating in saturation region from eqn. (2.45). At the DC bias current I_{BE} = 1mA, in the case of V_{in} = 0.5V, I_{B2}= 880μA, the result shows that the transconductance gain g_{mT}= 5.398×10^{-4} AV^{-1} is achieved. The conversion error from the simulation result is about 0.5%, this results are agree with the conversion error predicted from eqn.(4.17).

To demonstrate that the circuit of Fig. 4.4 can be functioned as current multiplier, two sinusoidal current signals are applied. Fig. 4.13 shows the response for the case of $i_{in1} = 0.2\sin(2\pi1000t)$ mA, $i_{in2} = 0.2\sin(2\pi20000t)$ mA and I_{BE1} = 1mA. This result confirms that the circuit can accurately modulate two different input signal currents. The DC transfer characteristics of the multiplier circuit shown in Fig. 4.14 were observed by setting the bias currents I_{BE1}= I_{BE2}= I_{BE3}= 1mA, and the input current i_{in1} and i_{in2} are varied from -200μA to 200μA with 100μA per step. The transfer characteristic demonstrated that the simulated and calculated data are agreed very well over the input range of ± 190μA with the error of less than 1%. The high frequency characteristic of the multiplier circuit is also studied. The simulated –3dB bandwidth for the case of the input i_{in1} to the output I_{out}, with i_{in1} = 0.5sin(2π10000t) mA, i_{in2}= 500μA and I_{BE1} = 1mA, is about 75 MHz and the simulated –3dB bandwidth of the circuit for the input i_{in2} to the output I_{out}, with i_{in2} = 0.5sin(2π10000t) mA, i_{in1}= 500μA and I_{BE1} = 1mA, is about 71 MHz.

For the linearly voltage-controlled current amplifier in Fig. 4.6, we set I_{BE}= 600μA and I_{B2}=1mA. Fig. 4.15 shows the current transfer characteristic of the proposed voltage controlled current amplifier. This figure shows the plot of the output current i_{out} against the input current i_{in} from -500μA to 500μA for different V_c values; V_c = 0.1V, 0.5V, 1V and 1.5V. The simulation and calculated data are agreed very well, where the conversion error of i_{out} versus i_{in} in the case of V_c =0.5V is plot in Fig. 4.16. For example at V_c = 0.5V, over the ± 500μA input range, error was less than 5%.

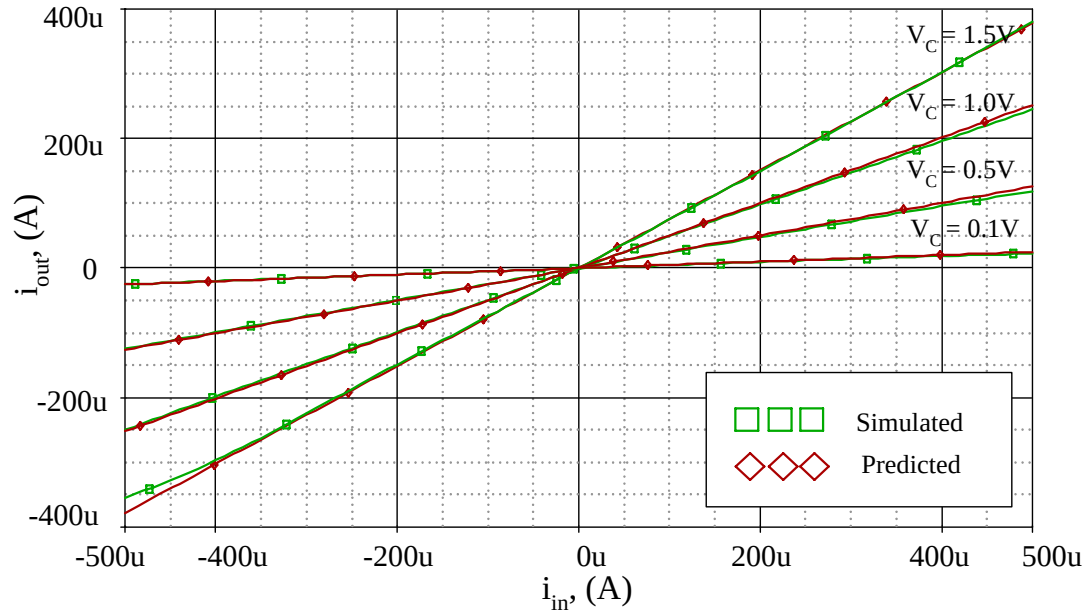

Fig. 4.15 The current transfer characteristic of the voltage controlled current amplifier

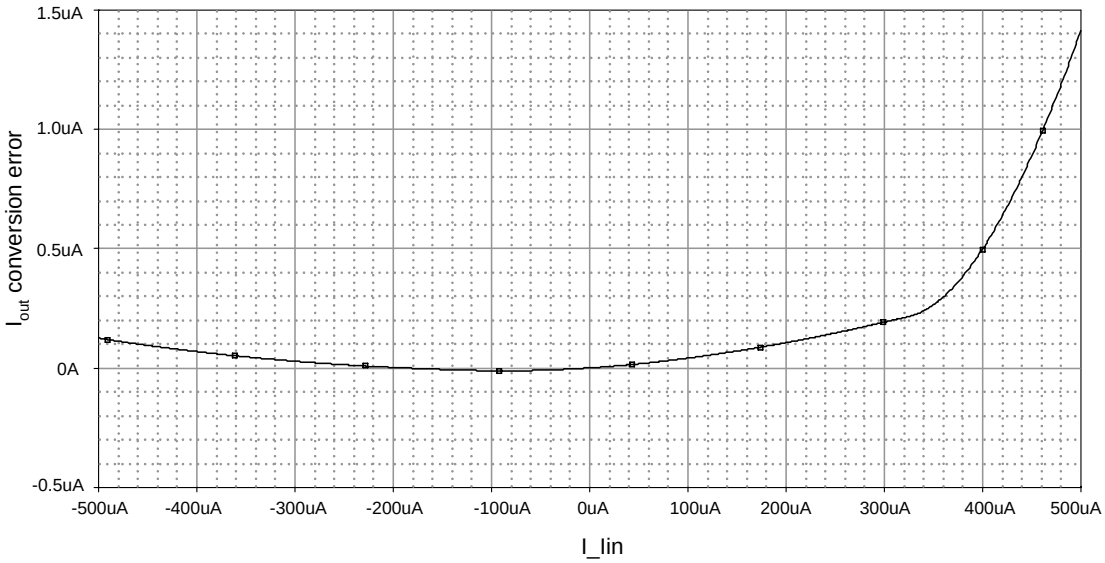

Fig. 4.16 Conversion error of i_{out} versus i_{in} of voltage controlled current amplifier

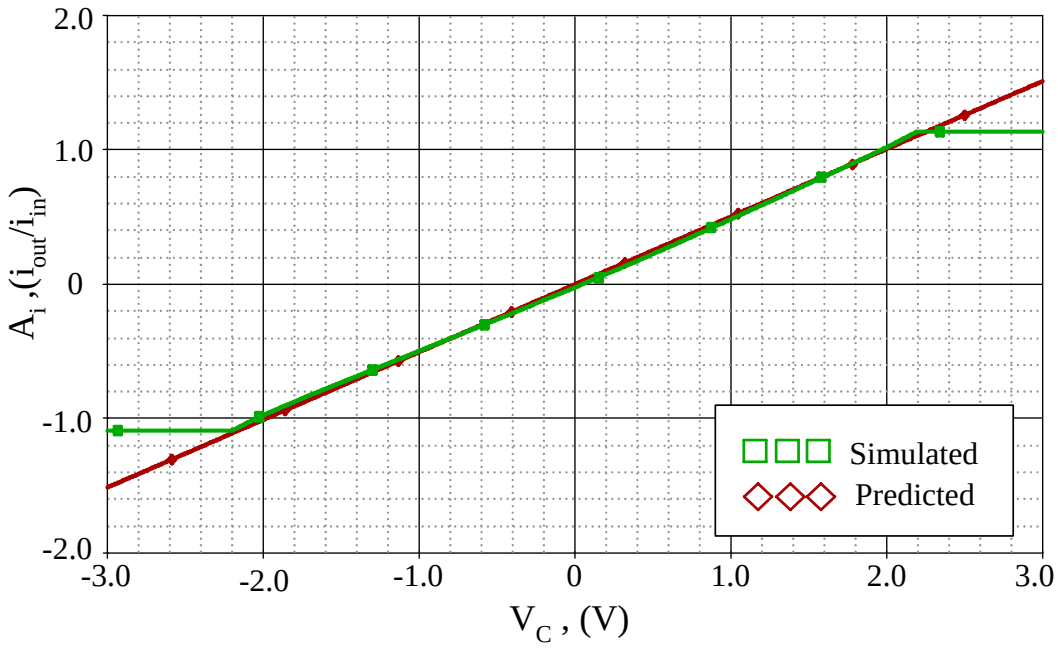

Fig. 4.17 The performance of gain controllability of the voltage controlled current amplifier

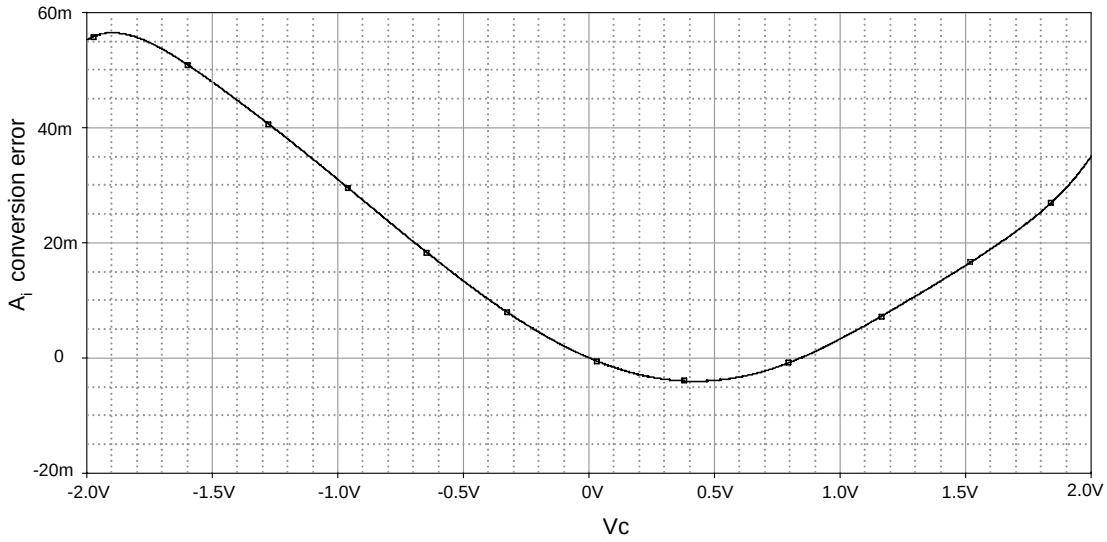

Fig. 4.18 Conversion error of A_i versus V_c of voltage controlled current amplifier

Fig. 4.17 represents the plots of the variation of current gain $A_i = i_{out}/i_{in}$ versus the control voltage V_c in the case of i_{in}=10μA. It is seen that both the results from simulation and calculation are in good agreement, where the conversion error of A_i is plot in Fig. 4.18. The nonlinearity is seen to be less than 5% for the control voltage (V_c) range from -2V to 2V, The control voltage range of the circuit depend on condition in eqn. (2.45) that transistor must be operating in saturation region.

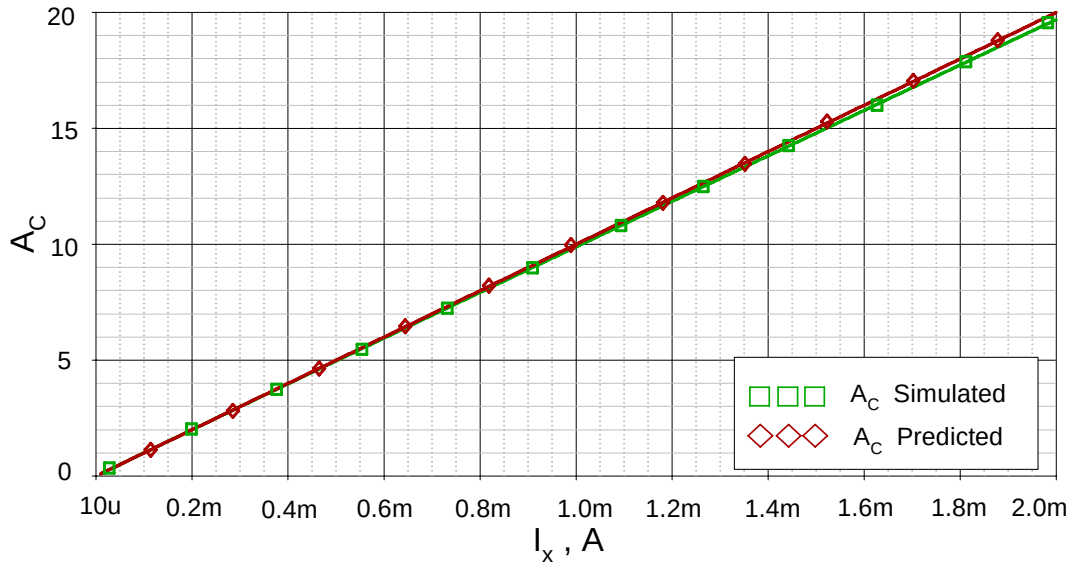

Fig. 4.19 The gain controllability of the linearly current-controlled current amplifier

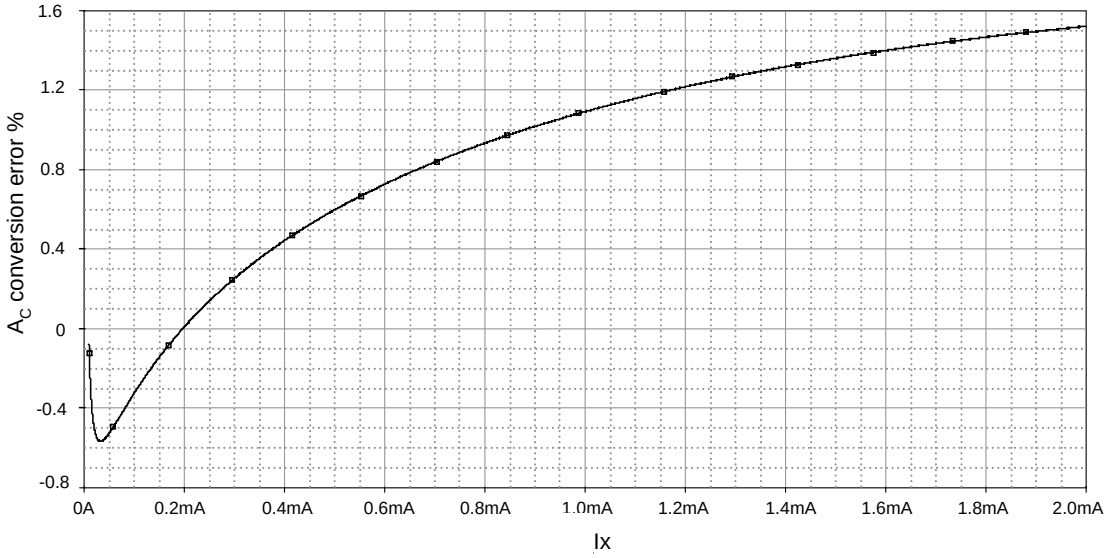

Fig. 4.20 Conversion error of A_c versus I_x of the linearly current-controlled current amplifier

The gain and the controllability of the proposed current-controlled current amplifier in Fig. 4.8 obtained by simulation and calculation are shown in Fig. 4.19, for I_x from 10μA to 2mA where I_y is kept be constant at 100μA. It is seen that both results are in good agreement, where the conversion error of A_c versus I_X is plot in Fig. 4.20. For example, at I_x = 2mA, the conversion error is less than 1.5%. We found that the current gain (A_C) can be electronically and linearly tuned from 0.1 to 20 (3 decade).

Table 4.1 The performance of the proposed linearly controllable transconductances and the propose EOTA

Transconductor	[4.16]	[4.17]	[4.18]	proposed EOTA
Technology	2μm MOSIS	0.8μm CMOS CXQ	5μm CMOS	2μm MOSIS
Controllable g_m	DC voltage	DC voltage	DC voltage	DC current
Controllable range	0.1-1V	1.2-1.4V	NA	10μA-1mA
Transconductance range	98-396μA/V	180-346μA/V	330μA/V	0.54-540μA/V
V_{supply}	5V	1.4V	± 5V	± 3V to ± 5V
V_{in}	-1.4 to 1.4V	± 1V	1.2V	± 1V (I_{BE}=1mA)
Bandwidth	50MHz	420MHz	20MHz	120MHz

This table shows that the proposed EOTA has some advantages over other proposed linearly controllable transconductances in [4.16], [4.17] and [4.18]. The EOTA has wider controllable range and wider transconductance range.

4.5 Conclusion

A design of electronically and linearly tunable CMOS OTA has been proposed. The EOTA circuit composed of three balanced CMOS OTAs which is suitable for implementing in CMOS integrated form. The achieve characteristics of the proposed circuit were similar as the bipolar OTA that the transconductance gain (g_m) can be linearly tuned by the DC bias current. Simulation results have been employed to demonstrate the performances of the proposed EOTA. Moreover to confirm that EOTA can be replacing the bipolar OTA, the current-mode multiplier circuit, and both of current-controlled and voltage controlled current amplifier current amplifier were used to display the performances of the proposed circuit.