CHAPTER 3

CMOS Based True RMS-to-DC Converter

3.1. Introduction

The Root-Mean-Square (RMS) value of arbitrary signal is one of important parameters in electronics measurements, especially for digital multimeters (DMM's). The RMS value is the parameter for measuring the size of signal. As the name suggests; this parameter consists of the square root of the average value of the square of the signal. Moreover, the RMS value is such an important measurement for the following reason: It is the most common way of describing the size of an AC signal. The RMS value is a measure of the energy content in the signal since the RMS value of an AC voltage or signal is defined as being equivalent to that DC voltage or current which has a similar heating effect of the AC signal when applied to an identical resistor. In addition it is useful in some statistical operations; for example with any stationary, zero mean random signal, the RMS value is equal to the standard deviation of the signal.

A true RMS-to-DC converter is a device which converts a signal (DC, AC, AC+DC) for all waveforms to its equivalent DC heating value which proportional to the square root of the average of the input waveform squared. It is an important instrument that used for measuring the average energy content in an electrical signal. This device found useful in the fields of instrumentation, communication and display systems [1]. Automatic gain control and digital multimeters are examples of these applications.

To realize this RMS converter, we have two alternative methods; a comparing and a computing methods.

The comparing method, which is based on a thermal principle or the thermal RMS-to-DC converter [44],[45]. This method is achieved by converting an unknown voltage or current into heat from a known value of resistance. The squaring of the input signal is realized by measuring the temperature of a resistor, which is heated by the Joule heat of the electrical current. The dissipated energy is proportional to the square of the input signal. Integration can be achieved by using the thermal time constant of the circuit or by an extra electronic integration circuit. Most of the thermal converters use a feedback system, which compares the temperature of a dc-driven resistor with the temperature of the resistor driven by the input signal. The temperature can be

measured using a bipolar transistor [46] or a thermopile [47], which can be realized by using extra bulk micromachining steps. The thermal conversion is the simplest method in theory, but however, it is the most difficult and expensive to implement.

The computing method is based on analog signal processing or digital signal processing. Although the analog processing method using translinear property of bipolar circuitry has led to elegant solution [4],[6],[48], however, these converters are difficult to implement in standard CMOS processes. We can determine the RMS value of a wave form electronically with multiplier circuits by using either of the two techniques. One technique is knows as direct computation [Analog Device commercial IC AD737, AD736] which directly computes the square, the mean and square root of the analog value. Using this direct approach, a squarer, a low pass filter, and a square rooter are required according to the definition, resulting in a true rms-to-dc converter applicable to measuring an arbitrary waveform. This direct approach has a limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. The other one technique is indirect or implicit computation [commercial IC AD536A, AD637, MX636], [7],[49]-[51]. This approached uses feedback to perform the square root function implicitly or indirectly. Therefore the scheme requires only a squarer and a low pass filter to measuring an arbitrary waveform. Some advantages of implicit rms computation over other methods are fewer components, greater dynamic range, and generally lower cost.

Several methods to obtain true RMS-to-DC converters amenable to silicon implementation have been proposed [52]. However, in most cases, these converters are implemented by means of BJT transistors [6]. Thus, these techniques are difficult to translate to standard CMOS processes. An attempt to fill this gap is to employ an analog-to-digital converter and to perform digital processing [53],[54] that designed based on $\Delta\Sigma$ computational technique, but the extra circuitry needed leads to a considerable increment of chip area. In [55] another proposal employing continuous time analog processing and standard CMOS process are presented. In such an implementation, the dynamic MOS translinear principle are employed [4],[6]. The RMS to DC converter design based on CMOS technology has been also proposed [56]. The circuit design based on pseudo RMS-to-DC converter concept since it does not give, in the general case, an output proportional to the square root of the average of the input waveform squared.

In this thesis, through the use of a MOS transistor square law characteristic, a design technique for the realization of a true RMS-to-DC converter is proposed. The circuit is suitable

for all input wave forms. The conversion circuit performs the implicit computation scheme, by feedback the root-mean square current to be the circuit bias current. A full-wave rectifier is not required by the proposed realization scheme. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system. The performance of the conversion circuit is studied from PSPICE simulation results and experimental results.

3.2 Exiting RMS-to-DC converters

Many true RMS-to-DC converters have been proposed [2]-[4], [57], most of them are design based on a bipolar integrated circuit technology. Their conversion schemes are mostly performed through the use of full-wave rectifiers and multiplier/divider circuits that employing a log-antilog principle. Due to the bandwidth and the slew-rate of the full-wave rectifiers, the useful frequency ranges of these converters are limited to less than 5 MHz. Commercial monolithic IC's for the RMS-to-DC converter are available. The popular examples from Analog Devices are the AD536/536AJ, AD636J, AD336J, AD737J, AD736 and AD737, from National Semiconductor is LH0097 and from Burr-Brown is 4340/4341. Most of these IC's are similarly built up from two main part: namely, a full-wave rectifier circuit and a multiplier/divider circuit employing a log-antilog principle. However, the bandwidth of the full-wave rectifiers and the high frequency performance of the IC's is also limited by their full-wave rectifier part.

New design techniques based on bipolar dynamic translinear circuits have been proposed to implement true RMS-to-DC converters [4],[6],[48]. Unfortunately, only circuit descriptions are outlined, but the characteristics of the RMS-to-DC conversion circuits have not been reported. In addition, their circuits are operated in only one quadrant and also required full-wave rectifiers. Recently, a new design technique for RMS-to-DC converter that realizes around a dual translinear-base squarer circuit, where the input current can be a two-quadrant current, is proposed [7]. The circuit exhibits a wide bandwidth because the full-wave rectifier is not required by this conversion scheme. However, the implementation scheme is rather complicate and suitable for implementing only in bipolar technology.

3.3 The proposed CMOS based true RMS-to-DC converter

In this section, through the use of a MOS transistor square law characteristic, a realization of a wide bandwidth current-mode CMOS true rms-to-dc converter is proposed. The conversion circuit performs the implicit computation scheme, by feedback the root-mean square current to be the circuit bias current. The square root function is obtained, while a square root circuit is not required by the proposed realization scheme. The circuit structure is simple since it requires only a squarer and a low-pass filter. The conversion circuit consumes very low power, due to the bias current of the circuit is provided by the root-mean-square current I_{RMS}.

Usually, for the RMS-to-DC converter through the implicit computation method, the circuit implements the root-mean-square function by performing two non-linear processes: squaring and square rooting. However, in this implementation, the squaring is the core of the circuit and the square rooting function is achieved through feedback. The proposed RMS-to-DC converter can be represented by the block diagram as shown in Fig. 3.1. It composes of the squarer/divider block, I_{in}^2 / I_b, in combination with the current mirrors CM_4 and CM_5 and the low-pass filter *LPF* (CM_3 and C_{AV}).

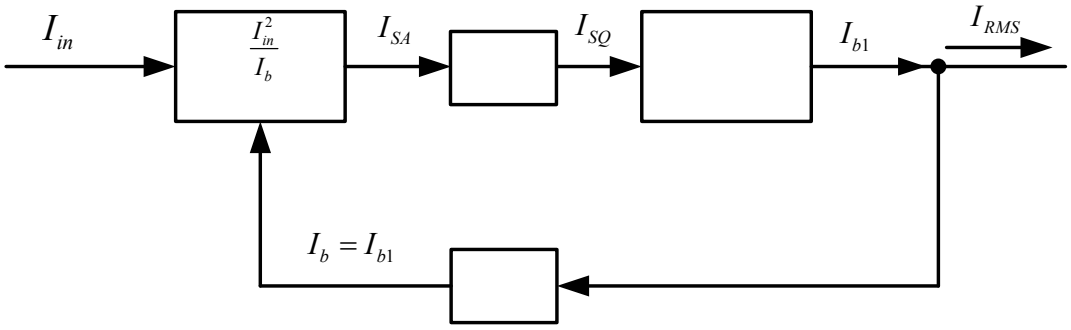


Fig. 3.1 Block diagram representation of the proposed true RMS-to-DC converter.

Noting that the conversion is performed through the feedback system, the instability will occur when the loop gain magnitude of the circuit exceeds one. However the loop gain magnitude of the proposed true RMS-to-DC converter is always less than one since the gain magnitude of CM_4 and CM_5 are unity and the gain magnitude of the LPF is always below one ($\omega >> 1/\tau$) for keeping the LPF work as ideal integrator. Therefore, the proposed RMS-to-DC converter is always stable.

3.3.1 Circuit descriptions of the true RMS-to-DC converter

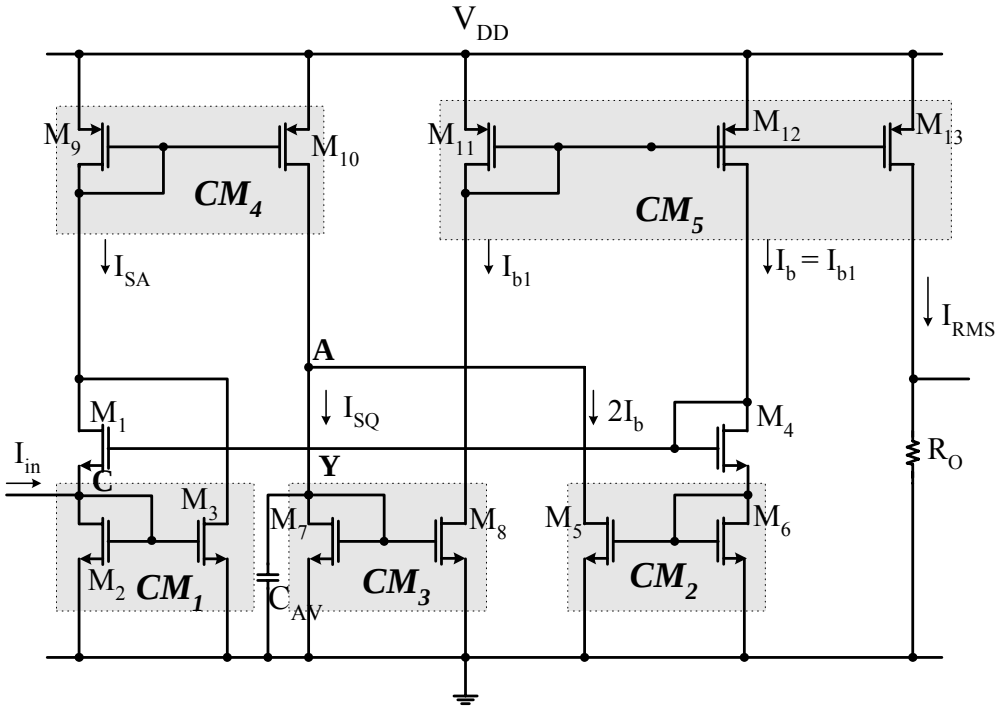


Fig. 3.2 The proposed true RMS-to-DC converter.

From Fig. 3.1 the schematic diagram of the proposed true RMS-to-DC converter can be represented as Fig. 3.2. In this figure, transistor M_1 to M_6 are formed as the current squaring circuit in combination with four current mirrors, CM_2 through CM_5, where the input signal current I_{in} is injected into point *C*. From routine circuit analysis, the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1}+I_{D2}$ can be given by [analyzed in section 2.2.1]

$$I_{SA} = \frac{I_{in}^2}{8I_b} + 2I_b \tag{3.1}$$

We can see that I_{SA} is the squaring of the input signal I_{in} plus the DC current $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit. Therefore in this proposed true RMS - to -DC converter is constructed such that the drain current of the

transistor M_5 of the current mirror CM_2 sources the current $2I_b$ from I_{SA}. Then from the eqn.(3.1), the current I_{SQ} can be expressed as

$$I_{SQ} = \frac{I_{in}^2}{8I_b} \tag{3.2}$$

In the figure, the current I_{SQ} passes through the averaging circuit or the first-order current mode low-pass filter (LPF) or the integrator circuit, which is consisting of the current mirror CM_3 (M_7 and M_8) and the grounded capacitor C_{AV} parallel connected to the mirror input [58]. The output current of the filter I_{b1} can be written as

$$I_{b1} \cong \frac{1}{8I_b\tau}\int I_{in}^2 dt \qquad , \quad s\tau >> 1 \tag{3.3}$$

where $\tau = C_{AV}/g_{m7}$ is the time constant of the filter and g_{m7} is the transconductance of the transistor M_7. Due to the unity gain current mirrors CM_3 (M_7 and M_8) and CM_5 (M_{11} and M_{12}), the bias current I_b is derived by the current I_{b1} such that

$$I_b = I_{b1} \tag{3.4}$$

At the output, since we set the transistor channel widths of the current mirror CM_5 as $W_{13} = \sqrt{8}\, W_{11}$, it means the output current

$$I_{RMS} = \sqrt{8} I_b \tag{3.5}$$

From eqn. (3.3), since $I_b = I_{b1}$, by solving for I_b, we can write

$$I_b = \frac{1}{\sqrt{8}}\sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \tag{3.6}$$

Then from eqns. (3.5) and (3.6), the current I_{RMS} can be given as

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 dt} \tag{3.7}$$

We can see that the output current I_{RMS} is in the form of the root-mean-square value. It should be noted from the eqns. (3.2)-(3.7) that the square root function is achieved by the feedback of the current I_{b1} to be the bias current I_b of the circuit.

In order that the proposed RMS-to-DC converter gives a good performance for the required frequency range, the value of the capacitor C_{AV} must be chosen such that [55]

$$C_{AV} >> g_{m7(MAX)} / 4\pi f_{(MIN)} \tag{3.8}$$

where $f_{(MIN)}$ is the lower end of the frequency range of interest and

$$g_{m7(MAX)} = \sqrt{2K_p I_{SQ} W_7 / L_7} \tag{3.9}$$

W_7 is the channel width and L_7 is the channel length of the transistor M_7. From eqn. (3.2), the $g_{m7(MAX)}$ can be expressed as

$$g_{m7(MAX)} = \sqrt{2K_p I_M^2 W_7 / 8 I_b L_7} \tag{3.10}$$

where I_M is the peak amplitude of the input signal I_{in} and I_b is the circuit bias current. For example, for $K_P = 25.035\text{x}10^{-6}\ A/V^2$ and $W_7/L_7 = 20$, then $g_{m7(MAX)}$ can be given by

$$g_{m7(MAX)} = 0.0316\sqrt{\left(I_M^2 / 8 I_b\right)} \tag{3.11}$$

In this case, C_{AV} must be chosen such that

$$C_{AV} >> (8.891\times 10^{-4}) I_M / \sqrt{I_b} f_{(MIN)} \tag{3.12}$$

It should be noted from (3.12) that the value of C_{AV} chosen is much depend on the ripple error that can be tolerate at the output. As a rule of thumb, the value of C_{AV} should exceed the right-hand term of eqn. (3.12) by the inverse of the fractional ripple error. For instance, for a 1 percent ripple

error, C_{AV} should be about 1/0.01 or 100 times as large as the right-hand term. For example, if a sinusoidal input signal with I_M = 1 mA, $f_{(MIN)}$ = 100 Hz, and the ripple error of 5 percent, then the averaging capacitance of $C_{AV} = 10\mu$F must be chosen.

The settling time, or time for the RMS converter to settle to within a given percent of the charge in RMS level, is set by the averaging time constant ($\tau = RC$). In this thesis, the settling time of the proposed RMS-to-DC converter is varies with the time constant of the first order low-pass filter, RC time constant ($\tau = C_{AV} / g_{m7}$), where g_{m7} is the function of I_{in} as expressed in eqn. (3.11). Due to the averaging capacitor connected across in the input part of the NMOS current mirror that form as the first order low-pass filter, the averaging time constant will increase as the input signal is reduced and vice versa. In addition, the settling time also varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased as shown in the simulation results section.

3.3.2 Circuit Performance

The ideal circuit performance that has been discussed in section 3.3.1 so far is based on the assumptions that the current mirrors have unity gain, transistors are perfectly matched, and each transistor is operated in its saturated regions and obeys a square law model. However, in practical realization, the finite values of transistor g_m and g_d and the transistor mismatched will contribute to deviate from the ideal performance. In the following, the transistor equivalent circuit and a small signal analysis will be used to study the performances of the conversion circuit of Fig.3.2.

3.3.2.1 Operating range

As we have been pointed out that the proposed true RMS-to-dc converter is based on the square law characteristic of MOS transistors biased in the saturation region. The square-law behavior for the current–voltage relationship of the MOS transistor in saturation is assumed as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ \ V_{GS} > V_T \\ 0 & , \ for \ \ V_{GS} \le V_T \end{cases} \qquad (3.13)$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and the threshold voltages, respectively.

Because of the input signal of the proposed true RMS-to-DC converter in Fig. 3.2 is a current signal. In order to remain a proper operation, the input current is restricted to the range

$$\left|I_{in}\right| < K\left(V_1 - 2V_T\right)^2 \tag{3.14}$$

$$V_1 = V_{DD} - V_{DS12(sat)} \tag{3.15}$$

Replace V_1 from (3.15) in (3.14), eqn. (3.14) can be rewritten as

$$\left|I_{in}\right| < K\left(V_{DD} - V_{DS12(sat)} - 2V_T\right)^2 \tag{3.16}$$

or, if biased with the relation of the DC bias current (I_b) which is fed back by the RMS current from the output. We will obtain

$$\left|I_{in}\right| < 4I_b \tag{3.17}$$

Eqns. (3.16) and (3.17) can be shown that the limitation of the input current is depend on the supply voltage and the dc bias current which should not over $4I_b$.

Due to the I_{RMS} is feedback to be the bias current I_b, or $I_b = I_{RMS}/\sqrt{8}$, of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions. Table 3.1 shows the output currents in RMS values (I_{RMS}) and the DC bias currents (I_b) of the current signal input (I_{in}) for 3 difference input waveforms. There are square waveform, sine waveform and triangular waveform, respectively, where the I_{RMS} is equal to the root mean square value of the input signal, $I_{RMS} = \sqrt{\frac{1}{\tau}\int I_{in}^2 dt}$, and I_b is equal to the average of the input signal $I_b = I_{b1} = \frac{1}{8I_b\tau}\int I_{in}^2 dt$, or $I_b = I_{RMS}/\sqrt{8}$. In addition, this table shows the saturation condition of transistors when I_b is in the term of I_{in} for its input waveform.

Table 3.1 The relation between the bias current (I_b) and the input current (I_{in})

Input waveform	I_{in}	I_{RMS}	$I_b = I_{RMS}/\sqrt{8}$	**Saturation condition*** $I_{in} \le 4I_b$	**Note**
Square	$I_{in(peak)}$	$I_{in(peak)}$	$\frac{1}{\sqrt{8}} \cdot I_{in(peak)}$	$I_{in(peak)} \le 1.414 I_{in(peak)}$ $(I_{in} < 4I_b)$	Under the saturation condition
Sine	$I_{in(peak)}$	$\frac{1}{\sqrt{2}} \cdot I_{in(peak)}$	$\frac{1}{4} \cdot I_{in(peak)}$	$I_{in(peak)} \le I_{in(peak)}$ $(I_{in} = 4I_b)$	Under the saturation condition
Triangular	$I_{in(peak)}$	$\frac{1}{\sqrt{3}} \cdot I_{in(peak)}$	$\frac{1}{\sqrt{24}} \cdot I_{in(peak)}$	$I_{in(peak)} \le 0.82 I_{in(peak)}$ $(I_{in} > 4I_b)$	Out of the saturation condition

*The circuit is somewhat limited by the saturation condition $I_{in} \le 4I_b$

Note:

- *Under the saturation condition* is defined as MOS transistors are biased in the saturation region.

- *Out of the saturation condition* is defined as MOS transistors can not biased in the saturation region.

From table 3.1 we found that the bias current (I_b) and the signal input current (I_{in}) of the sine wave and square wave are under the saturation condition, $I_{in} \le 4I_b$, except in the case of the input signal is triangular wave. From this results, we found that the accuracy of square wave input signal and sine wave input signal will be better than the triangular wave input signal.

3.3.2.2 Conversion Errors

From the block diagram in Fig. 3.1, the accuracy of the RMS-to-DC conversion depends on the imperfection of the squaring and the current mirrors circuits. From the eqns. (3.2)-(3.7), we can notice that the implicit computation is achieved by the feedback of the current I_{RMS} to the I_{in}^2 / I_b block by setting $I_b = I_{RMS}/\sqrt{8}$, where I_b is the transistor bias current. Then the accuracy

of the RMS-to-DC conversion depends on the imperfection of the squaring and the current mirrors circuits. In addition, due to the output current (I_{RMS}) should designed by $I_{RMS}=\sqrt{8}\,I_b$ by setting channel width of transistor M_{13} is $W_{13}=\sqrt{8}\,W_{11}$, however, in practice the value of $\sqrt{8}$ can not exactly setting, therefore we approximately given $W_{13}=2.83W_{11}$. From this result the output current will have some error from the approximation of $\sqrt{8}\cong 2.83$ about 0.056%.

The operating range of the squaring part can be studied through a the large signal analysis, by considering the MOS transistors operating in saturation. Since the output current of the squaring circuit (I_{SA}) is the sum of the drain current of transistors M_1 and M_3 , $I_{D1}+I_{D3}$, where I_{D3} is mirrored from the current mirror CM_1, and if the gain of the current mirror CM_1 is unity, I_{D3} can be expressed in the function of I_{D2} as

$$I_{D3}=\frac{(W/L)_3}{(W/L)_2}\left(\frac{V_{GS3}-V_{T3}}{V_{GS2}-V_{T2}}\right)^2\cdot\frac{1+\lambda V_{DS3}}{1+\lambda V_{DS2}}\cdot\frac{\mu_{n3}C_{ox3}}{\mu_{n2}C_{ox2}}I_{D2} \quad (3.19)$$

From this equation, we found that the mismatched of the channel width W, channel length L, mobility μ_n, and oxide thickness t_{ox} of the current mirror can produce the gain error. Also, the effect from channel length modulation and mismatched of the threshold voltage. This gain error of the current mirror will effect to the accuracy of the output current of the squaring circuit. This error can be reduced by using large values of transistor length L_3, but especially by enforcing equal V_{DS} value of transistors M_2 and M_3.

If the effect of channel-length modulation can be neglected ($\lambda=0$), assume the process parameters such as V_T, μ_n, C_{ox}, of MOS transistor are matched and $V_{DS2}\cong V_{DS1}$. By copying of I_{D2} via transistor M_3 and adding it to current I_{D1} , the sum current $I_{D1}+I_{D3}$ is available as output current I_{SA} of squaring part [Appendix A]

$$I_{SA}=\frac{1}{2}\frac{\mu_n C_{ox}W}{2L}\left(V_1-2V_T\right)^2+\frac{I_{in}^2}{2\frac{\mu_n C_{ox}W}{2L}\left(V_1-2V_T\right)^2} \quad (3.20)$$

In order to remain a proper operation from Appendix A.11, the input current is restrict to the range $|I_{in}|<K(V_1-2V_T)^2$.

The eqn (3.20) describes a current squaring function. Using the bias circuit, formed by transistors M_4 and M_6 , to combination with the current squaring circuit in Fig. A1 which shown in Fig. 2.8, a simpler expression is obtained

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{3.21}$$

Biasing with a current has the additional advantage of making the transfer function (in first-order approximation) independent of process parameters and operating temperature.

The conversion of the input signal current i_{in} to the current i_{SA} from the squaring part can be approximately expressed as [Appendix B]

$$\alpha = \frac{i_{SA}}{i_{in}} = \frac{1}{1 + \dfrac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}}} \tag{3.22}$$

where g_{di} and g_{mi} denote the drain conductance and the conductance of the transistor M_i, respectively. The input current I_{in} will accurately convert to i_{SA} if $\alpha \approx 1$. The percentage conversion error of the squaring circuit can be written as

$$\frac{\delta\alpha}{\alpha} = \frac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}} \times 100\% \tag{3.23}$$

For example, if $g_{m1} = 4.80 \times 10^{-4}$ AV^{-1}, $g_{m2} = 4.44 \times 10^{-4}$ AV^{-1}, $g_{m3} = 5.39 \times 10^{-4}$ AV^{-1} and $g_{d1} = 3.26 \times 10^{-6}$ AV^{-1}, the resulting conversion error is equal to 0.322%. It should be noted from eqn. (3.23) that the conversion error depends on drain conductance (g_d) of the transistors, where $g_d \approx \lambda I_D$ and λ is the channel length modulation parameter. We can further reduce this error by decreasing the transistor drain current I_D. In addition, if long channel transistors are used, we can neglect channel length modulation effect [59]

The current reflection errors ε_{pos} and ε_{neg} associated with the positive and negative current mirrors, respectively, can be approximately given by [60]

$$\varepsilon_{pos} = \left(\frac{I_{out}}{I_{in}}\right)_{CMpos} - 1 = \left(\frac{L_7 W_8}{W_7 L_8}\right)_{NMOS} \cdot \left(\frac{1+\lambda V_{DS8}}{1+\lambda V_{DS7}}\right)_{NMOS} - 1 \quad (3.24a)$$

$$\varepsilon_{neg} = \left(\frac{I_{out}}{I_{in}}\right)_{CMneg} - 1 = \left(\frac{L_9 W_{10}}{W_9 L_{10}}\right)_{PMOS} \cdot \left(\frac{1+\lambda V_{DS10}}{1+\lambda V_{DS9}}\right)_{PMOS} - 1 \quad (3.24b)$$

where V_{DS} is drain-source voltage. For example, let $W_7 = W_8 = W_9 = W_{10}$ =100 μ m, $L_7 = L_8 = L_9 = L_{10}$ =5 μ m, λ = 0.01 volts^{-1}, V_{DS7}= 2.72 volts, V_{DS8}= 4.94 volts, V_{DS9}= -2.76 volts, and V_{DS10}= -4.99 volts, these errors (ε_{pos} and ε_{neg}) is approximately less than 2.17 %. Notice from the eqns. (3.24a) and (3.24b) that the accuracy of the current mirror also depends on the channel length modulation. In order to reduce the influence of the channel length modulation, cascode current mirrors should be used.

3.3.2.3 Frequency response

The frequency response of an RMS-to-DC converter provides a measure of how well the circuit can measure the RMS of sine wave input signals of varying frequencies. This frequency response is different from that used when describing filters or amplifiers which are essentially linear devices. The RMS-to-DC converter is a non-linear device with an AC input and a DC output and so has a frequency response which is defined as the percent error on the output against the frequency of the input sine wave. This frequency range is much greater than 1/τ where τ is the time constant of the smoothing circuit being used. As the frequency of the input signal is reduced, the smoothing filter is not able to average effectively and a greater ripple content appears on the output together with a DC output error.

So, for low input frequencies, about 10Hz, a compromise needs to be made between having a large time constant for smoothing which provides a slow response time with good accuracy or having a small time constant which provides a faster response time but poorer accuracy. The high frequency response is limited by the finite bandwidth of the circuit structure, which for this proposed true RMS-to-DC converter circuit, it is limited by the current mirror, CM_5. Many commercial ICs that employ by using op amp to construct the full wave rectifier, therefore, the high frequency response is dependent on the finite bandwidth and slew rate of the input full wave rectifier of the circuit.

To verify the high frequency response, from the block diagram of Fig. 3.2, the transfer function of the proposed RMS-to-DC converter circuit can be approximately given by

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{I_{SA}(s)}{I_{in}(s)} \cdot \frac{I_{SQ}(s)}{I_{SA}(s)} \cdot \frac{I_{b1}(s)}{I_{SQ}(s)} \cdot \frac{I_{RMS}(s)}{I_{b1}(s)} \tag{3.25}$$

By a small signal analysis of the Fig.3.2, the transfer function of the circuit can be approximated as [Appendix C]

$$\frac{I_{RMS}(s)}{I_{in}(s)} = \frac{(g_{m3}-g_{m1})/(g_{m1}+g_{m2})}{\left(1+s\frac{C_1+C_2+C_3}{g_{m1}+g_{m2}}\right)} \cdot \frac{g_{m10}/g_{m9}}{\left(1+s\frac{C_9+C_{10}}{g_{m9}}\right)} \cdot \frac{g_{m8}/g_{m7}}{\left(1+s\frac{C_7+C_8}{g_{m7}}\right)} \cdot \frac{g_{m13}/g_{m11}}{\left(1+s\frac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \tag{3.26}$$

Let p_1 denotes the pole of the squaring circuit, p_2 is the pole of the current mirror CM4, p_3 is the pole of the lowpass filter, and p_4 is the pole of the current mirror CM5. Then from eqn. (3.26), the poles p_1, p_2, p_3 and p_4 can be respectively expressed as

$$p_1 = -\frac{g_{m1}+g_{m2}}{C_1+C_2+C_3} \tag{3.27}$$

$$p_2 = -\frac{g_{m9}}{C_9+C_{10}} \tag{3.28}$$

$$p_3 = -\frac{g_{m7}}{C_7+C_8} \tag{3.29}$$

$$p_4 = -\frac{g_{m11}}{C_{11}+C_{12}+C_{13}} \tag{3.30}$$

If I_{in} = 1mA, g_{m1}= 4.80×10^{-4} AV^{-1}, g_{m2}= 4.44×10^{-4} AV^{-1}, g_{m9} = 3.31×10^{-4} AV^{-1}, g_{m7}= 4.27×10^{-4} AV^{-1}, g_{m11}= 3.31×10^{-4} AV^{-1}, $C_1=C_2=C_3=C_7=C_8$= 1.21×10^{-13}F, $C_9=C_{10}=C_{11}=C_{12}$= 1.15×10^{-13}F, and C_{13} = 3.26×10^{-13}F, where $C_i = Cgs_i$ and Cgs_i is the gate-to-source capacitance of transistor Mi. Then the cut-off frequencies of the poles p_1, p_2, p_3 and p_4 are approximately located at 405MHz, 229MHz, 281MHz and 95MHz, respectively. We can see that the high frequency limitation is due

to the pole p_4 that associated with the PMOS current mirror (CM5). Then the cut-off frequency of the RMS-to-DC converter can be given by

$$f_{-3dB} = \frac{\left(g_{m11}\right)}{2\pi\left(C_{11}+C_{12}+C_{13}\right)} \tag{3.31}$$

It should be noted that g_{m1}, g_{m2}, g_{m7}, g_{m9} and g_{m11} are varied in direct proportion to the input current I_{in}, since $g_m = \sqrt{2K_p\left(W/L\right)I_D}$ and $I_D = I_{RMS}/\sqrt{8} \cong 0.707 I_{in(peak)}$. Therefore, the cut-off frequency of the RMS-to-DC converter can be increased if I_{in} increase, and vice versa. For example, using the same data above, for I_{in}= 1mA$_{(peak)}$ the cut-off frequency of the RMS-to-DC converter circuit is about 95MHz and for I_{in}=500μA$_{(peak)}$ the cut-off frequency of the RMS-to-DC converter circuit is about 66MHz.

3.3.2.4 DC and ripple errors

In practice, apart from the current I_{RMS}, there are also a low-frequency ripple and a dc error that presented at the output port of the circuit, which depend on the value of the capacitor C_{AV} and the frequency of the input current I_{in}. These errors can be computed by expressing the relationship of the currents I_{RMS} and I_{in} in the form of transfer function, where the current I_{in} is an input sine wave of the form $I_{in} = \sqrt{2} I_{RMS}\cos(\omega t)$. Using a simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or f >1/τ), the output ripple e_{ripple} and the dc error e_{odc} can be expressed in term I_{RMS} of as [65] , [66] ,[Appendix D]

$$e_{ripple} = \frac{I_{RMS}\cos 2\omega t}{2\sqrt{1+4\omega^2\tau^2}} \tag{3.32}$$

and

$$e_{odc} = \frac{I_{RMS}}{16\left(1+4\omega^2\tau^2\right)} \tag{3.33}$$

where only the ripple that due to the second-harmonic term is expressed. The ripple error in the output can be reduced in many applications with a simple low-pass filter. Eqns. (3.32) and (3.33)

showing that the ripple error e_{ripple} and dc error e_{odc} decrease with increasing AC input frequency.

Clearly, the ripple and DC error can be reduced by increasing the time constant of the LPF, however this will slow down the response of the circuit.

3.4 Simulation and Experimental results

The performance of the proposed true RMS-to-DC converter has been studied through simulation and experimental results. The simulation has been carried out by employing PSPICE analogue simulation program, using the CMOS CD4007 transistor parameters that were extracted by the use of the method in [61], [62]. The transistor dimensions are listed in the Table 3.2.

Table 3.2 The aspect ratios of the transistors in Fig.3.2.

Transistor	W(μm)	L(μm)
M1,M2,M3,M4,M6,M7,M8	100	5
M9,M10,M11,M12	100	5
M5	200	5
M13	283	5

For the input current (I_{in}) equal to zero, all MOS transistors are cut-off and I_{out} is also zero. This statement can be confirmed through simulation result, where in the case of V_{dd}= 5V the circuit has the supply current (I_{supply}) of about 100pA, which is near to zero. Fig. 3.3 shows the operation of the true RMS-to-DC converter of Fig.3.2 for sine wave input with $I_{in(peak)}$=100μA and f =1kHz. Where the current $I_{D(M9)}$ is the output current from the squaring circuit, $I_{D(M11)}$ is the output current from the integrator (LPF) and $I_{D(M13)}$ is the I_{RMS}. When an input signal is applied from time 0s to 5ms, the circuit is conducted only in the half cycle, where we can see that the $I_{D(M9)}$ is the form of rectified waveform. After that due to the feedback loop and the averaging circuit (or LPF), time 5ms to 10ms, gradually developed and supply to be the bias current I_{b1} (or $I_{D(M11)}$) of the circuit. For the steady state the squaring circuit can properly operate as a squarer

function. Therefore the circuit can function as Root-Mean-Square. Since the dc bias current of the true RMS-to-DC converter is zero and conducts only when the input signal is present, this circuit is operated as a Class B circuit.

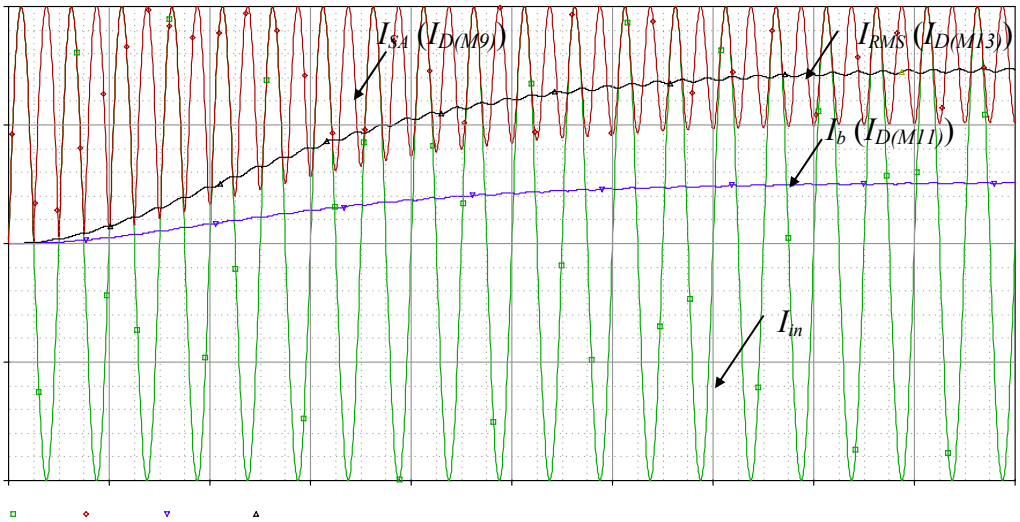


Fig. 3.3 The operation of the proposed true RMS-to-DC converter

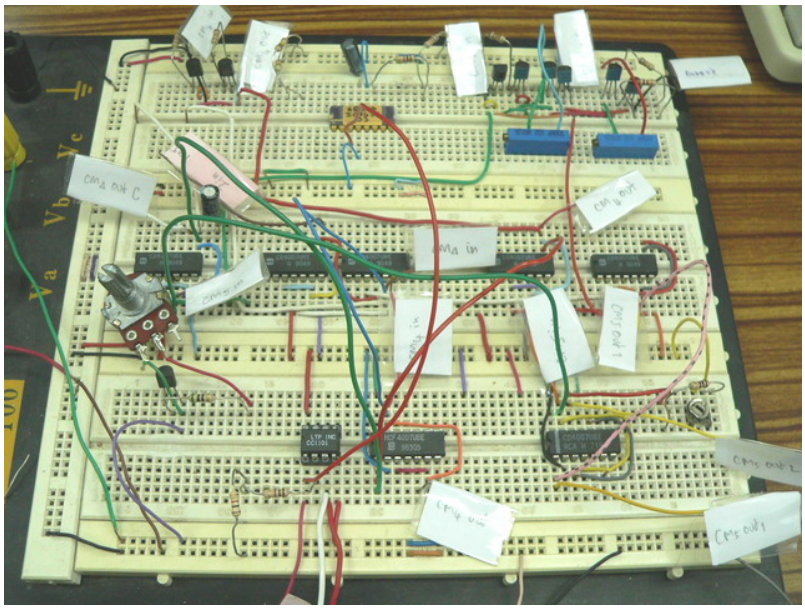
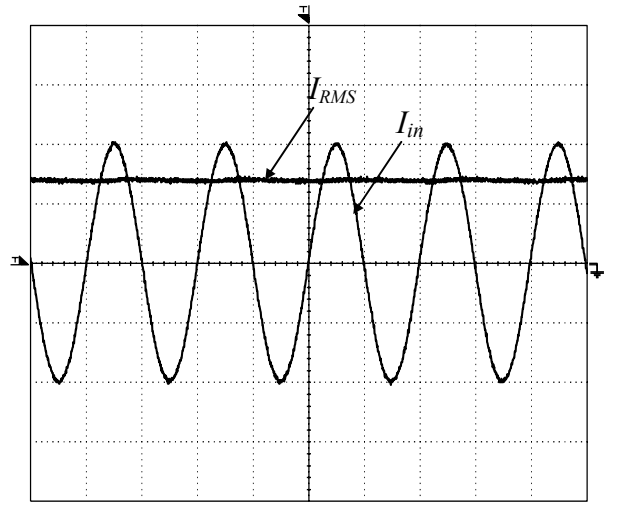


Fig. 3.4 The experiment of the RMS-to-DC converter on a prototype board

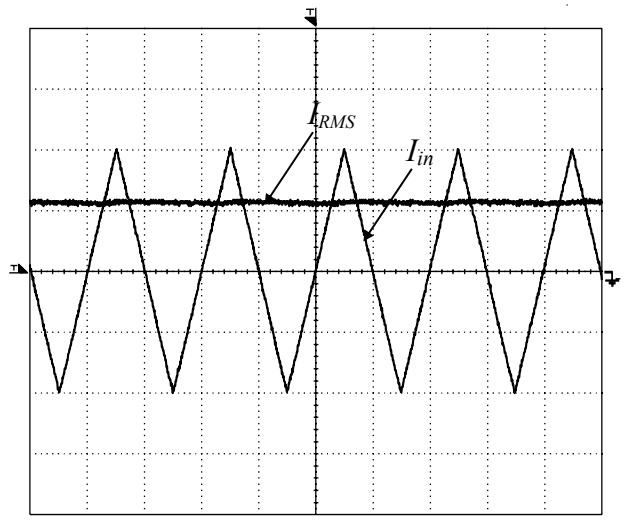
0A

In order to test the performance of the circuit, the true rms-to-dc converter of the Fig.3.2 was also constructed on prototype board as shown in Fig. 3.4. All MOS device used was in the form of complementary MOS pair (CD4007). The transistors that required close matching, especially M_1, M_2 and M_3 and the current mirrors were contained in the same array package. The supply voltage was set to V_{dd} =15V. The capacitor C_{AV} is 10 μF for f_{MIN} = 100Hz. Due to the proposed RMS-to-DC converter operates in current mode, a commercially available current conveyor CCII01 [63] was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor R_{in}=1kΩ is connected at ports X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of I_{in} = $1mA_{(peak)}$, the input voltage equal to 1V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1kΩ was connected at the output of the RMS-to-DC converter and the voltage across the resistor R_o is measured instead.

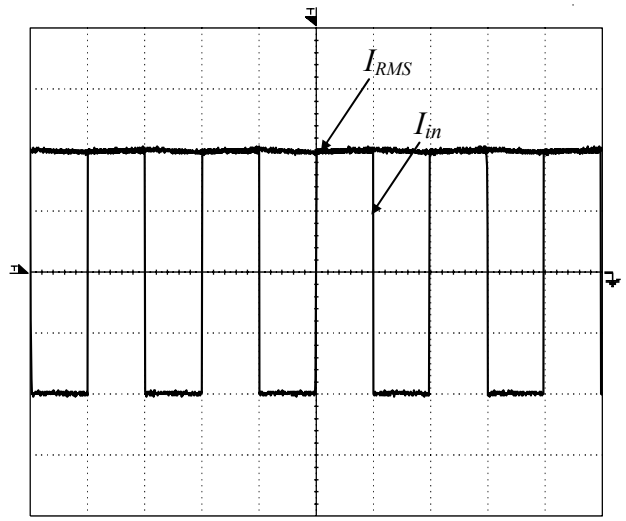
The experimental results in Fig. 3.5(a), 3.5(b) and 3.5(c) show the I_{RMS} for the input signals in the form of sinusoidal, triangular and square wave waveforms, respectively, with the peak amplitude of 1mA and with the frequency of 1 kHz. With the error of less than 10μA, the I_{RMS} signal with the amplitudes close to 0.7mA, 0.5mA, and 1mA, respectively, were achieved. These results demonstrated that the circuit can convert the AC signals into the corresponding DC signals with accurate rms values. To demonstrate that the circuit can operate in a wide frequency range, Fig.3.6(a), 3.6(b) and 3.6(c) show the measured I_{RMS} for the cases of the sinusoidal input signal with the frequencies of f = 500Hz, 5kHz and 5MHz, respectively, and with the peak amplitude of 1mA. The results show that the I_{RMS} signals with the amplitude of about 0.7mA are achieved. The dc errors from the simulation results are about 11%, 0.2% and 0.1%, respectively. We found that this results were agree with the dc error predicted from eqn.(3.33), where the dc error decrease with increasing AC input frequency ($\omega >> 1/\tau$).



(a)

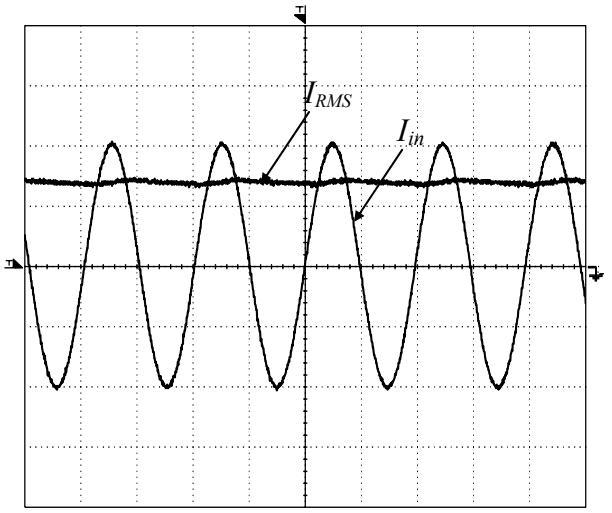


(b)

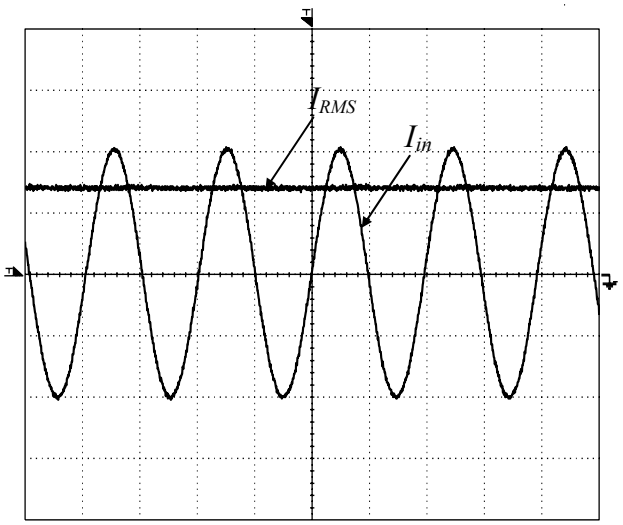


(c)

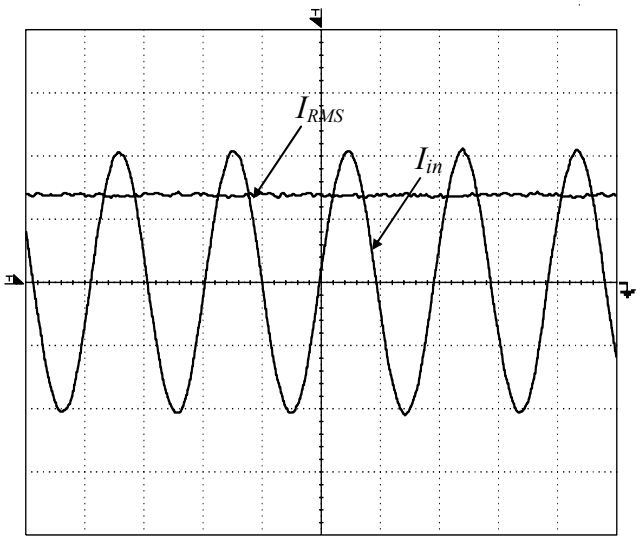
Fig. 3.5 Experimental results for the input signals: (a) sinusoidal; (b) triangular; and (c) square wave. (Vertical scale: 0.5V/div. Horizontal scale: 0.5ms/div)



(a)



(b)



(c)

Fig. 3.6 Experimental results of I_{RMS} with I_{in}=1mA for:

(a) f = 500Hz ; (Vertical scale: 0.5V/div. Horizontal scale: 1ms/div)

(b) f = 5kHz ; (Vertical scale: 0.5V/div. Horizontal scale: 100μs/div) and

(c) f = 5MHz ; (Vertical scale: 0.5V/div. Horizontal scale: 100ns/div).

From the Fig.3.6(a), 3.6(b) and 3.6(c), we can notice that the output ripple for the input signal at low frequencies, i.e. f = 500Hz, is higher than the case of the input signals with higher frequency. This is due to that, in this case, the capacitor C_{AV} is selected for f_{MIN} = 100Hz. We will further study this effect through the simulation result owing to that the ripple cannot accurately be measured from the experimental results. Usually, the % ripple is calculated by

$$\% \text{ ripple} = (I_{ripple(p\text{-}p)}/I_{DC}) \times 100\% \qquad (3.34)$$

where $I_{ripple(p\text{-}p)}$ is the peak to peak amplitude of the output current and I_{DC} is the DC component of the output current. From the simulation results at f = 500 Hz, 5 kHz and 5 MHz, the output signals have percent ripple errors of about 1.1% , 0.13% and 0.0001%, respectively. On the other hand, according to eqn.(3.8), since the averaging capacitor is selected 20 times grater than the predicted value (C_{AV}=10μF) and for I_M = 1mA, the calculated output percent ripple is about 1% at f = 500Hz. It agree with the simulation results above. Fig. 3.7 shows the simulated results of the I_{RMS} for 3 difference values of the capacitor C_{AV}, i.e. 1μF, 5μF and 10μF, when the input is a sinusoidal waveform with the peak amplitude of 1 mA and the frequency f = 1 kHz. The results show that the circuit will provide the I_{RMS} with lower ripple if a larger capacitor is used. But, however, it will result in a longer settling time.

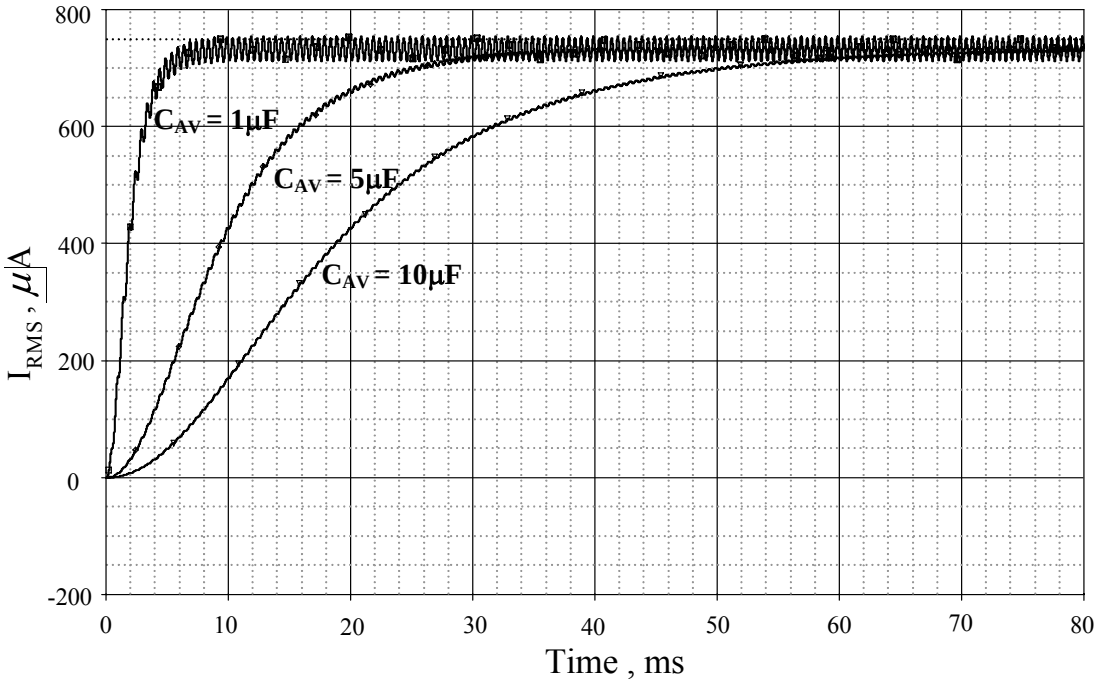


Fig. 3.7 The I_{RMS} that simulated for 3 different values of the capacitor C_{AV}.

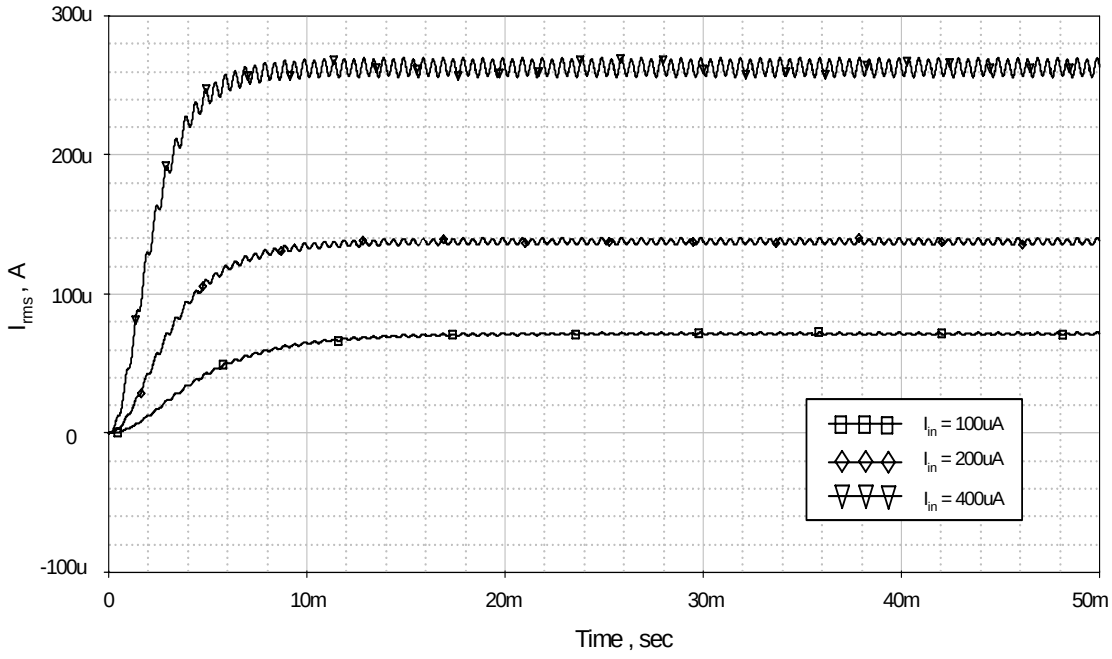


Fig. 3.8 Settling time versus input current (I_{in}).

Fig. 3.8 show the simulated results of the proposed RMS-to-DC converter settling time versus the signal input current I_{in} . The results were simulated for the case of I_{in}=400µA, 200µA and 100µA

where the capacitor C_{AV} = 0.5μF and the frequency f = 1 kHz, respectively. The settling time is about 6.22ms, 7.76ms and 11ms, respectively with less than 5% of reading error. This simulation results demonstrated that, the settling time is depending by the averaging time constant ($\tau = C_{AV}/g_{m7}$). The settling time varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased.

The experimental results that demonstrate the linearity of the RMS-to-DC converter are shown in Fig.3.9. The transfer characteristics are the plots of the I_{RMS} against the input signal current I_{in} with the peak amplitude varied from 300μA to 1.5mA, for the sine, triangular and square waveforms. The signal frequencies are 1kHz and C_{AV}=10μF. We found that the maximum conversion nonlinearity of about 2% was achieved. It should be noted that the lower limit of the circuit is due to the fact that the I_{RMS} is feedback to be the bias current I_b of the circuit. Therefore, through I_b, the I_{RMS} should be large enough to bias all the transistors in their saturation regions.

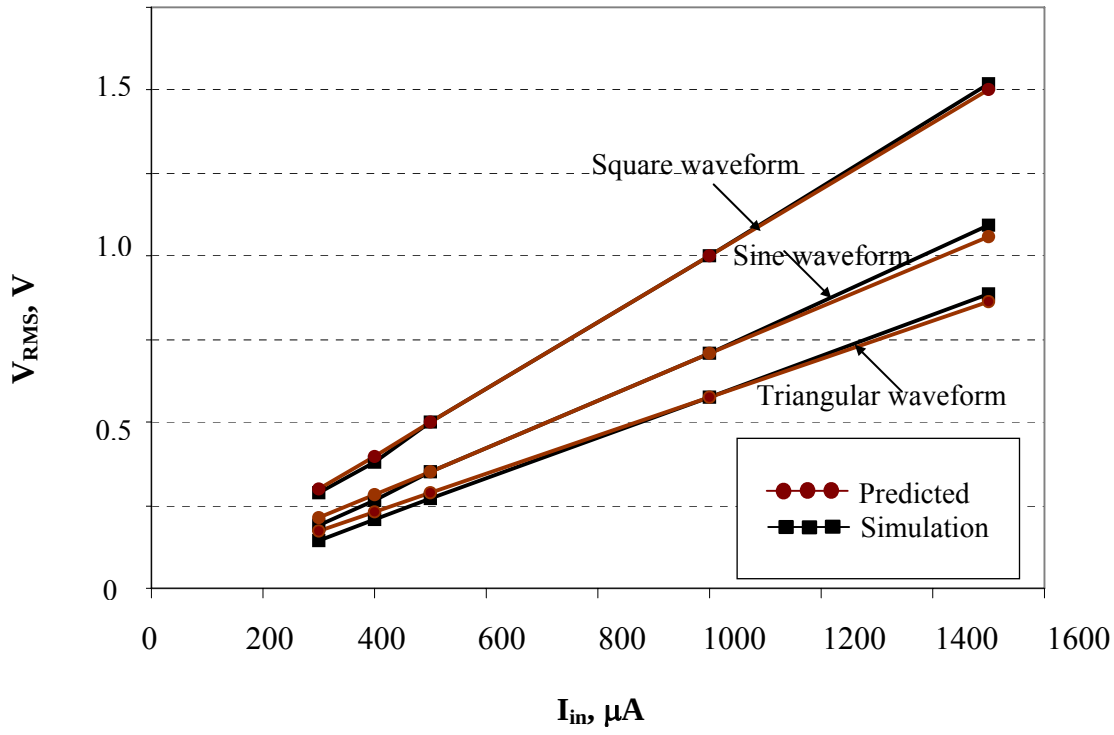


Fig. 3.9 DC transfer characteristic curves of the rms-to-dc converter circuit.

The relation of I_{RMS} between I_b and I_{in} can be shows from these results. For example, the input signals is sinusoidal, triangular and square waveforms, respectively, for $I_{in(peak)}$ = 1mA, f = 1 kHz. In the case of input waveform is sinusoidal with amplitude

Sinusoidal : I_b = 0.25mA , I_{RMS} = 0.714 mA Error = 0.01% of reading

Triangular : I_b = 0.2mA , I_{RMS} = 0.612 mA Error = 0.06% of reading

Square : I_b = 0.35mA , I_{RMS} = 1.05 mA Error = 0.05% of reading.

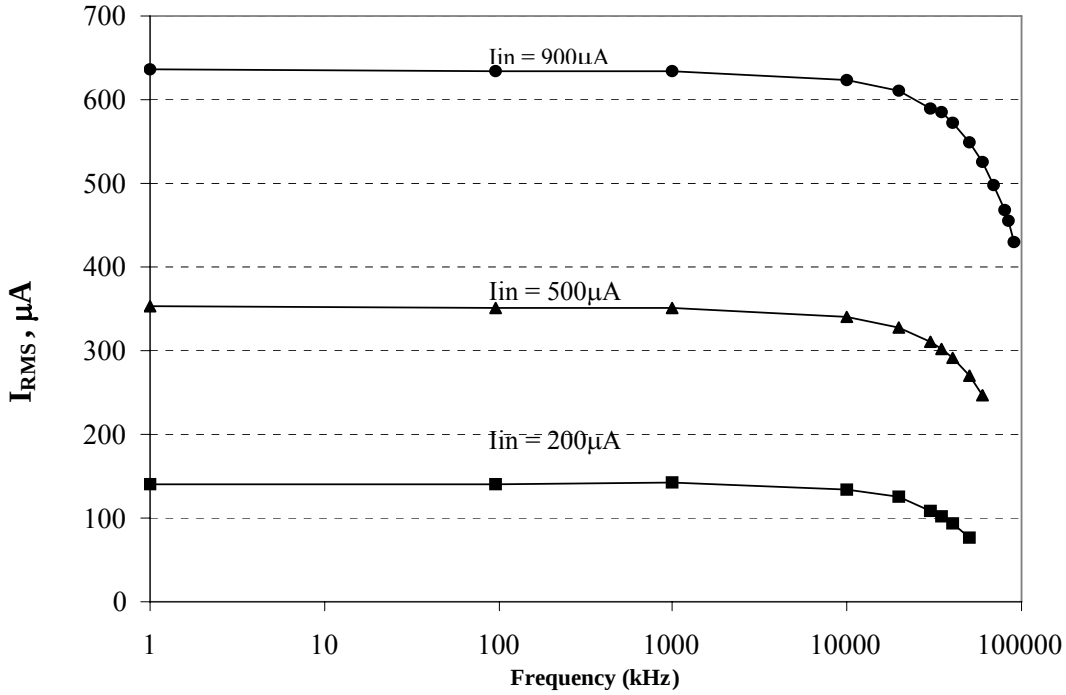


Fig. 3.10 High-frequency responses due to the variation of I_{in}.

Due to the stray capacitances in the bread boarding circuit, the high frequency response capability was not measured directly. The high frequency performance was studied through PSPICE simulation. Fig. 3.10 shows the frequency response for difference values of the input current (I_{in}). The input signals are sine waves with the amplitude of 20%, 50% and 90% of the full-scale current (I_{in} = 1mA$_{(peak)}$). The results show the bandwidth of about 35 MHz, 60 MHz and 85MHz, respectively. The results are agreed with the predicted value from the eqn. (3.31), where the bandwidth drops off as the input current signal is reduced. The simulation results for the –3dB

bandwidth with the peak input current ranging from I_{in} = 100μA to 1000μA were summarized in the Table 3.3. The simulated power dissipation for I_{in} = 1mA is about 6.04nW, which is very low.

Table 3.3 Performance of the RMS-to-DC converter design based on CMOS complementary CD4007.

Parameters	Simulated results
Supply voltage (rated)	5V to 15V
Input current range (MAX)	1.5mA
Power Dissipation	6.04nW (at I_{in}=0)
Gain error	2% Max. nonlinearity, 100 μA to 1.5mA input
Peak amplitude value I_{in} = 100 μA I_{in} = 200 μA I_{in} = 500 μA I_{in} = 900 μA I_{in} = 1000 μA I_{in} = 1500 μA	-3 dB bandwidth 25 MHz 40 MHz 60 MHz 85 MHz 90 MHz 100 MHz

Generally, crest factor is the ratio of the peak value relative to the RMS value. So far the characteristics of the circuit have been studied for the common waveforms as sine and triangle waveforms, which have relatively low crest factor ($\leq$2). The simulation results for the input signal with difference crest factors are shown in Fig 3.11. The rectangular pulse train with pulse width of 1ms was used for this test, since it is the worst-case waveform for RMS measurement. The duty cycle and peak amplitude were adjusted to produce a crest factors from 1 to 5, while maintaining a constant $1mA_{(peak)}$ input current [64]. We found that the proposed RMS-to-DC converter performs very well with crest factors of 3 or less. As shown in the Fig.3.11, for the case of crest factor equal to 3, the conversion error is less than 5%. However, for the higher crest factor, such as 4, the conversion error is more than 8%. This is due to that the waveforms with higher crest factor, the RMS value is decreased. Consequently, the bias current of the RMS-to-DC converter circuit is also reduced and will effect to

the accuracy of the circuit. To provide good accuracy at high crest factor, the input current should be increased. For example, with the crest factor = 4, the conversion error was reduced to 6% if we set the input current (I_{in}) equal to 2mA.

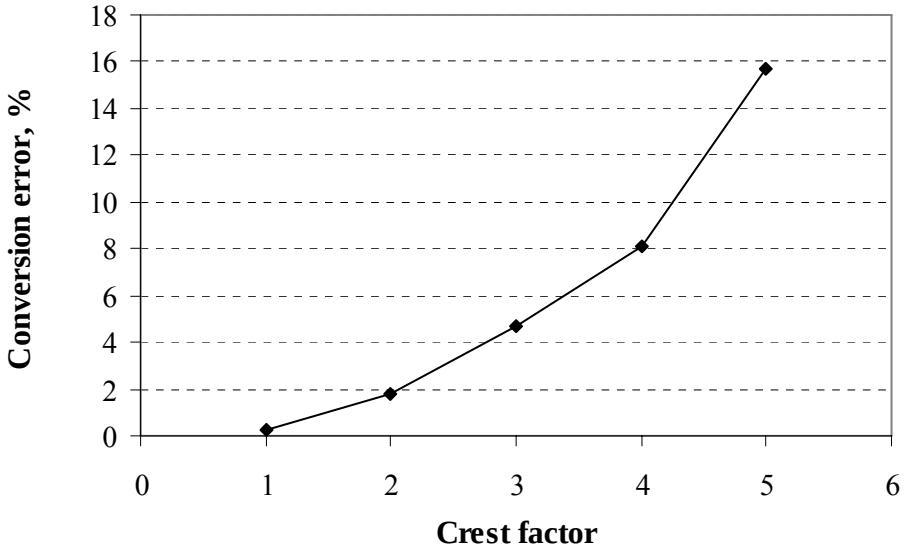
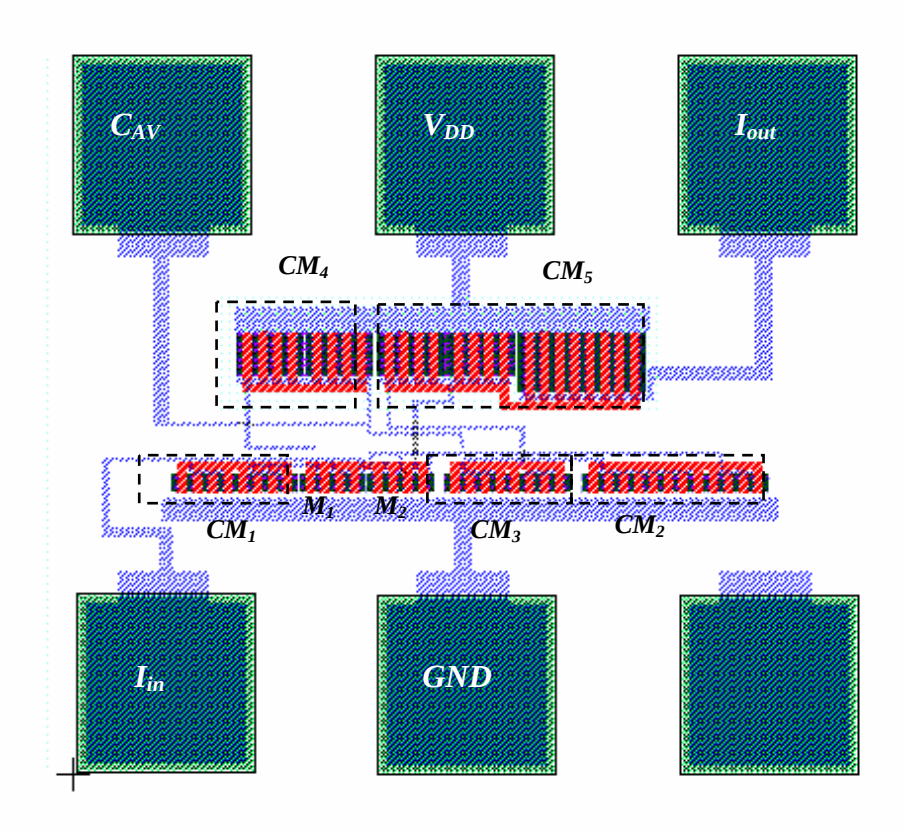


Fig. 3.11 Simulation results for the additional error versus crest factor.

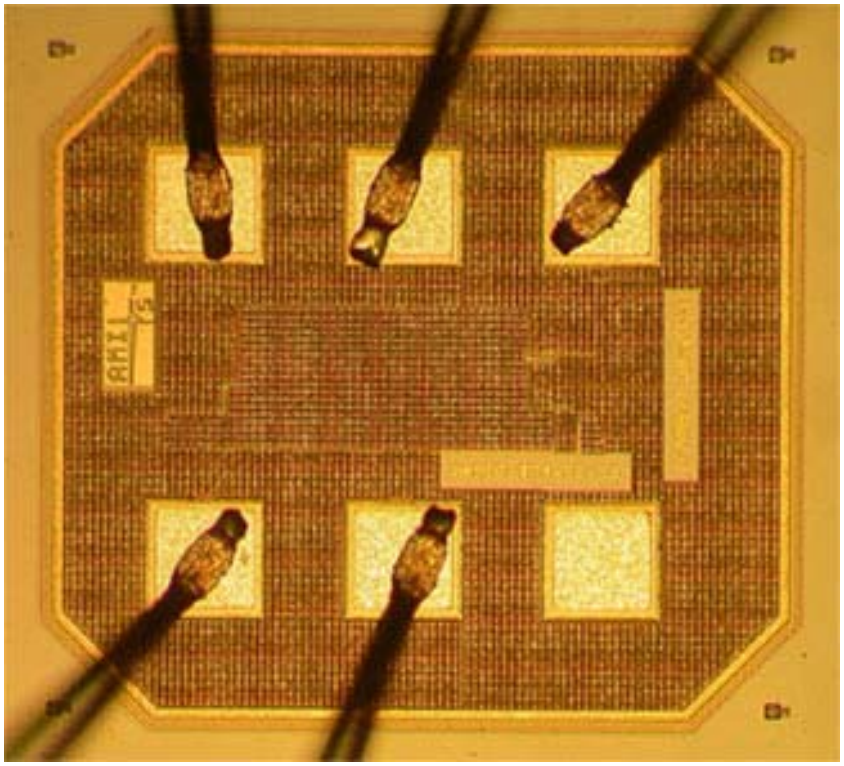
3.5 The implementation of the proposed RMS-to-DC converter and its experimentations.

The true RMS-to-DC converter that proposed in this thesis can be realize for real chip. The conversion circuit is simple, suitable for implementing in monolithic integrated form, and can be readily integrated as part of a larger system.

Fig. 3.12 shows the layout and microphotograph, fabricated in a 0.5 microns CMOS Technology AMIS process with $V_{th} \cong 0.7V$, of the proposed true RMS-to-DC converter. The total chip area occupied was 484x442 micron^2 excluding the bonding pads.



(a)



(b)

Fig. 3.12 The True RMS-to-DC Converter: (a) The layout and (b) Microphotograph.

The performance of the integrated true RMS-to-DC converter has been studied through simulation and experimental results. The simulation has been carried out by employing spectre in CADENCE simulation program and using the transistor parameters of the 0.5 microns CMOS Technology AMIS process. The transistor dimensions of the circuit in Fig. 3.2 are in micron, where the dimension of the transistors M_5 is W=80μm and L=5μm, M_{13} is W=283μm and L=5μm, M_1-M_4, M_6 are W=40μm and L=5μm and M_9-M_{12} are W=100μm and L=5μm. The power supply voltage were set to V_{DD}= 5V.

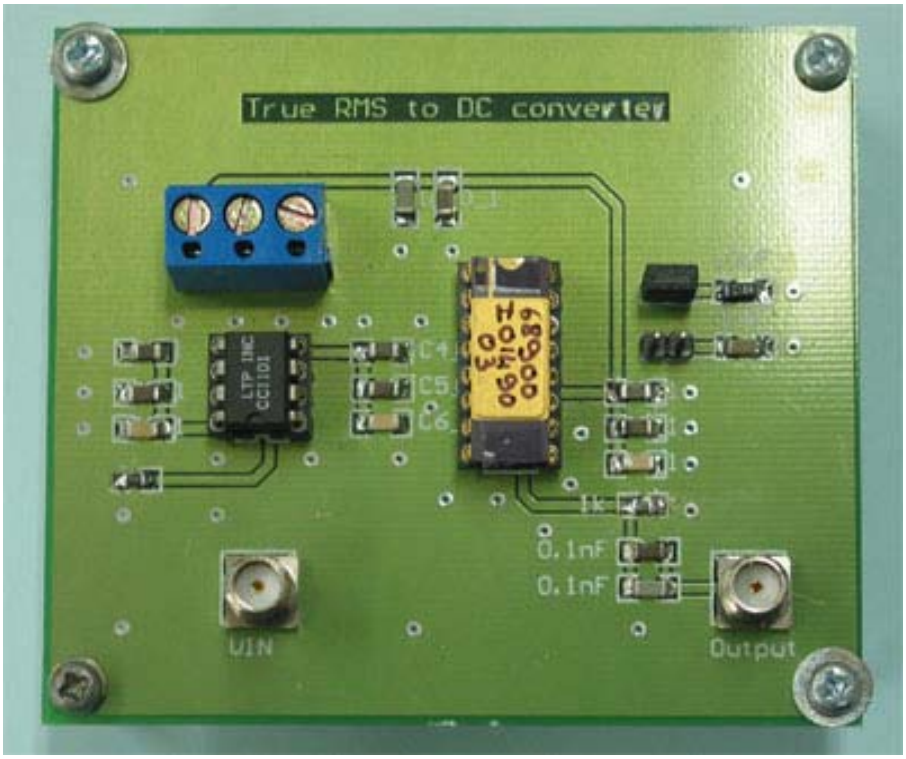
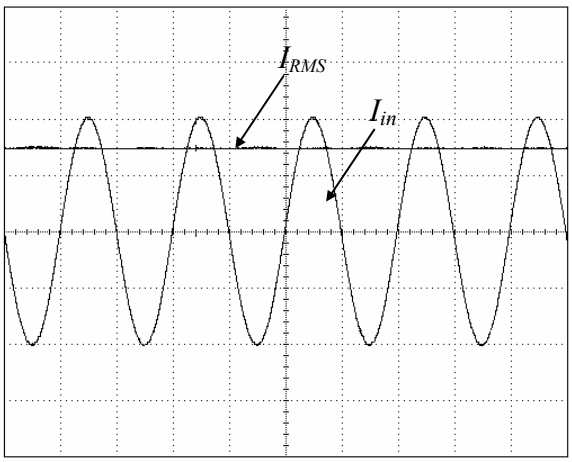
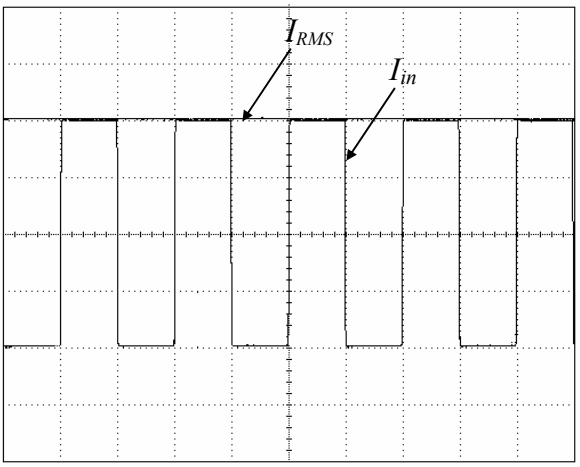


Fig. 3.13 True RMS-to-DC converter measurement setup

Employing the chip of the Fig.3.12, the measurement setup is shown in Fig. 3.13. The external capacitor C_{AV} is 10μF. Due to the proposed RMS-to-DC converter operates in current mode, a commercially available current conveyor CCII01 was used to convert the input voltage V_{in} into the input current signal I_{in}. The resistor R_{in}=1kΩ is connected at ports X and the input voltage was applied to the port Y of the CCII. For example, by setting the input signal current of I_{in} = $1mA_{(peak)}$, the input voltage equal to 1V is applied to port Y of the CCII. To measure the value of the I_{RMS}, a resistor of 1kΩ was connected at the output of the RMS-to-DC converter and the voltage across the resistor R_o is measured instead.



(a)



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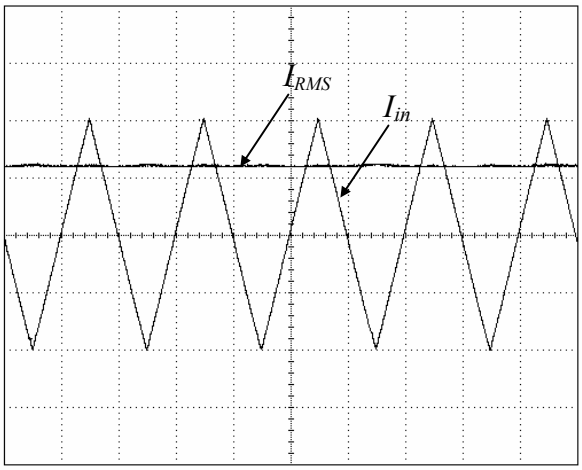

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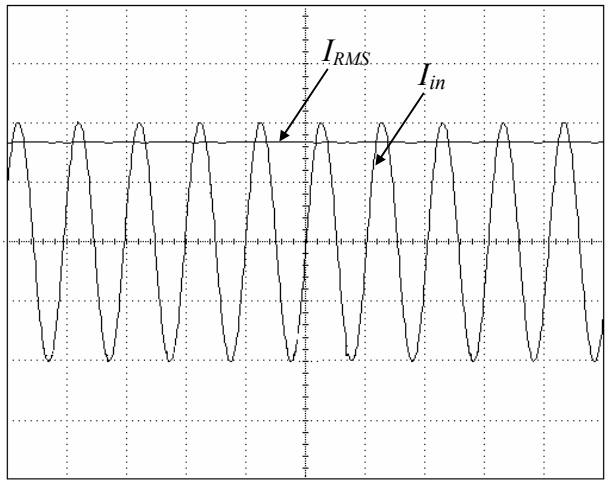

(d)

Fig. 3.14 Experimental results for the input signals: (a) sinusoidal; (b) triangular; (c) square wave; (Vertical scale: 0.5V/div. Horizontal scale: 5us/div) and (d) sinusoidal. (Vertical scale: 0.5V/div. Horizontal scale: 200ns/div)

The experimental results in Fig. 3.14(a), 3.14(b) and 3.14(c) show the I_{RMS} for the input signal of sinusoidal, triangular and square waveforms, respectively, with the peak amplitude of 1mA and with the frequency of 100 kHz. The I_{RMS} signal with the amplitude close to 0.7mA, 0.5mA, and 1mA, respectively, with the error of less than 10μA, were achieved. These results demonstrated that the circuit can be accurately converted the AC signals into the RMS values. To demonstrate that the circuit can operate in a wide frequency range, Fig. 3.14(d) shows the measured I_{RMS} for the cases of the sinusoidal input signal with the frequencies of f = 5MHz, and with the peak amplitude of 1mA. The results show that the I_{RMS} signals with the amplitude of about 0.7mA are achieved. The dc error from the simulation results is about 12%. From the simulation results at f = 100 Hz, 100kHz and 5 MHz, the output signal have percent ripple error of about 3% , 1.35% and 0.0001%, respectively.

The high frequency performance was studied through cadence simulation. The simulation results for the –3dB bandwidth with the peak input current ranging from I_{in} = 100μA to 1.5mA were summarized in the Table 3.4.

Table 3.4 Performance of the RMS-to-DC converter design based on 0.5µm CMOS AMIS technology .

Parameters	Simulated Results
Supply voltage (rated)	1.5V-5V
Input current range $_{(MAX)}$	1.5mA
Power Dissipated	0.1mW
Gain error	2% Max. nonlinearity, 100µA to 1.5mA input
Peak amplitude value	-3 dB bandwidth
I_{in} = 100 µA	20 MHz
I_{in} = 200 µA	40 MHz
I_{in} = 500 µA	60 MHz
I_{in} = 900 µA	85 MHz
I_{in} = 1000 µA	90 MHz
I_{in} = 1500 µA	100 MHz

Table 3.5 Summary of RMS-to-DC converter characteristics

Characteristics	**CMOS complementary CD4007**	**0.5µm CMOS AMIS Technology**
Supply voltage	Min : 5V Max : 15V	Min : 1.5V Max : 5V
I_{in}	Min : 100µA Max : 1.5mA	Min : 100µA Max : 1.5mA
Conversion accuracy		
Total error	100µA-1mA Max. ± 3% of reading	100µA-1mA Max. ± 3% of reading
Nonlinearity	2% at 1mA 1MHz	2% at 1mA 1MHz
Error VS Crest factor		
CF = 3	4.7%	4%
CF = 5	16.7%	13%
Input Characteristics		
Signal range	5V supply 1 mA I_{RMS}	5V supply 1 mA I_{RMS}
Peak transient	1 mA_{P-P}	1 mA_{P-P}

Characteristics	**CMOS complementary CD4007**	**0.5µm CMOS AMIS Technology**
Input offset current	1.5 pA	8 pA
Frequency Response		
BW for 5% additional error		
	Frequency (Hz)	Frequency (Hz)
I_{in} = 100µA	25MHz	20MHz
I_{in} = 200µA	40MHz	40MHz
I_{in} = 500µA	60MHz	60MHz
I_{in} = 900µA	85MHz	85MHz
I_{in} = 1mA	90MHz	90MHz
I_{in} = 1.5mA	100MHz	100MHz
Out put characteristics		
Offset current	10pA	50pA

Table 3.5 shows the summary characteristics of the proposed true rms to dc converter of CMOS complementary CD4007 and 0.5µm CMOS AMIS technology. There are the conversion accuracy, the error VS crest factor, the input characteristics, the frequency response and the output characteristics. This results quite agree with the prediction.

The performance of some commercial RMS-to-DC converter circuits and the proposed RMS-to-DC converter in this thesis are listed in Table 3.6.

Table 3.6 The performance of commercial RMS-to-DC converters and the proposed RMS to DC converter.

	AD536AJ	**AD637J**	**AD736J**	**AD735**	**SMM-21110**	***Proposed RMS***
Voltages						
Supplies (rated)	±15 V	±15 V	±5 V	±5 V	±15 V	1.5V to5 V
Input range(max)	$7V_{RMS}$	$7V_{RMS}$	$1V_{RMS}$	$1V_{RMS}$	$3mA_{pk-pk}$	100µA-1.5mA
Accuracy						
Gain error	0.5%	0.5%	0.5%	0.5%	±0.5 dB	2%
Offset error	5mV	1mV	0.5mV	0.4mV	5nA	10pA-0.1nA
Crest factor error	CF=3 0.1% CF=7 1.0%	CF=3 0.1% CF=10 1.0%	CF=3 0.7% CF=5 2.5%	CF=3 0.7% CF=5 2.5%	CF=5 0.5dB CF=8 1.0dB	CF = 3 4 % CF = 5 13%
Dynamic						
3 dB bandwidth						
V_{in} = 10mV	90 kHz	80 kHz	55 kHz	5.5 kHz	50 kHz (I_{in}=1µA)	25 MHz (I_{in}=100µA)
V_{in} = 10mV	450 kHz	600 kHz	170 kHz	170 kHz	300 kHz (I_{in}=10µA)	60 MHz (I_{in}=500µA)
V_{in} = 1V	2.3 MHz	5 MHz			1.5 MHz (I_{in}=1mA)	90 MHz (I_{in}=1mA)
Comments*						
	(1)	(2)	(3)	(4)	(5)	(6)

Comments * :

(1) Monolithic device. Gain and offset errors easily trimmed. The AD636 is a very similar device, but designed for signals below 200mV.

(2) Wider bandwidth RMS-to-DC converter.

(3) Low power monolithic RMS-to-DC converter. Similar device is the AD737.

(4) Low power monolithic RMS-to-DC converter. Without output buffer. Contains power down circuitry. Similar device AD736.

(5) Current input to current output device. Requires several external resistors for voltage operation.

(6) Current input to current output device. Wide bandwidth and low power true RMS-to-DC converter.

This table shows that the proposed RMS-to-DC converter has some advantages over other methods. The circuit operates for single supply at low voltage, wide input swing, wide bandwidth.

Table 3.7 The performance of the other RMS-to-DC converters and the proposed RMS to DC converter

RMS-to-DC	[6]	[7]	[56]	propose RMS
Technology	Bipolar	Bipolar	MOS model 5	0.5μm AMIS
V_{supply}	2V-4V	± 15V	± 1.5V	1.5V-5V
Input Signal	V_{in}= 4V (max)	V_{in}=13.4V(max), I_{in}= 10μA-1mA	I_{in}= 40μA(max)	I_{in}=100μA-1.5mA
Bandwidth	5MHz	150MHz	>100kHz	90MHz
Accuracy	NA	0.2% at 1mA	1% at 40μA	2% at 1mA
Crest factor error	CF=10 1%	CF=3 0.25% CF=10 3%	NA	CF =3 4% CF=5 13%
Input waveform	All waveform	All waveform	sinusoidal	All waveform
RMS-to-DC	True RMS-to-DC	True RMS-to-DC	Pseudo RMS	True RMS-to-DC

This table shows that the proposed RMS-to-DC converter has some advantages over other methods. The circuit operates for single supply at low voltage, wide dynamic range and wide bandwidth.

3.6 Discussion and Conclusion

In this chapter, a simple CMOS true RMS-to-DC converter circuit has been developed that based on the use of the characteristic of a CMOS squaring circuit, where all the transistors are biased in the saturation region. The realization scheme is based on the implicit computation method and is suitable for implemented in standard CMOS process. The circuit is suitable for all

input waveforms. Moreover the wide bandwidth characteristic is obtained since the circuit structure is simple and requires a few components.

The characteristics of the proposed RMS-to-DC converter are studied by the implementation of CMOS complementary pairs CD4007 on a bread-board discrete circuit. The transient response, DC transfer characteristic and the error versus crest factor are tested by the experimentation. Due to the stray capacitances in the bread boarding circuit, the high frequency response capability was not measured directly, PSPICE simulation is used for study the high frequency performance. In addition, to confirm that this proposed circuit is suitable for implementing in monolithic integrated form. This circuit is also studied based on 0.5 microns CMOS technology AMIS process by PSPICE simulation results and it has been fabricated. The chip performances are tested by the measurement setup, there are agreed with the simulation and the implementation by CMOS complementary CD4007. The RMS-to-DC converter performances from the simulation, the experimental of discrete circuit and the experimental of real chip are included in this chapter. The simulation and experimental results are agreed with the prediction.