CHAPTER 2

Active circuit elements

In this chapter, the circuit elements which will be used as major active circuit elements in this thesis are described. The circuit descriptions of the CMOS current mirror, the CMOS current squarer circuit and the CMOS OTA are respectively outlined.

2.1 Current-mirror

2.1.1 Circuit Description

Current mirrors have come to be widely used in analog integrated circuits both as biasing elements and as active load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature [19], [20].

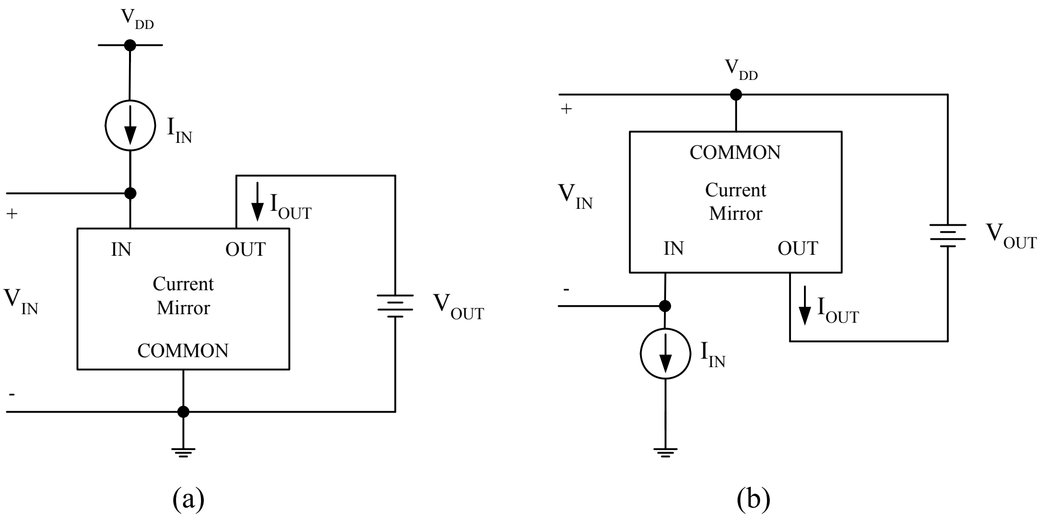

Fig. 2.1 Current-Mirror block diagram referenced to (a) ground and (b) the positive supply.

A current mirror is an element with at least three terminals, as shown in Fig. 2.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. The output current is ideally equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is simply reflected to the output, leading to the name current mirror. Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminal. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire supply voltage to appear across the input current source, simplifying its transistor-level design. More than one input and/or output terminals are sometimes used.

For MOS transistor, a commonly used parameter for the characterization of channel length modulation (λ) is the reciprocal of the Early voltage (V_A), $\lambda = 1/V_A$. Thus we can include the effect of channel-length modulation in the *I-V* characteristics. If one assumes that the transistors operate in the saturation region $(V_{DS} > V_{GS} - V_T)$, the value of I_D in this region can be given by

$$I_D = \frac{\mu_n C_{ox} W}{2L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right) \tag{2.1}$$

where the parameters are:

μ_n	surface mobility of the channel, $\left(cm^2 / volt \cdot \sec\right)$
$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$	gate oxide capacitance density, $\left(F/cm^2\right)$
W	effective channel width, (m)
L	effective channel length, (m)
V_T	threshold voltage, (volt)
λ	channel length modulation parameter, (volt^{-1})

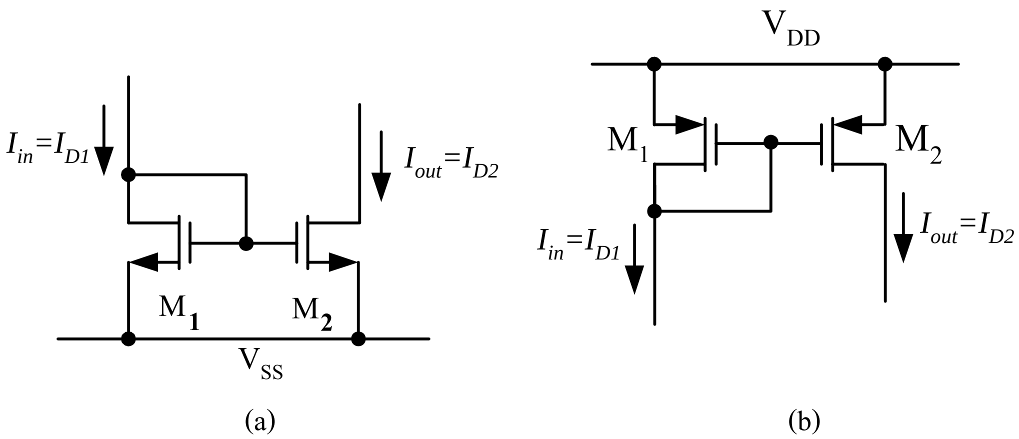

Fig. 2.2 Simple MOS current mirrors

(a) NMOS current mirror (b) PMOS current mirror

A simple realization of a CMOS current-mirror is presented in Fig. 2.2. From the circuit

$$V_{GS2} = V_{T2} + \sqrt{\frac{2I_{D2}}{\mu_n C_{ox}(W/L)_2}} = V_{GS1} = V_{T1} + \sqrt{\frac{2I_{D1}}{\mu_n C_{ox}(W/L)_1}} \quad (2.2)$$

If the transistors are identical, $(W/L)_2=(W/L)_1$, and therefore we get the relation of the currents

$$I_{out} = I_{D2} = I_{D1} \quad (2.3)$$

Eqn. (2.3) shows that the current that flows in the drain of M_1 is mirrored to the drain of M_2. Using Kirchhoff 's Curent Law, eqn. (2.3) yield.

$$I_{out} = I_{D2} = I_{in} \quad (2.4)$$

Thus for identical device operating in the saturation region with infinite output resistance, the gain of the current mirror is unity. This result holds when the gate currents are zero; that is, eqn. (2.4) is at least approximately correct for DC and low-frequency AC currents. As the input frequency increases, however, the gate currents of M_1 and M_2 increase because each transistor has a nonzero gate-source capacitance. In practice, the devices need not be identical. Then from eqns. (2.2) and (2.4),

$$I_{out} = \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} I_{D1}$$

$$= \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} I_{in} \tag{2.5}$$

Then, if the effect of source and load impedances is first neglected, the current-mirror large signal equation shows current gain (A_i) proportional to the aspect ratios of transistors M_1 and M_2, with certain additional dependencies

$$A_i = \frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1}\left(\frac{V_{GS2}-V_{T2}}{V_{GS1}-V_{T1}}\right)^2 \cdot \frac{1+\lambda V_{DS2}}{1+\lambda V_{DS1}} \frac{\mu_{n2}C_{ox2}}{\mu_{n1}C_{ox1}} \tag{2.6}$$

From this equation, we found that the process variation of the channel width W, channel length L, mobility μ_n, and oxide thickness t_{ox} can produce linear gain error.

If the effect of channel-length modulation can be neglected ($\lambda = 0$), assume the process parameters such as V_T, μ_n, C_{ox}, of MOS transistor are matched and $V_{DS2} \cong V_{DS1}$. The eqn. (2.5) can be rewritten as

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{D1} = \frac{(W/L)_2}{(W/L)_1} I_{in} \tag{2.7}$$

and the current gain (A_i) in eqn. (2.6) can be rewritten as

$$A_i = \frac{I_{out}}{I_{in}} = \frac{(W/L)_2}{(W/L)_1} \tag{2.8}$$

Eqn. (2.8) shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths (W) or the lengths (L) can be made unequal in principle.

Due to finite input and output impedances have a significant effect on the current mirror gain accuracy. The small signal equivalent circuit of the current mirror will be used to analyze the input impedance , the output impedance and the current gain.

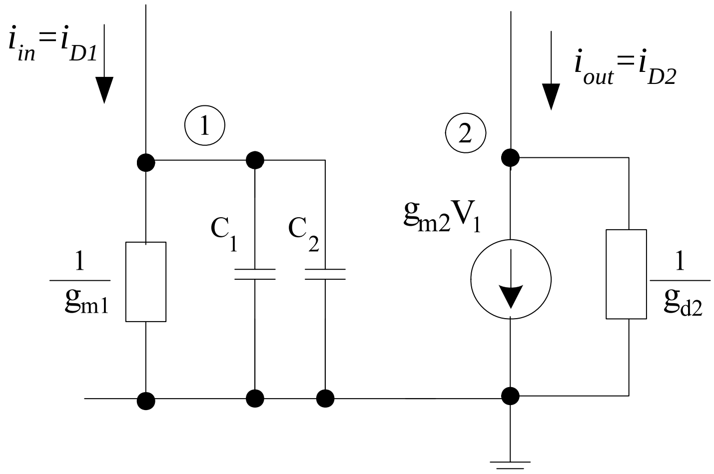

Fig. 2.3 Small signal equivalent circuit of NMOS current mirror in Fig. 2.2

From Fig. 2.3, the small-signal input impedance of the current mirror depends on the transconductance of the input transistor M_1

$$r_{in} \approx \frac{1}{g_{m1}} = \frac{1}{\sqrt{2\mu_{o1}C_{ox1}\frac{W_1}{L_1}I_{D1}}} \tag{2.9}$$

where g_{m1} is the transconductance of transistor M_1, and the small-signal output impedance depends on the drain-source conductance of the output transistor M_2, accordingly

$$r_{out} \approx \frac{1}{g_{d2}} = \frac{1}{\lambda I_{D2}} \tag{2.10}$$

where g_{d2} is the drain-source conductance of the transistor M_2.

The relation between the input current (I_{in}) and the output current (I_{out}) of the basic current mirror can be written as

$$I_{out} = \frac{g_{m2}}{g_{m1}} I_{in} \tag{2.11}$$

For the high frequency response of the simple current mirror, from Fig. 2.3 the transfer function of input current and output current ($i_{out}(s)/i_{in}(s)$) can be expressed in eqn. (2.12)

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m2}}{g_{m1}} \cdot \frac{1}{1 + \frac{s(C_1 + C_2)}{g_{m1}}} \tag{2.12}$$

where $C_i = C_{gsi} + C_{gdi}$

C_{gsi} is the gate-source capacitance of transistor M_i, (F)

C_{gdi} is the gate-drain capacitance of transistor M_i , (F)

The basic current mirror characteristics from eqns. (2.5) to (2.12) show that the current gain can be controlled by the channel width (W) and/or channel length (L) of the MOS transistor.

From eqn. (2.12) the cut-off frequency of the basic current mirror in Fig. 2.2 which depending on one pole can be expressed as eqn. (2.13)

$$f_{-3dB} \cong \frac{g_{m1}}{2\pi(C_1 + C_2)} \tag{2.13}$$

Eqn. (2.13) shows that the dominant pole of the basic current mirror is normally situated at quite high frequencies because of the low value of g_{m1}. Thus, the current mirror operates well up to high frequencies.

In modern sub-micron CMOS processes the g_m/g_{ds} ratio is less than 100 and consequently results in not a significant gain error. This gain error is usually reduced by increasing the output impedance using different cascode mirror topologies rather than the simple two transistor current-mirror. In this case, however, the drain-source voltages $V_{DS1} \neq V_{GS}$ gain error as expressed in eqn. 2.6 may result. Moreover, these drain voltages are signal dependent and thus the channel length modulation λ , which continuously increases as progressively shorter channel length devices are introduced, can additionally produce significant amount of distortion. Therefore, topological improvements must be made in the current-mirror in order to maintain the drain-source voltages V_{DS1} and V_{DS2} as equal as possible. This is achieved by using the current-mirror topologies rather than the simple current-mirror or the cascode current-mirror that shows in Fig. 2.4. The additional current-mirror constructed of transistors M_3 and M_4 is added on top of the original current mirror in order to force the drain voltage V_{DS2} of the transistor M_2 equal to $V_{DS1} = V_{DS2} = V_{GS}$ [19]. Unfortunately, this reduces significantly the input and output voltage ranges and thus the minimum supply voltage of the circuit is quite high.

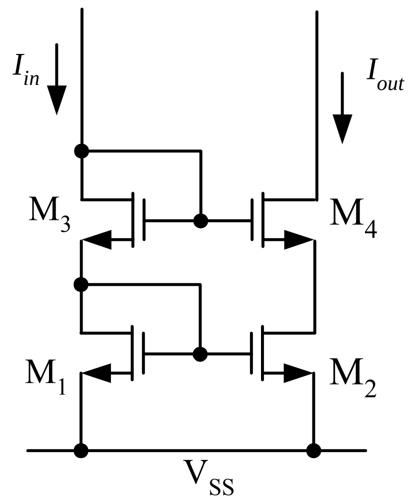

Fig. 2.4 A simple four transistor cascode current mirror.

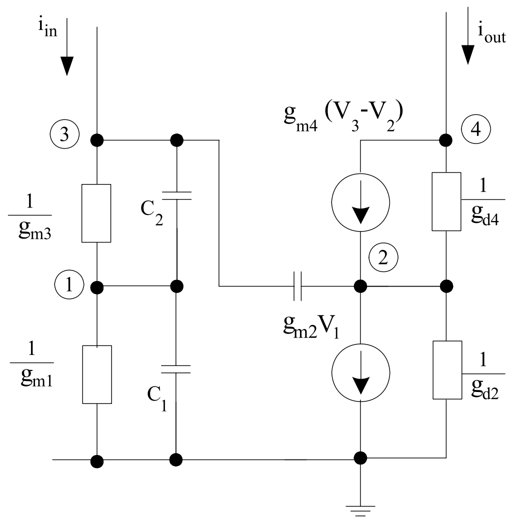

Fig. 2.5 Small signal equivalent circuit of cascode current mirror in Fig. 2.4

From the small signal equivalent circuit in Fig. 2.5, the relation between the input current (i_{in}) and the output current (i_{out}) of the cascode current mirror in Fig 2.3 can be written as

$$i_{out} = \frac{g_{m2} g_{m4}}{g_{m1} g_{m3}} i_{in} \tag{2.14}$$

The input impedance of the cascode current mirror can be written as

$$r_{in} = \frac{g_{m1} + g_{m3}}{g_{m1} g_{m3}} \tag{2.15}$$

and the output impedance can be written as

$$r_{out} = r_{d2} + r_{d4} + g_{m4} r_{d2} r_{d4} \cong g_{m4} r_{d2} r_{d4} \tag{2.16}$$

where r_{di} is the drain-source resistance of the MOS transistor M_i

The frequency response of the cascode current mirror in Fig. 2.5 can be expressed as

$$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m4}}{g_{m1}}\left[\frac{1}{\frac{C_1(C_2+C_3)}{g_{m1}g_{m2}}s^2 + \frac{((C_1+C_2)(g_{m1}+g_{m2})+C_{gs4}g_{m2})}{g_{m1}g_{m2}}s+1}\right] \quad (2.17)$$

Eqn. (2.17) shows that the cascode current mirror has a complex pole. Therefore, its bandwidth of the cascode current mirror is less than the basic current mirror. However, the cascode current mirror has higher output resistance and less error in current i_{out}.

Table 2.1 Characteristics summary of the basic current mirror and cascode current mirror

Current mirror	Input resistance (r_{in})	Output resistance (r_{out})	Frequency response $i_{out}(s)/i_{in}(s)$
Basic Current mirror	$r_{in} = 1/g_{m1}$	$r_{out} = 1/g_{d2}$	$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m2}}{g_{m1}}\left(\frac{1}{1+\frac{S(C_1+C_2)}{g_{m1}}}\right)$
Cascode Current mirror	$r_{in} = \frac{g_{m1}+g_{m3}}{g_{m1}g_{m3}}$	$r_{out} = r_{d2}+r_{d4}+g_{m4}r_{d2}r_{d4}$ $\cong g_{m4}r_{d2}r_{d4}$	$\frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m4}}{g_{m1}}\left[\frac{1}{\frac{C_1(C_2+C_3)}{g_{m1}g_{m2}}s^2 + \frac{((C_1+C_2)(g_{m1}+g_{m2})+C_{gs4}g_{m2})}{g_{m1}g_{m2}}s+1}\right]$

2.2 CMOS current squarer circuit

Squarer circuit is one of the useful basic circuit functions in the amplitude domain, the need for which arises quite often. They are essential to the extraction of the exact RMS value of a signal, and in power measurement in general.

Recently, the realization of squarer circuits have been proposed for various techniques [7], [21]-[30]. For [21]-[23], the circuits are designed by using the operational amplifier (op-amp) where the circuit designs with transistors that are operated in the saturation and the triode region. The output current is the function of their input voltage squared. On the other hand, the works in [24] - [30] are designed by using only MOS transistors. These circuits are function as a voltage-mode squarer circuit. The circuits are designed by using square-law characteristic. All of MOS transistor are biased in the saturation region. Finally, the [7] is a current-mode squarer circuit.

Some example of the proposed squarer circuits will be outlined as follow.

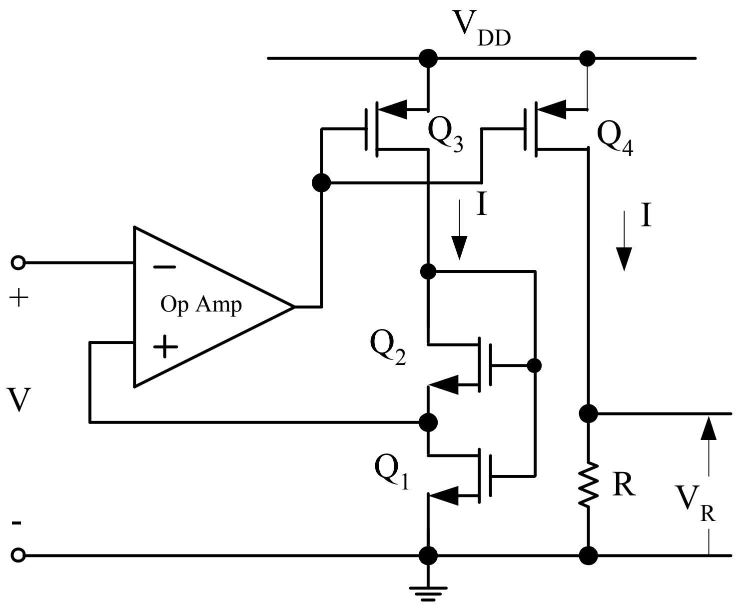

Fig. 2.6 Squarer circuit [21]

The squarer circuit that shown in Fig. 2.6 was proposed by *I.M. Filanovsky and H.P. Baltes* [21]. The circuit structure include an operational amplifier (op-amp) and nested transistor pair (Q_1 and Q_2) where transistor Q_1 operates in triode region. When the input voltage (V) is applied to the op-amp, the op-amp output voltage will force the transistor Q_3 and the current I, which will flow through the transistors Q_1 and Q_2 can be calculate as follow.

The transistor Q_2 will be pinch-off and transistor Q_1 will be forced into the triode region of operation. The gate-source voltage V_{GS2} of the transistor M_2 will be

$$V_{GS2} = V_{TN} + \sqrt{\frac{2I}{k_2}} \tag{2.18}$$

where V_{TN} is the threshold voltage of n-channel transistor and $K_2 = \mu_n C_{ox}(W/L)_2$ from the other side, due to the triode operation of Q_1, the current I will satisfy the equation

$$I = K_1(V_{GS1} - V_{TN})V - \frac{K_1 V^2}{2} \tag{2.19}$$

where $K_1 = \mu_n C_{ox}(W/L)_1$. Besides,

$$V_{GS1} = V + V_{GS2} \tag{2.20}$$

substituting (2.18) and (2.20) into (2.19), one can find that

$$I = K_1\left[\sqrt{(K_1/K_2)}\sqrt{(K_1/K_2)+1} + (K_1/K_2) + 1/2\right]V^2 \tag{2.21}$$

Transistors Q_3 and Q_4 are used to copy the current I to the output of the squaring circuit. Eqn. (2.21) shows that this circuit can operate as squarer function. The output current is proportional to the square of the input voltage. Due to this technique requires the operational amplifier, the circuit performance depends on the performance of the operational amplifier. Such as, the bandwidth is limited, since the cut-off frequency of the open-loop gain of the op-amp is typically in the range of 10-100Hz.

Fig. 2.7 shows the voltage-mode squarer circuit that proposed by *O.A. Seriki and R.W. Newcomb* [28]. The circuit is designed by the used of CMOS transistors. The circuit is function as voltage-mode squarer circuit.

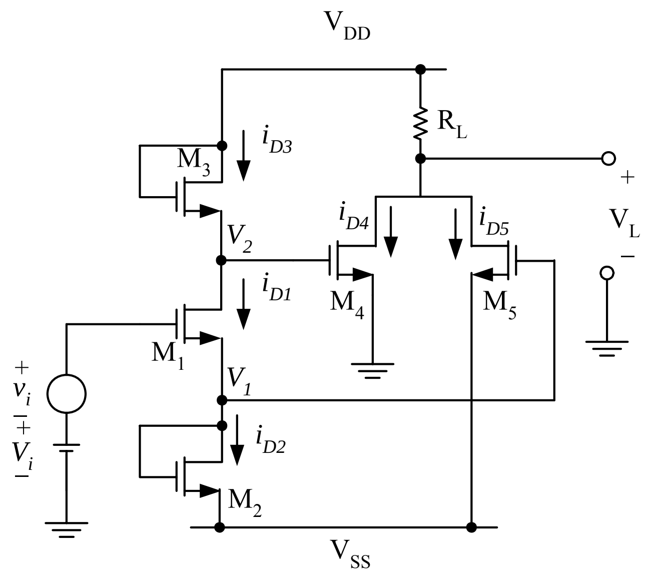

Fig. 2.7 Squarer circuit proposed by O.A. Seriki and R.W. Newcomb [2.8]

This circuit is a two-stage arrangement. The first stage which consisting of equal transistors M_1, M_2 and M_3 (NMOS) is a linear amplifier, where the output voltages V_1 and V_2 are measured with respect to ground, having their signal components the negative of each other. In the second stage, which is the squaring function, the current i_L that flowing through R_L is the sum of the drain currents i_{D4} and i_{D5} of the two equal transistors M_4 and M_5. These currents being squares of the inputs when the transistors are properly biased. For the circuit analysis, assuming the transistors are biased to operate in the square-law region, the drain current i_D of an n-channel MOS transistors is related to its gate-to-source voltage, V_{GS}, by

$$i_D = K(V_{GS} - V_T)^2 \tag{2.22}$$

Since the current i_{D1}, i_{D2} and i_{D3} flowing through the transistors are the same, the gate-to-source voltage V_{GS1}, V_{GS2} and V_{GS3} are equal. Since $V_{GS1}+V_{GS2}=2V_{GS2}=2V_{GS3}=V_i+V_{SS}+v_i$, Kirchhoff's voltage law shows that the voltages v_1 and v_2 are given by

$$v_1 = V_{DD} - V_{GS3} = V_{DD} - \frac{1}{2}(V_i + V_{SS}) - \frac{1}{2}v_i \tag{2.23}$$

$$v_2 = V_{GS2} - V_{SS} = \frac{1}{2}(V_i - V_{SS}) + \frac{1}{2}v_i \tag{2.24}$$

Hence, a signal v_i fed into the input of the first stage divided equally, but with opposite signs, between v_1 and v_2 to form the signal components of the voltages which control the gates of transistors M_4 and M_5 of the second stage.

The current i_L flowing through the resistor R_L is the sum of the drain current i_{D4} and i_{D5}. The total out put voltage, v_L, is given by

$$v_L = V_{oo} - KR_L(a_2 - a_1)v_i - \frac{1}{2}KR_L v_i^2 \tag{2.25}$$

where V_{oo} is the dc bias component , $V_{oo} = V_{DD} - KR_L(a_1^2 + a_2^2)$, $a_1 = V_{DD} - \frac{1}{2}V_{SS} - \frac{1}{2}V_i - V_T$ and $a_2 = \frac{1}{2}V_{SS} + \frac{1}{2}V_i - V_T$.

From eqn. (2.25), since this second term is not desired in the output of a squaring circuit, it contributes to the amount of distortion or error introduced by the circuit. The last term is an undistorted reproduction of the square of the input signal and this is the desired output signal. The second term can be reduced or eliminated completely by satisfying the condition a_2 - a_1= 0. We can found that this circuit can function as voltage squaring circuit.

The circuit is shown in Fig. 2.8 that has been proposed in [7], is the current mode squarer circuit. This work is the one of the method that realized by using the square law characteristic of MOS transistor where all transistors are biased in saturation region. The circuit structure is simple and provides good accuracy over a wide range of input currents. Therefore, in this thesis, the current squarer circuit as shown in Fig. 2.8 has been used for designing the proposed true rms to dc converter. The circuit structure composes of two current mirrors and the output current is the function of the square input current and DC bias current. This current squarer circuit description will be outlined in this section.

2.2.1 Circuit Description

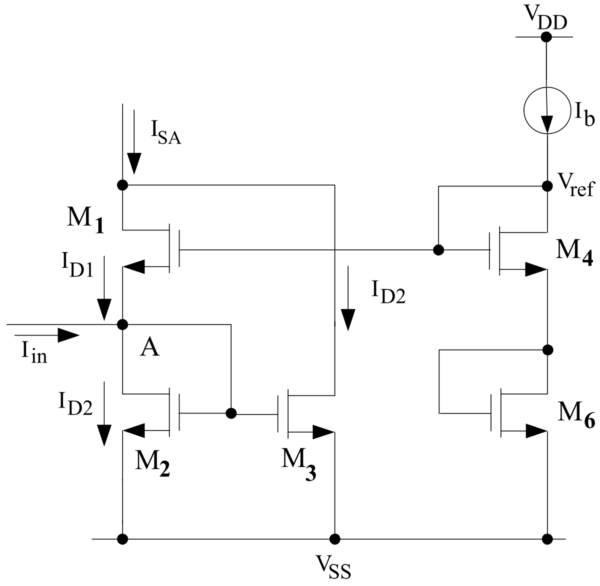

Fig. 2.8 CMOS current squarer circuit

The operation of the CMOS current squarer circuit of the Fig. 2.8 is based on the square law characteristic of MOS transistors biased in the saturation region [31], [32]. Transistors M_1 through M_3 function as a current squarer, where M_4 and M_6 and the current source I_b formed as the current-controlled bias circuit. The input signal current I_{in} is injected into point A. From the squarer circuit in Fig. 2.8, consider the transistor M_1, M_3, M_4 and M_6, we will obtain

$$V_{GS4} + V_{GS6} = V_{GS1} + V_{GS3} \tag{2.26}$$

Assume all MOS transistors are biased in the saturation region, the square-law behavior for the current –voltage relationship of the MOS transistor in saturation is assumed as

$$I_D = K\left(V_{GS} - V_T\right)^2 \tag{2.27}$$

where V_{GS} can be expressed as

$$V_{GS} = \sqrt{\frac{I_D}{K}} + V_T \tag{2.28}$$

from eqns. (2.26) and (2.28), set $V_{T1} = V_{T2} = V_{T4} = V_{T6} = V_T$ and $K_1 = K_2 = K_4 = K_6 = K$ and from circuit analysis $I_{D4} = I_{D6} = I_b$, therefore

$$2\sqrt{I_b} = \sqrt{I_{D1}} + \sqrt{I_{D3}} \tag{2.29}$$

squaring the eqn. (2.29) given

$$4I_b = I_{D1} + 2\sqrt{I_{D1}I_{D2}} + I_{D2} \tag{2.30}$$

From routine circuit analysis, the relation between I_{D1}, I_{D2} and I_{in} can be expressed as

$$I_{D1} = I_{D2} - I_{in} \tag{2.31}$$

or

$$I_{D2} = I_{D1} + I_{in} \tag{2.32}$$

From eqns. (2.30) and (2.31) , we will obtain

$$2\sqrt{I_{D2}^2 - I_{in}I_{D2}} = 4I_b + I_{in} - 2I_{D2} \tag{2.33}$$

By squaring eqn. (2.33) , the drain current of transistor M_2, (I_{D2}) can be written as

$$I_{D2} = \frac{16I_b^2 + 8I_bI_{in} + I_{in}^2}{16I_b} \tag{2.34}$$

Eqn. (2.34) can be rewritten as

$$I_{D2} = \frac{\left(4I_b + I_{in}\right)^2}{16I_b} \quad , \left|I_{in}\right| \le 4I_b \tag{2.35}$$

From eqns. (2.29) and (2.34) , the drain current of transistor M_1, (I_{D1}) can be written as

$$I_{D1} = \frac{16I_b^2 - 8I_bI_{in} + I_{in}^2}{16I_b} \tag{2.36}$$

or

$$I_{D1} = \frac{\left(4I_b - I_{in}\right)^2}{16I_b} \quad , \left|I_{in}\right| \leq 4I_b \tag{2.37}$$

The unity gain positive current mirror CM_1, formed by M_2 and M_3, reflects the current I_{D2} in order to add with the current I_{D1}. Then, from eqns. (2.35) and (2.36), the summation of the currents I_{D1} and I_{D2} or $I_{SA} = I_{D1}+I_{D2}$ becomes

$$I_{SA} = I_{D1} + I_{D2} \tag{2.38}$$

Replace I_{D1} and I_{D2} in eqn. (2.32) with I_{D1} and I_{D2} from eqns. (2.34) and (2.36) respectively , I_{SA} can be rewritten as

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \tag{2.39}$$

We can see that I_{SA} consists of the signal current which is the squaring of the input signal I_{in} and the DC current $2I_b$. If the DC current $2I_b$ can be compensated, the circuit will be functioned as a squarer/divider circuit, which can be used as a basic cell to realize rms-to-dc converter by the implicit computation method in this thesis.

2. 3 A balanced CMOS OTA

An operational transconductance amplifier (OTA), also called a transconductance element or a transconductance, is a device that converts voltage inputs to current outputs (or a voltage controlled current source) such that $i_{out} = g_mV_{in}$. The transconductance gain g_m can usually be varied over a wide range by adjusting an external DC bias current I_B.

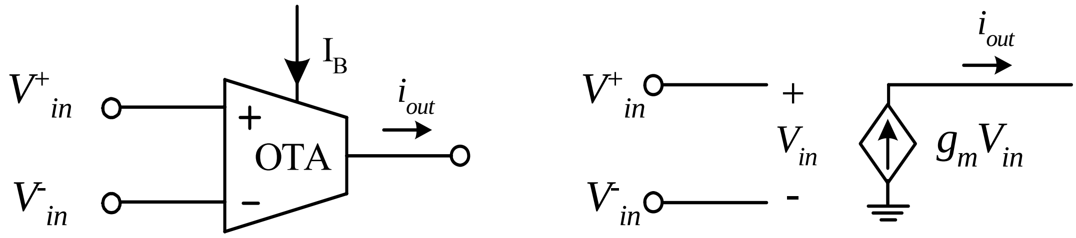

Fig. 2.9 Ideal model of the operational transconductance amplifier (OTA)

In Fig. 2.9, the small-signal model for an ideal OTA is seen to be a differential input voltage-controlled current source (VCCS), with infinite input and infinite output impedances. An OTA is a voltage controlled current source, more specially the term "operational" comes from the fact that it takes the difference of two voltages as the input for the current conversion. The ideal transfer characteristic is therefore

$$i_{out} = g_m \left(v_{in}^{+} - v_{in}^{-} \right) \tag{2.40}$$

or, by taking the pre-computed difference as the input,

$$i_{out} = g_m v_{in} \tag{2.41}$$

with the ideally constant transconductance g_m as the proportional factor between the two. In practice the transconductance is also a function of the input differential voltage, as we will later see.

In the literature, many design techniques have been proposed for realizing the operational transconductance amplifier. For CMOS-based OTA, a well-known practical linearization technique for transconductors is source degeneration [33]-[35] and by using cross-coupled differential pairs operating in saturation, e.g. [36]-[40]. Some of these realizations are not intended for low-power usage, others have problems with the body effect and/or channel length-modulation. In addition an interesting approach of a low-power linear OTA working in the non-saturation region has been proposed in [41]. However a double supply voltage and matching of a p-type and n-type OTA is needed. As a matter of principle the transconductances for positive and negative input voltages do not match exactly.

In this thesis, a balanced CMOS OTA has been used for realizes the transconductor which can be electronically and linearly tuned. The circuit structure is composed of a *V/I* converter (or differential amplifier) and three current mirrors. The circuit description will be described. Firstly a simple CMOS OTA will be introduced.

In Fig. 2.10 a simple CMOS OTA is shown, the simple CMOS OTA consists of a self-bias MOS transistor differential stage with active load. Transistors M_1 and M_2 form a matched transistor pair. Transistors M_3 and M_4 have equal W/L, as well. All current levels are determined by current source I_B, half of which flows through M_1 and M_3, with the other half flow through M_2 and M_4.

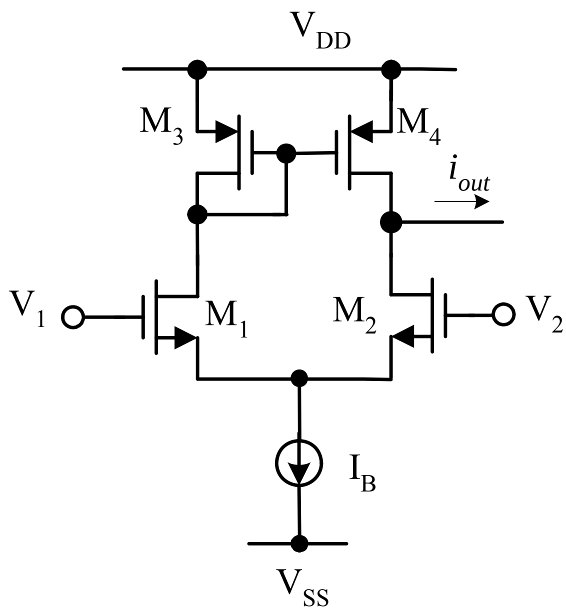

Fig. 2.10 A simple CMOS OTA

At low frequency, the transconductance of the OTA is given by $G_m = g_{m1} = g_{m2}$. It is also given by

$$G_m = \sqrt{2I_B K} \tag{2.42}$$

in which $K = \mu_n C_{ox} W/2L$ is the transconductacne parameter for MOS transistor in saturation. Also note that the current I_B in eqn.(2.42) is the total current, which is twice the current through one transistor.

For the structure of this simple CMOS OTA, their input stage consists of a differential pair loaded by a current mirror. This load is thus very asymmetrical due to only M_3 is connected as a diode that causes V_{DS3} fixed, whereas V_{DS4} is varied up to load. Therefore, the DC current which flows through M_1, M_3, and the other one flowing through M_2, M_4 are unbalance. From this result, the symmetrical CMOS OTA or balanced CMOS OTA is preferred for the circuit design in thesis, which provides the same load to both input devices.

Simple balanced CMOS OTA

The circuit schematic of the balanced CMOS OTA with symmetrical input stage is given in Fig. 2.11. The differential pair is formed by the input transistors M_1 and M_2. They drive their output currents in two transistors, M_3 and M_5, which are connected as diodes. They are the inputs of two current mirrors with current multiplication factor (current mirror ratio). The output current of transistor M_4 is then mirrored once more in current mirror M_7, M_8, with the unity gain current mirror, as indicated. In addition, for the balanced OTA structure, current mirrors constructed of transistor M_3-M_4 and M_5-M_6 will force the drain voltage V_{DS1} of transistor M_1 equal to V_{DS2} of transistor M_2.

2.3.1 Circuit Descriptions of a balanced CMOS OTA

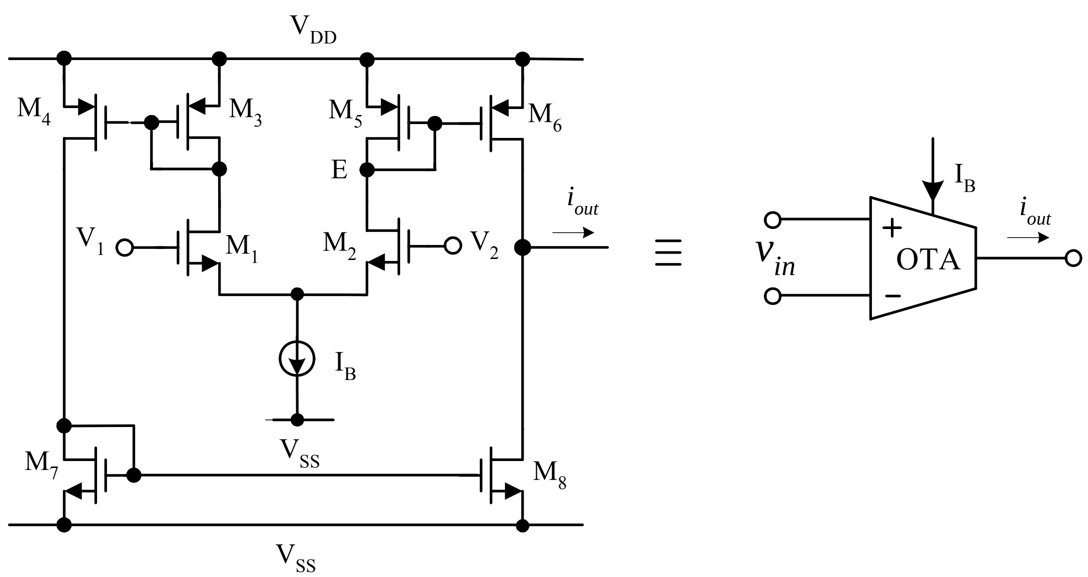

Fig. 2.11 Schematic diagram of a balanced CMOS OTA

For the purpose of the following analysis, we will assume that all MOS devices operate in the saturation region. This means that the transistor drain current I_D is characterized by a square-law model as

$$I_D = \begin{cases} K(V_{GS} - V_T)^2 & , \ for \ V_{GS} > V_T \\ 0 & , \ for \ V_{GS} \le V_T \end{cases} \tag{2.43}$$

where the transconductance parameter $K = \mu_n C_{ox} W/2L$, μ_n is the mobility of the carrier, C_{ox} is the gate-oxide capacitance per unit area, W is the effective channel width, L is the effective channel length, and V_{GS} and V_T are the gate-to-source and threshold voltages, respectively.

If we let V_{in} is the differential input voltage (V_{in}=V_1-V_2), i_{out} is the output current and I_B is the bias current. Let us assume that M_1 and M_2 are perfectly matched and the current mirrors have unity current gain. By using eqn. (2.43), the differential output current of the circuit in Fig. 2.11 can be given by [42]

$$\begin{aligned} i_{out} &= i_2 - i_1 \\ &= \sqrt{2I_B K} \cdot V_{in} \cdot \sqrt{1 - \frac{KV_{in}^2}{2I_B}} \ , \quad for -\sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \end{aligned} \tag{2.44}$$

The transconductance gain (g_m) of the MOS coupled pair can be derived by taking the derivative of (2.44) with respect to V_{in}, yielding

$$g_m = \left. \frac{di_{out}}{dV_{in}} \right|_{V_{in}=0} = \sqrt{2I_B K} \ , \qquad for -\sqrt{\frac{I_B}{K}} \le V_{in} \le \sqrt{\frac{I_B}{K}} \tag{2.45}$$

From the eqn. (2.44), the current i_{out} can rewritten as

$$i_{out} = g_m V_{in} = \sqrt{2I_B K} \cdot V_{in} \tag{2.46}$$

Eqn. (2.45) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_B, but in the form of square root function. In addition, in order to operate in the low distortion range, the input voltage V_{in} should be in the range of [20]

$$V_{in} \leq \left|\sqrt{I_B / K}\right| \qquad (2.47)$$

Moreover, Fig. 2.12 is a multiple current output or fully differential OTA . As shown in dashed-line the multiple current outputs OTA can be implemented by current replicas using current mirrors formed by transistors M_9-M_{12}. However, the method that uses two OTAs in parallel input terminals to produce multiple outputs can also be used [43].

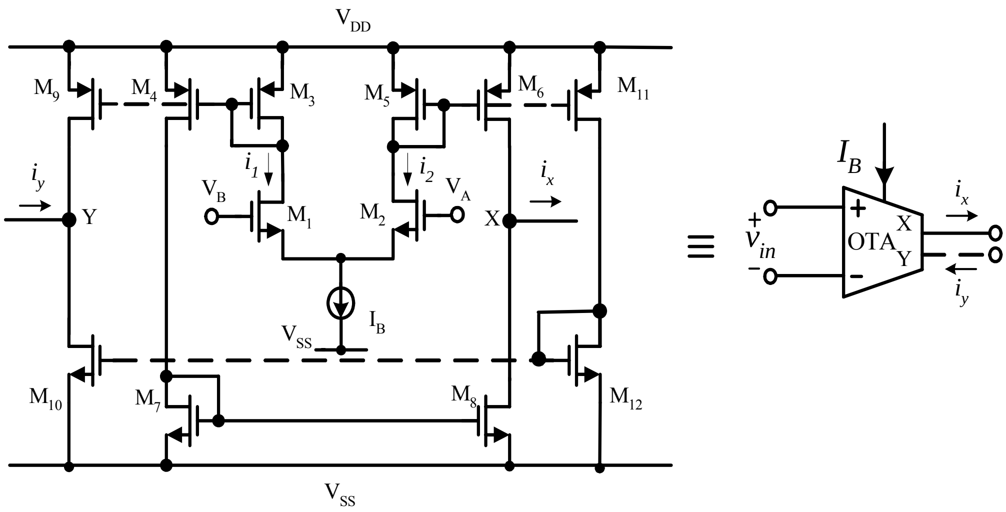

Fig. 2.12 Schematic diagram of the fully differential CMOS OTA

Where v_{in} is the differential input voltage ($v_{in}=V_A-V_B$), I_x is the output current and I_B is the bias current. The differential output current of the circuit of Fig. 2.12 can be given by

$$i_x = i_2 - i_1 = \sqrt{2I_B K} \cdot v_{in} \cdot \sqrt{1 - \frac{K v_{in}^2}{2I_B}} \;, \quad for - \sqrt{\frac{I_B}{K}} \leq v_{in} \leq \sqrt{\frac{I_B}{K}} \qquad (2.48)$$

The transconductance gain (g_m) of the fully differential OTA can be derived by taking the derivative of (2.48) with respect to v_{in}, yielding

$$g_m = \left.\frac{di_x}{dv_{in}}\right|_{v_{in}=0} = \sqrt{2I_B K} \qquad (2.49)$$

Thus we can obtain the following equation for a small signal;

$$i_x = g_m v_{in} = \sqrt{2I_B K} \cdot v_{in} \tag{2.50}$$

Eqn. (2.49) shows that the transconductance gain (g_m) of the OTA can be varied by the bias current I_B, but in the form of a square root function. It should be noted that the transconductance gain (g_m) of the balance CMOS OTA shown in Fig. 2.11 will provide low harmonic distortion if the input voltage is limited in the range of

$$g_m = \sqrt{2I_B K}, \quad for -\sqrt{\frac{I_B}{K}} \le v_{in} \le \sqrt{\frac{I_B}{K}} \tag{2.51}$$

The effect from the non-ideality can be studied through the use of the OTA small signal model that shown in the Fig. 2.13,

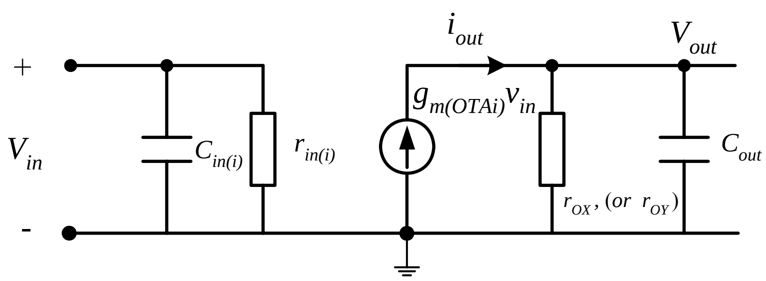

Fig. 2.13 Small signal model of a balanced CMOS OTA

where $r_{in(i)}$ is the input resistance of OTAi, r_{OX} or r_{OY} is the different output resistance at port X or port Y, $C_{in(i)}$ is the input capacitance of OTAi and $C_{out(i)}$ is the output capacitance of OTAi [20],[25],[26]. The differential output resistance r_{OX} is approximately equal to the output resistance of the current mirror M_5-M_6 in parallel with the output resistance of the current mirror M_7-M_8 or r_{OX} approximate $1/(g_{d6}+g_{d8})$ and , similarly, r_{OY} approximate $1/(g_{d9}+g_{d10})$