APPENDIX A

Large signal analysis of the squaring circuit [32]

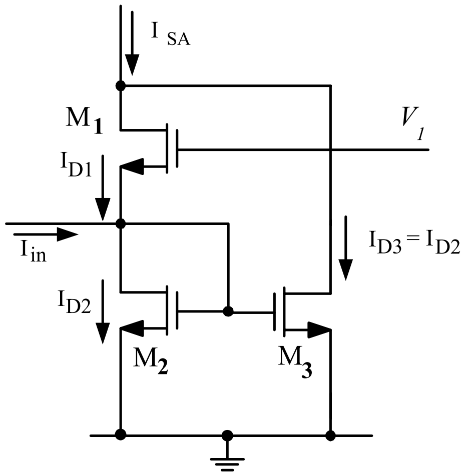

Fig. 1A The current squaring circuit

Consider two matched MOS transistors which include the effect of channel-length modulation (λ), operating in saturation and characterized to first order by

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L} \left(V_{GS1} - V_{T1}\right)^2 \left(1 + \lambda V_{DS1}\right) \tag{A.1}$$

$$I_{D2} = \frac{\mu_n C_{ox} W}{2L} (V_{GS2} - V_{T2})^2 \left(1 + \lambda V_{DS2}\right) \tag{A.2}$$

By copying of I_{D2} via transistor M_3 and adding it to current I_{D1}, the sum current I_{D1}+ I_{D3} is available as output current I_{SA} of squaring part

$$I_{SA} = I_{D1} + I_{D3} \tag{A.3}$$

From the unity gain current mirror CM_1, I_{D3} can be expressed in the function of I_{D2} as

$$I_{D3} = \frac{(W/L)_3}{(W/L)_2} \left(\frac{V_{GS3} - V_{T3}}{V_{GS2} - V_{T2}} \right)^2 \cdot \frac{1 + \lambda V_{DS3}}{1 + \lambda V_{DS2}} \cdot \frac{\mu_{n3} C_{ox3}}{\mu_{n2} C_{ox2}} I_{D2} \tag{A.4}$$

If the effect of channel-length modulation can be neglected ($\lambda = 0$), assume the process parameters such as V_T, μ_n , C_{ox}, of MOS transistor are matched and $V_{DS2} \cong V_{DS1}$. The eqns. (A.1) and (A.2) can be rewritten as

$$I_{D1} = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS1} - V_{T1}\right)^2 \tag{A.5}$$

$$I_{D2} = \frac{\mu_n C_{ox} W}{2L}(V_{GS2} - V_{T2})^2 \tag{A.6}$$

$$V_{GS1} = V_1 - V_{GS2} \tag{A.7}$$

where V_1 is bias voltage at transistor M_1 , and V_{GS1}, V_{GS2} are the gate-source voltage of transistor M_1 and M_2 respectively.

Using simple algebra we may write for the output current difference

$$I_{D2} - I_{D1} = \frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)\left(V_{GS2} - V_{GS1}\right) \tag{A.8}$$

With (A.3), (A.5) - (A.7), the sum of the output currents may be written as

$$I_{D2} + I_{D1} = \frac{1}{2}\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2 + \frac{\left(I_{D1} - I_{D2}\right)^2}{2\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2} \tag{A.5}$$

By copying of I_{D2} via transistor M_3 and adding it to current I_{D1} , the sum current I_{D1}+ I_{D3} is available as output current I_{SA} of squaring part

$$I_{SA} = I_{D1} + I_{D3} = I_{D1} + I_{D2} \tag{A.6}$$

From Fig. A1, the common node of M_1 and M_2 is now considering as input. The input current can be written as

$$I_{in} = I_{D2} - I_{D1} \tag{A.7}$$

Substitution of (A.7) and (A.6) in (A.5) yields

$$I_{SA} = \frac{1}{2}\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2 + \frac{I_{in}^2}{2\frac{\mu_n C_{ox} W}{2L}\left(V_1 - 2V_T\right)^2} \qquad \text{(A.8)}$$

which describes a current squaring function. Using the bias circuit, formed by transistors M_4 and M_6 , to combination with the current squaring in Fig. A1 which shown in Fig. 2.8, a simpler expression is obtained

$$I_{SA} = 2I_b + \frac{I_{in}^2}{8I_b} \qquad \text{(A.9)}$$

Biasing with a current has the additional advantage of making the transfer function (in first-order approximation) independent of process parameters and operating temperature.

From the current controlled biasing circuit (M_4 and M_6). We found that the relation between the control current I_b and the voltage V_1 is given by [2.15]

$$I_b = \frac{1}{4}K(V_2 - 2V_T) \qquad \text{(A.10)}$$

where $K = \dfrac{\mu_n C_{ox} W}{2L}$

From equation (A.8), in order to remain a proper operation, the input current is restricted to the range

$$\left|I_{in}\right| < K(V_2 - 2V_T)^2 \qquad \text{(A.11)}$$

or, if biased with the biasing circuit

$$\left|I_{in}\right| < 4I_b \qquad \text{(A.12)}$$

APPENDIX B

Conversion error of the squaring circuit

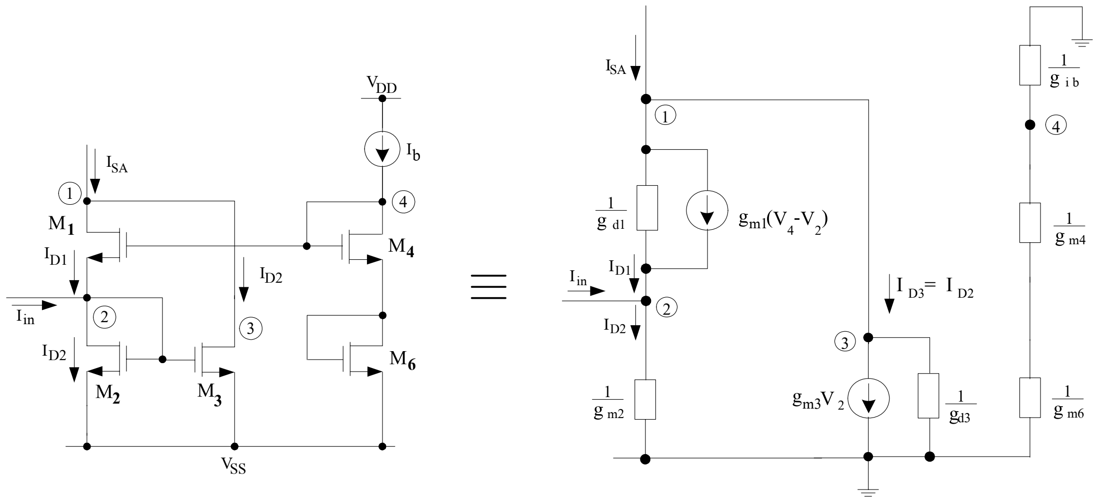

Fig. 1B Squaring circuit (a) Circuit diagram, (b) Small-signal equivalent circuit.

By using KCL analysis, transfer function of the input small signal current (i_{in}) and the output current (i_{SA}) of the squaring circuit in Fig. 1B can be expressed below.

From Fig. 1B(b) using KCL at node 2 , the equation is shown.

$$i_{in} + \left[g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) \right] = g_{m2}v_2 \quad \text{(B.1)}$$

using KCL at node 1

$$i_{SA} = g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) + g_{m3}v_2 + g_{d3}v_3 \quad \text{(B.2)}$$

If $g_m >> g_d$ from equations (B.1) and (B.2) the conversion of the input signal current I_{in} to the current I_{SA} from the squaring part can be approximately expressed as

$$\alpha = \frac{i_{SA}}{i_{in}} = \frac{1}{1 + \dfrac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}}} \quad \text{(B.3)}$$

where g_{di} and g_{mi} denote the drain conductance and the conductance of the transistor M_i, respectively. The input current i_{in} will accurately convert to i_{SA} if $\alpha \approx 1$. The percentage conversion error of the squaring circuit can be written as

$$\frac{\delta\alpha}{\alpha} = \frac{g_{d1}(g_{m2} + g_{m3})}{g_{m1}g_{m3} + g_{m2}g_{m3} - g_{m1}^2 - g_{m1}g_{m2} - g_{m1}g_{d1} - g_{m2}g_{d1}} \times 100\% \quad \text{(B.4)}$$

APPENDIX C

Frequency response of true RMS to DC converter

Consider the frequency response of the true rms-to-dc converter. Because of the circuit is composed of the squaring circuit in combination with four current mirrors (CM_2 through CM_5). Thus we should pay attention on the frequency response of the squaring circuit and the current mirrors.

To verify the high frequency response, from the block diagram of Fig. 3.1, the transfer function of the proposed rms-to-dc converter circuit can be given by

$$\frac{i_{RMS}(s)}{i_{in}(s)} = \frac{i_{SA}(s)}{i_{in}(s)} \cdot \frac{i_{SQ}(s)}{i_{SA}(s)} \cdot \frac{i_{b1}(s)}{i_{SQ}(s)} \cdot \frac{i_{RMS}(s)}{i_{b1}(s)} \tag{C.1}$$

The small signal equivalent circuit of the squaring circuit from and the positive current mirror CM4 and the negative current mirror CM3, can be represented in Fig. 1C (b), 2C (b) and 3C (b), respectively.

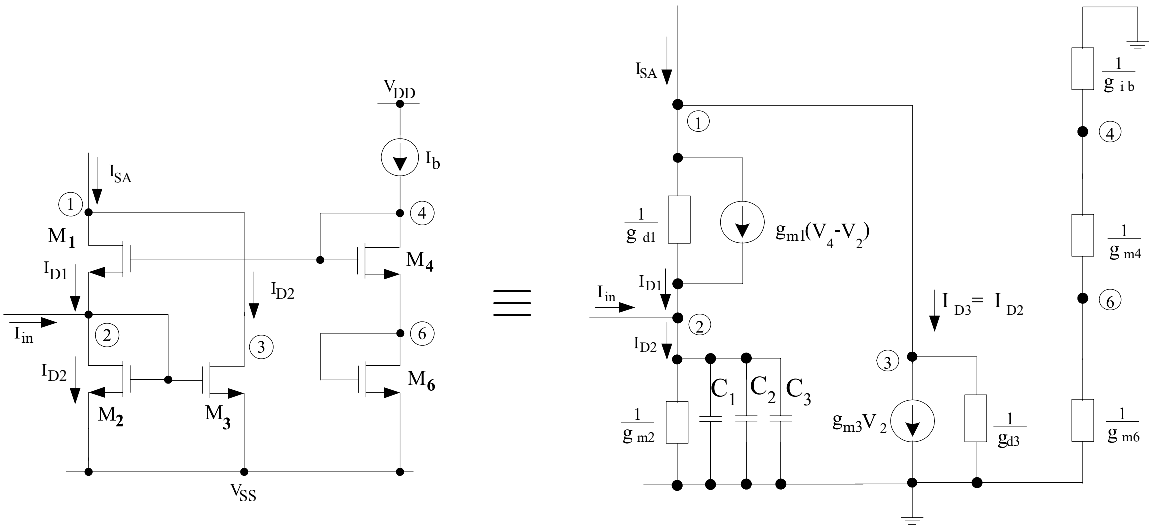

Fig. 1C Squaring circuit (a) Circuit diagram, (b) Small-signal equivalent circuit.

By using KCL analysis, transfer function of the input signal current (I_{in}) and the output current (I_{SA}) of the squaring circuit in Fig. 1C can be expressed below.

From Fig. 1C(b) using KCL at node 2 , the equation is shown.

$$i_{in} + \left[g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) \right] = \left[g_{m2} + s\left(C_1 + C_2 + C_3\right) \right] v_2 \quad \text{(C.2)}$$

using KCL at node 1

$$i_{SA} = g_{d1}\left(v_1 - v_2\right) + g_{m1}\left(v_4 - v_2\right) + g_{m3}v_2 + g_{d3}v_3 \qquad \text{(C.3)}$$

If $g_m >> g_d$ from equations (C.2) and (C.3) the transfer function $i_{SA}(s)/i_{in}(s)$ of the squaring circuit in Fig.1C can be approximately expressed as

$$\frac{i_{SA}(s)}{i_{in}(s)} = \frac{\dfrac{g_{m3} - g_{m1}}{\left(C_1 + C_2 + C_3\right)}}{\left(s + \dfrac{g_{m1} + g_{m2}}{\left(C_1 + C_2 + C_3\right)}\right)} \qquad \text{(C.4)}$$

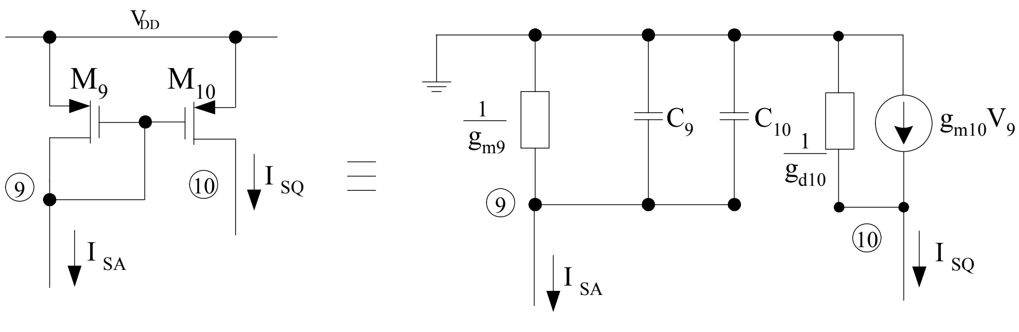

Fig. 2C Current mirror (CM4) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 2C , using KCL at node 9, the equation can be shown.

$$\left[g_{m9} + s\left(C_9 + C_{10}\right) \right] v_9 = -i_{SA} \qquad \text{(C.5)}$$

using KCL at node 10,

$$-i_{SQ} = g_{m10}v_9 + g_{d10}v_{10} \tag{C.6}$$

If $g_m >> g_d$ from equations (C.5) and (C.6) the transfer function $i_{SQ}(s)/i_{SA}(s)$ of the current mirror (CM4) in Fig. 2C can be expressed as

$$\frac{i_{SQ}(s)}{i_{SA}(s)} = \frac{g_{m10}/g_{m9}}{\left(1 + s\dfrac{C_9 + C_{10}}{g_{m9}}\right)} \tag{C.7}$$

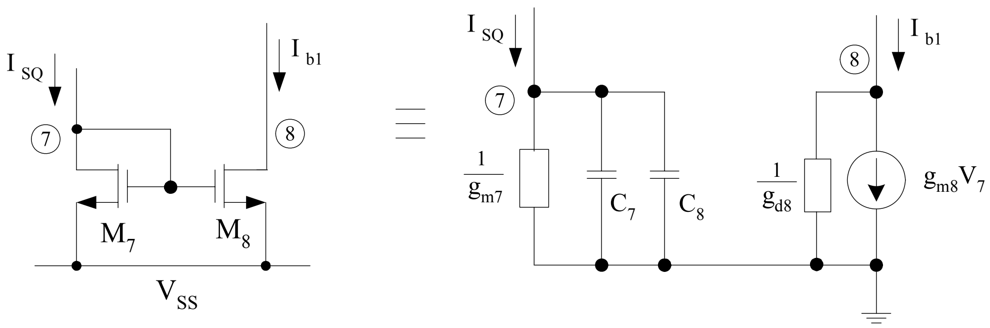

Fig. 3C Current mirror (CM3) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 3C, using KCL at node 7, the equation can be shown.

$$\left[g_{m7} + s\left(C_7 + C_8\right)\right]v_7 = i_{SQ} \tag{C.8}$$

using KCL at node 8,

$$i_{b1} = g_{m8}v_7 + g_{d8}v_8 \tag{C.9}$$

If $g_m >> g_d$ from equations (C.8) and (C.9) the transfer function $i_{b1}(s)/i_{SQ}(s)$ of the current mirror (CM3) in Fig. 3C can be expressed as

$$\frac{i_{b1}(s)}{i_{SQ}(s)} = \frac{g_{m8}/g_{m7}}{\left(1+s\dfrac{C_7+C_8}{g_{m7}}\right)} \tag{C.10}$$

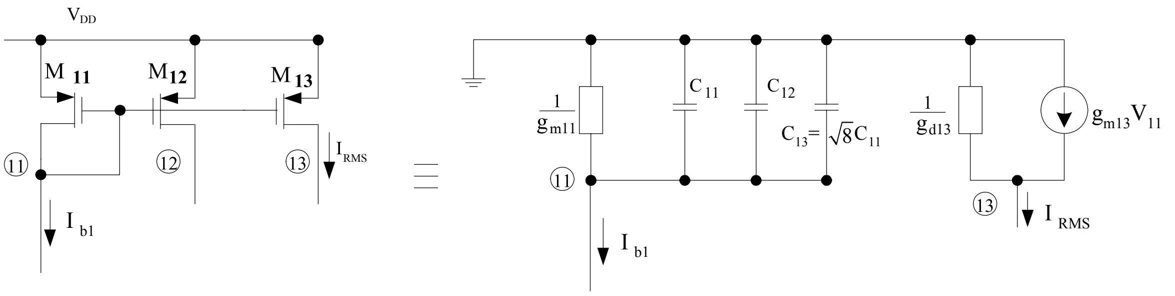

Fig. 4C Current mirror (CM_5) (a) Circuit diagram, (b) Small-signal equivalent circuit.

From Fig. 4C , using KCL at node 11, the equation can be shown.

$$\left[g_{m11}+s\left(C_{11}+C_{12}+C_{13}\right)\right]v_{11} = i_{b1} \tag{C.11}$$

using KCL at node 13,

$$i_{RMS} = g_{m13}v_{11} + g_{d13}v_{13} \tag{C.12}$$

If $g_m >> g_d$ from equations (C.11) and (C.12) the transfer function $i_{b1}(s)/i_{SQ}(s)$ of the current mirror (CM5) in Fig. 4C can be expressed as

$$\frac{i_{RMS}(s)}{i_{b1}(s)} = \frac{g_{m13}/g_{m11}}{\left(1+s\dfrac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \tag{C.13}$$

By a small signal analysis of the proposed true RMS-to-DC converter, the transfer function of the circuit can be approximated as

$$\frac{i_{RMS}(s)}{i_{in}(s)}=\frac{(g_{m3}-g_{m1})/(g_{m1}+g_{m2})}{\left(1+s\frac{C_1+C_2+C_3}{g_{m1}+g_{m2}}\right)}\cdot\frac{g_{m10}/g_{m9}}{\left(1+s\frac{C_9+C_{10}}{g_{m9}}\right)}\cdot\frac{g_{m8}/g_{m7}}{\left(1+s\frac{C_7+C_8}{g_{m7}}\right)}\cdot\frac{g_{m13}/g_{m11}}{\left(1+s\frac{C_{11}+C_{12}+C_{13}}{g_{m11}}\right)} \tag{C.14}$$

Let p_1 denotes the pole of the squaring circuit, p_2 is the pole of the current mirror CM4, p_3 is the pole of the lowpass filter, and p_4 is the pole of the current mirror CM_5. Then from eqn. (C.14), the poles p_1, p_2, p_3 and p_4 can be respectively expressed as

$$p_1=-\frac{g_{m1}+g_{m2}}{C_1+C_2+C_3} \tag{C.15}$$

$$p_2=-\frac{g_{m9}}{C_9+C_{10}} \tag{C.16}$$

$$p_3=-\frac{g_{m7}}{C_7+C_8} \tag{C.17}$$

$$p_4=-\frac{g_{m11}}{C_{11}+C_{12}+C_{13}} \tag{C.18}$$

High frequency limitation is due to the pole p_4 that associated with the PMOS current mirror (CM_5). The cut-off frequency of the rms-to-dc converter can be given by

$$f_{-3dB}=\frac{(g_{m11})}{2\pi(C_{11}+C_{12}+C_{13})} \tag{C.19}$$

APPENDIX D

Error Analysis of the RMS value

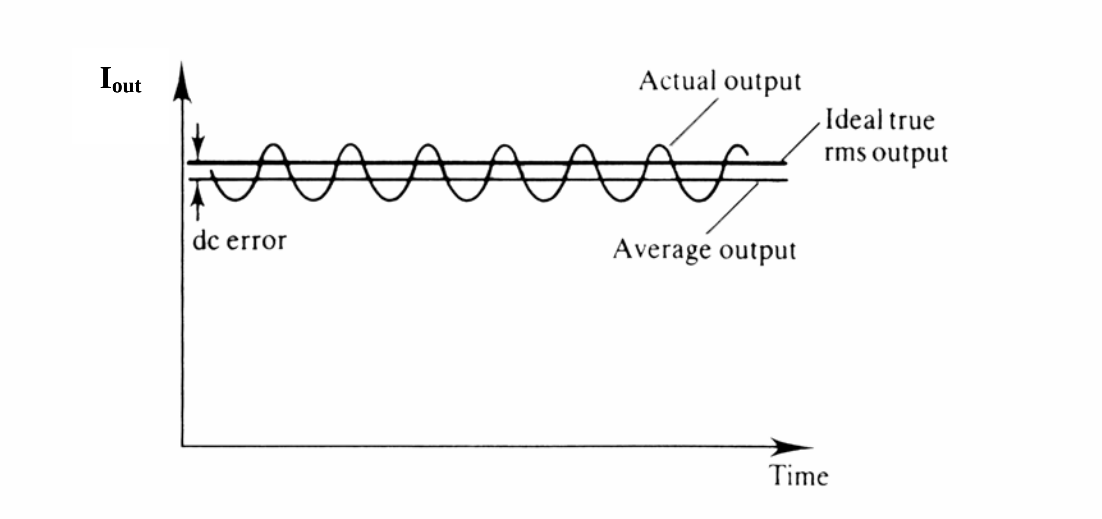

Fig. 1D Output waveform for sinusoidal input current

Since the RMS current value (I_{RMS}) is expressed as

$$I_{RMS} = \sqrt{\frac{1}{\tau}\int_0^{\tau} I_{in}^2 dt} \tag{D.1}$$

From equation C.1 the transfer function of the true RMS-to-DC converter can be written as

$$I_{out}^2(s) = \frac{I_{in}^2(s)}{(1+s\tau)} \tag{D.2}$$

where τ is equal to RC. Suppose that the input current is given by

$$I_{in} = \sqrt{2} I_{RMS} \cos(\omega t) \tag{D.3}$$

where I_{RMS} is the RMS value of the sinusoidal input signal of angular frequency ω. The output current as a function of the input frequency is

$$I_{out}\left(t\right)=\sqrt{I_{RMS}\left(1+\frac{\cos\left(2\omega t\right)}{\sqrt{1+4\omega^{2}\tau^{2}}}\right)} \tag{D.4}$$

Using a simple trigonometric and Taylor series approximation and by assuming that the frequency of input current is greater than the inverse of the averaging time constant τ (or $f > 1/\tau$), I_{out}(t) of equation (D.4) can be given by

$$I_{out}\left(t\right)=I_{RMS}\left[1-\frac{1}{16\left(1+4\omega^{2}\tau^{2}\right)}+\frac{I_{RMS}\cos\left(2\omega t\right)}{2\sqrt{1+4\omega^{2}\tau^{2}}}\right] \tag{D.5}$$

From this it is seen that there is both a dc error and an ac error in the output. The dc error e_{odc} can by expressed as

$$e_{odc}=\frac{I_{RMS}}{2\left[1+4\omega^{2}\tau^{2}\right]} \quad , \quad \omega>\frac{1}{\tau} \tag{D.6}$$

and from equation (D.6) the ac error in the output current, the output ripple e_{ripple} , is essentially

$$e_{ripple}=\frac{I_{RMS}\cos 2\omega t}{2\left[1+4\omega^{2}\tau^{2}\right]^{1/2}} \quad , \quad \omega>\frac{1}{\tau} \tag{D.7}$$

since the fourth-harmonic ripple term is much less than the second-harmonic term with $\omega > 1/\tau$. The ripple error in the output can be reduced in many applications with a simple low-pass filter, but an error in the output dc level e_{odc} will still exist.