Thesis Title	On the Design of Low-Voltage, Voltage Mode Minimum and Maximum Circuit with Threshold Voltage Cancellation in CMOS Technology
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ABSTRACT

This thesis proposes on the design of low-voltage, voltage mode minimum and maximum circuit. The proposed circuit is realized by sub-circuits such as voltage level-shifter and shunt feedback buffer circuits. This achieved circuit has a simple scheme with minimum components at ±1.5Volts power supply, input dynamic range of ±600mV is achieved. Performance including the DC-characteristic, high-frequency response are carried out by PSpice.