Suthida Preechadech 2010: Prediction of Silicon Wafer Lapping Time by Artificial Neural Network. Master of Engineering (Industrial Engineering), Major Field: Industrial Engineering, Department of Industrial Engineering. Thesis Advisor: Mr. Chana Raksiri, D.Eng. 139 pages.

Lapping time of silicon wafer is predicted by artificial neural network is the objective of this research. There are five inputs and one output for proposing neural network architecture. Further the numbers of neuron in hidden layer are varied to obtain minimization of error prediction by artificial neural network. This artificial neural network is based on Backpropagation neural network. Levenberg-Marquardt training algorithm is applied to train the design network for optimum weight and bias network with all trained inputs data. The results show the final architecture neural network consists of five neurons in input layer, fifty-five neurons in hidden layer and one neuron in output layer (5-55-1). Transfer functions in hidden and output layer are Log-sigmoid and Linear function respectively. In addition, the network Mean Square Errors (MSE) of training process and testing process are 0.0164 and 0.0398 respectively. Moreover, the network Efficiency Index (EI) of testing process is 87.97%. The results show silicon wafer lapping time can be predicted by proposing neural network architecture.

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