เอกสารอ้างอิง

1. Xilinx Inc., *"Virtex-II proDeverlopment System: Data Sheet"*. 2009.
2. J D. J. C. MacKay and R. M. Neal, "Near Shannon limit performance of low-density parity check codes," *Electron. Lett.*.vol. 32, p. 1645, 1996.
3. Draft STANDARD for Information Technology – Telecommu-nications and information exchange between systems - Local and metropolitan area networks - Specific requirements-, IEEE P802.11n./D3.00, Sept. 2007.
4. Xin-Yu Shih, Cheng-Zhou Zhan, Cheng-Hung Lin, and An-Yeu (Andy) Wu, "An 8.29 mm^2 52 mW Multi-Mode LDPC Decoder Design for Mobile WiMAX System in 0.13 μm CMOS Process," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, March 2008.
5. M. Karkooti, P. Radosavljevic, and J. R. Cavallaro, "Configurable LDPC Decoder Architectures for Regular and Irregular Codes," *J. Signal Processing Systems,* vol. 53, pp. 73-88, October 2008.
6. Hiroyuki SHIMAJIRI, Akifumi HAYASHI and Takeo YOSHIDA, "RTL design of LDPC decoder for IEEE802.11n WLAN," *ISCIT 2009. 9th International Symposium on Communications and Information Technology,* 2009, Sep. 2009, pp. 302-307.

ภาคผนวก

ดัชนี

สำนักงานคณะกรรมการวิจัยแห่งชาติ ห้องสมุดงานวิจัย

A

Analog information, 31
approximation, 25

C

Carry Propagate Adder, 30
Carry save adder, 30
closure, 9
CNUs Unit, 37
Control Unit, 42
Convolution code, 7

D

Decision, 46
de-permutation, 36
Digital information, 31

E

Encoder, 6

F

Forward error correction, 1
FPGA, 42

G

generator matrix, 9

H

Hamming bound, 12
Hamming weight, 13

I

Input Buffer Unit, 40
Irregular LDPC codes, 16
iteration, 35

L

Linear block code, 7
linear property, 8
Log Likelihood Ratios, 22

M

Memmory Unit, 41
Min-Sum Algorithm, 25
Modified Min-Sum Algorithm, 28

N

Noise, 7

O

OutputBuffer Unit, 40

P

parity-check matrix, 11
permutation, 36

R

Regular LDPC codes, 14
reorder parity check matrix, 29
RTL, 36

S

scaling factor, 28
soft iterative decoding, 18
Sum-Product Algorithm, 20

T

Tanner, 19

V

VNUs Unit, 38

X

Xilinx, 48
XOR, 38

ค

ค่าซินโดรม, 11