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Design and Simulation of Reversible Time-Synchronized Quantum-Dot Cellular Automata Combinational Logic Circuits with Ultralow Energy Dissipation

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Abstract

The quantum-dot cellular automata (QCA) represent emerging nanotechnology that is poised to supersede the current complementary metal-oxide-semiconductor digital integrated circuit technology. QCA constitutes an extremely promising transistor-less paradigm that can be downscaled to the molecular level, thereby facilitating tera-scale device integration and extremely low energy dissipation. Reversible QCA circuits, which have reversibility sustained down from the logical level to the physical level, can execute computing operations dissipating less energy than the Landauer energy limit (kBTln2). Time synchronization of logic gates is an essential additional requirement, especially in cases involving complex circuits, for ensuring accurate computational results. This paper reports the design and simulation of eight new both logically and physically reversible time-synchronized QCA combinational logic circuits. The new circuit design presented here mitigates the clock delay problems, which are caused by the non-synchronization of logic gate information, via the use of an inherently more symmetric circuit configuration. The simulation results confirm the behaviour of the proposed reversible time-synchronized QCA combinational logic circuits which exhibit ultralow energy dissipation and simultaneously provide accurate computational results.

Discipline: Electrical Engineering

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1 Introduction

Conventional computational processes typically involve irreversible operations. However, some input bits of information might be erased during these operations. Landauer (1961) proved that irreversible computations lead to information loss and are accompanied by heat dissipation to the environment. The amount of heat dissipated is (kBTln2) per bit erased, where kB is the Boltzmann constant and T is the temperature [1]. According to Gershenfeld (1996), the amount of energy dissipated owing to the loss of information is significantly higher than Landauer's lower limit [2]. However, continuous decreases in the size of computing devices and improvements in material and fabrication processes are resulting in contemporary nanoelectronics circuits and systems whose energy dissipation levels are starting to approach Landauer's bound of (kBTln2) per bit erased. Therefore, to be able to continue the trend of reducing power consumption, as has been the case in the last few decades, and approach Landauer's lower limit, unconventional methods of computation that allow for Boolean logic operations without information loss are required. One alternative is the reversible computation paradigm, which is realized using reversible logic operations, wherein each input signal has a unique output pin. In 1973, Bennett proved that reversible computations could mitigate the problem of information loss and, in theory, even eliminate it [3]. Consequently, technologies that can implement logic operations reversibly are the way forward for the realization of ultralow-energy-dissipation computing [4].

In 1993, Lent *et al.* presented the principle of quantum-dot cellular automata (QCA), employing the cell charge configuration to encode binary information [5]. The specified cell layout and cell-cell electrostatic interactions allow for logic operations, and many researchers have adopted QCA as a prospective computing paradigm [6-8]. QCA is field-coupled nanotechnology, where information is encoded in the form of the polarization of each cell [9]. The information is subsequently propagated to the neighboring cells via the Coulombic electrostatic force. This results in low energy dissipation as there is no current flow [9]. The QCA cell is in the form of four quantum dots, where two electrons are "placed" [10]. Tunneling is allowed between the quantum dots within a cell, wherein the cell moves towards its ground state in a configuration determined by the electrostatic configuration of the neighborhood. The quantum dots are located at the corners of a square and are represented in white in Figure 1 while the two mobile electrons are depicted in black. Adjusting the height of the tunnel barriers or the bias on the cells allows for the clocking control of the QCA computation. Owing to electrostatic interactions, the electrons within a cell experience reciprocal repulsion and are consequently pushed to the opposing corners of the square. The Coulombic interactions between the adjacent cells cause the saturation of the polarization of the cells towards a specific alignment. These interactions and the prescribed layout of the cell system are the essences of the QCA approach for implementing wires and logic gates. The fundamental gate is the majority gate that demonstrates the majority of the voting logic behavior. Figure 1 illustrates the QCA states, wires, and primitive logic gates.

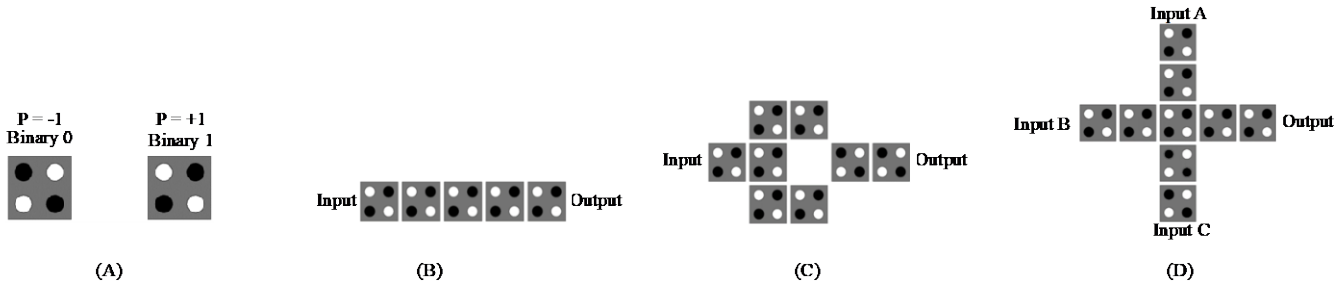

Figure 1: (A) QCA states, (B) QCA Wire, (C) Inverter, and (D) Majority gate

In QCA circuits, information flows from the input toward the output, in a pipeline architecture governed by an adiabatic switching clocking system with four distinct phases [9]. The clocking system keeps the QCA circuit always in an instantaneous ground state by controlling the potential barriers between quantum dots within a QCA cell and preventing metastability issues [11, 12]. The adiabatic switching clocking scheme is realized by an underlying circuitry that generates an electric field for the modulation of the tunneling barriers between the dots of QCA cells [13]. The clock is implemented by having buried conducting metal wires that yield signals to accomplish four clock phases, with phase shift by π/2 per signal [14]. The four clock phases are always in the ordered sequence of four states: Switch, Hold, Release, and Relax. The QCA chip is divided into clock zones, labeled Clock 0-3. The cells in each zone are controlled by a specific clock signal to perform a particular computation [11]. The four clocking zones correspond to the four clock signals and form a complete QCA clock cycle. Data flow in QCA circuits is only possible among cells controlled by consecutively numbered clocks, i.e., Clock 0 to Clock 1, Clock 1 to Clock 2, Clock 2 to Clock 3, Clock 3 to Clock 0, and so on, see Figure 2A. The clocking phase switching in the different clock zones is illustrated in figure 2B. In the first phase (Switch), the interdot barriers of the cells start to raise while the input is applied. Increased interdot barriers lead the cells to reach the second phase (Hold), where the cells become polarized into the bistable states corresponding to the ground state of the new input. In the third phase (Release), the interdot barriers of the cells begin to lower gradually to remove the polarization induced by the old input data. Decreased interdot barriers lead the cells to reach the last phase (Relax), where the cells exhibit no polarization state.

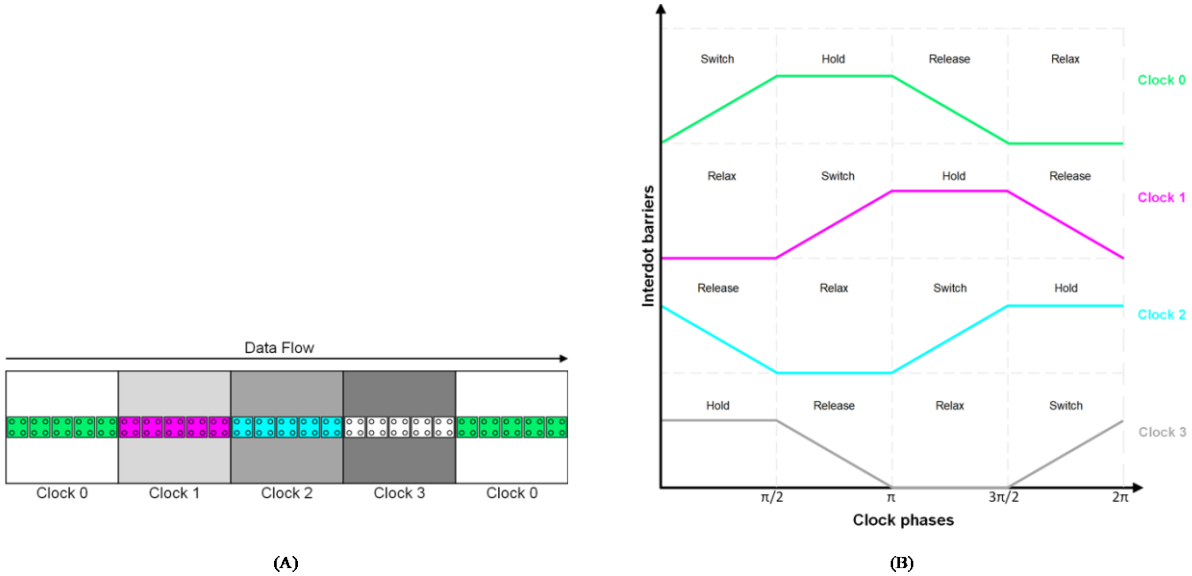

Figure 2: (A) QCA data flow (B) Clocking phases in different clock zones

To realize ultralow-energy-dissipation computing operations, that is, operations, where the amount of energy dissipated, is below the (k_BTln2) limit, reversible computational circuits need to be implemented. However, Landauer pointed out that, in the case of conventional technologies, the energy required for operating circuits is still considerably higher than the (k_BTln2) limit. This is the case even if reversible computations are implemented at the logic level because circuits do not act in a physically reversible manner [1]. DeBenedictis *et al.* (2016) stressed that reversible computing is a sensible low-power strategy only if reversibility is ensured down to the physical level, where the amount of energy dissipated is less than the crucial Landauer limit per operation [4]. QCA is suitable nanotechnology for performing operations that are both physically and logically reversible, thus allowing for the realization of ultralow-energy-dissipation computing. Although there have been numerous studies on reversible QCA designs recently [15-17], these studies have tended to address reversibility only at the logical level and have not treated information loss at the physical level. The current lack of precise calculation techniques for power dissipation in QCA designs could yield invalid results. This, in turn, may lead to uncertainty regarding whether the QCA designs indeed allow for reversibility at the logical and physical levels and thus permit operations below the critical energy barrier. Torres *et al.* (2018) introduced a physics-based model, which is a thorough description of how energy is dissipated in a QCA circuit, and it has been implemented in the simulator *QCADesigner-E* [18]. Torres *et al.* (2019) then, for the first time, used this approach to investigate whether logically and physically reversible QCA designs can operate with near-zero energy dissipation [19]. The results confirmed that the basic logically and physically reversible QCA building blocks such as wires, single-logic gates, and more complex reversible QCA circuits, made up of these reversible building blocks, can indeed be operated in a logically and physically reversible fashion, resulting in energy dissipation levels lower than (k_BTln2) per operation. However, they did not consider the data synchronization of the design, which can influence the accuracy of the computation that the circuit is supposed to perform.

In complex digital circuit designs, clock synchronization is essential for all the logic gates that compose the circuit, starting from the first logic gate to the final output. Clock synchronization is necessary to ensure the balance of the data propagation speed and guarantee that the data arrival time is correct for the next stage in the circuit [20]. Furthermore, the absence of clock synchronization constraints can lead to the generation of inaccurate bits in the next stage, resulting in incorrect data transmission. Thus, designing QCA digital circuits that are logically and physically reversible can ensure that the energy dissipated is less than (k_BTln2) per operation. However, this needs to be supplemented by time synchronization to guarantee data propagation accuracy at all the circuit stages.

In this study, for the first time, logically and physically reversible circuit elements that are time synchronized were designed and simulated. To this end, new reversible and synchronous QCA combinational circuits were designed to mitigate the clock delay problems that may cause the

nonsynchronization of the logic gate information. These novel designs, which allow for time synchronization, have an inherently more symmetric circuit configuration. Reversible time-synchronized designs for eight QCA combinational logic circuits were developed, and the circuits were simulated. These included circuits for the XOR and XNOR gates and a half-adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder. The simulation results confirmed that it is possible to design ultralow-energy-dissipation QCA circuits whose energy dissipation limit is less than the Landauer energy limit of 0.06 meV for a temperature of 1 K and provide reliable computational results. These circuits are logically and physically reversible as well as time-synchronized.

The remainder of this paper is organized as follows. In Section 2, the QCA design and simulation setup are described. In Section 3, the simulation results are described, while the conclusions of the study are stated in Section 4.

2 Design and Simulation Setup

Recent research has provided strong evidence that logically and physically reversible QCA circuits are "breaking through" Landauer's energy limit [19]. However, the time synchronization of the input data at every logic gate was not considered in these studies. The absence of time synchronization can affect the accuracy of the circuit outputs, especially in the case of complex designs. Therefore, the time synchronization of the logic gates is considered crucially important in this study. Time synchronization is achieved by design, alongside the logical and physical reversibility of the circuits, to ensure accurate computational results and ultralow energy dissipation. In 2019, Torres *et al.* devised logically and physically reversible QCA circuits by designing reversible primitive logic gates and then created a half-adder based on those reversible primitive logic gates [19]. However, the design of this half-adder, (see Figure 3), does not consider clock synchronization of the internal logic signals. This affects circuit output reliability, leading to inaccurate computations. The sum operation has two inputs that have diverging arrival times. The reversible OR gate inputs arrive after 9 and 13 clock zones respectively, which means input 1 arrives before input 2 by four clock zones, i.e., a whole clock cycle. Hence, input 1 must not change for an additional clock cycle to achieve time synchronization and consequently achieve correct operation.

Generally, in QCA circuits, the primary synchronized information applied to the input pins does not necessarily produce a similar arrival time for the inputs of all logic gates that comprise the circuit. Moreover, input signal paths leading to a particular logic gate can come from different clock zones. To assure time synchronization and preserve the circuit functionality then we should enforce that each logic gate inputs data during the same clock cycle, i.e., four clock zones, before inputting new data. Time synchronization can be achieved by utilizing additional clock zones that can guarantee the information's arrival within the same clock cycle.

In this study, we investigated the clock synchronization of reversible QCA circuits by introducing a QCA logic design paradigm that can be operated reversibly both logically and

physically. Furthermore, the proposed design paradigm also considers the issue of clock synchronization. Thus, it yields accurate output results for reversible QCA combinational logic circuits, which run below the ($k_BT$ln2) energy limit. To this end, and to demonstrate the effectiveness of the proposed design paradigm, we investigated eight combinational logic circuits. In particular, logically and physically reversible time-synchronized QCA designs were developed for the XOR and XNOR gates and a half-adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder, and the circuits were simulated to authenticate the proposed method. All the implemented circuits were inspired by the reversible design method proposed by Torres *et al.* (2019) [19]. The contribution of the present work is that, for the first time, time synchronization has been incorporated in the design of logically and physically reversible QCA circuits to mitigate the problem of clock delays that can occur in complex circuits. This is achieved by using an inherently more symmetric circuit configuration.

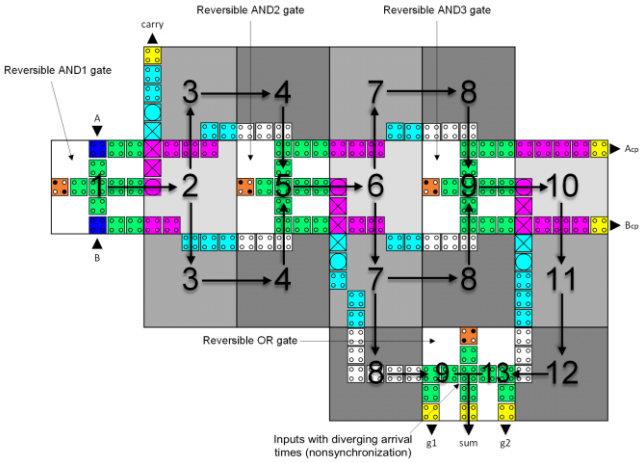

Figure 3: Torres et al. [19] Reversible half-adder circuit

Overall, the proposed design method is implemented by forming each circuit from an arrangement of reversible QCA primitive logic gates connected by QCA wires. Information arrives at every input of a logic gate at each level in the design simultaneously, that is, with a similar delay. Thus, synchronized "signals" are transferred to the subsequent logic gate level in the circuit, up to the final outputs.

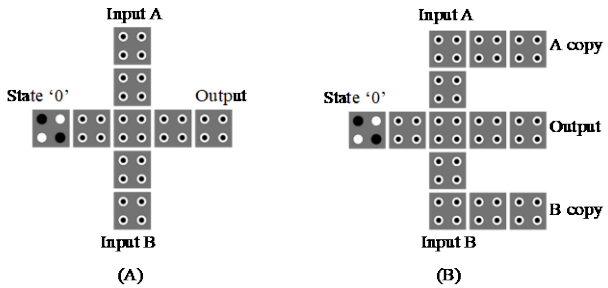

Figure 4: (A) Standard QCA AND gate, (B) Reversible QCA AND gate

To highlight the difference between the standard and reversible QCA logic gates, Figure 4 shows the contrast between the standard and reversible QCA AND gates. The standard QCA AND gate depicted in Figure 4A is a nonreversible logic operation and has three inputs and one output. Therefore, it exhibits information loss and, hence, has an accompanying energy dissipation level

that is greater than Landauer's limit. On the other hand, the reversible QCA AND gate illustrated in Figure 4B generates copies of the input data and has three inputs and three outputs; therefore, there is no information loss and no associated energy dissipation to the environment.

To implement the circuit layout and simulate the energy dissipation levels for QCA designs, an appropriate tool is required. Presently, two technology computer-aided design tools are available for simulating the energy dissipation of QCA circuits: *QCADesigner-E*, which was introduced by Sill Torres *et al.* (2018) [18], and *QCAPro*, which was developed by Srivastava *et al.* (2008) [21]. The *QCAPro* simulation tool requires an ideal clock slope and can yield a higher limit for energy dissipation. Thus, *QCAPro* is not suitable for determining the energy dissipation values. In contrast, *QCADesigner-E* can accurately calculate the energy dissipation values. The *QCADesigner-E* simulation tool is based on the widely used *QCADesigner* software package. *QCADesigner* implements the coherence vector simulation engine (CVSE), which incorporates the microscopic physics quantum-level modeling of the QCA cell performance [22]. Accordingly, the *QCADesigner-E* tool was selected to simulate the energy dissipation of the QCA designs, owing to its incorporation of a proper energy dissipation treatment based on the application of quantum mechanics to the microscopic QCA cell. Moreover, *QCADesigner-E* extends the CVSE model of *QCADesigner* to include power dissipation.

Throughout the logic circuit execution process, clocking control is required to precisely regulate the data flow between the cells and prevent the system from being stuck in a metastable state. An external clock is employed to vary the intercellular tunneling barrier height within the QCA cells to achieve clocking control. In this study, all the designs employed the universal, standard, and efficient (USE) clocking scheme pioneered by Campos *et al.* (2015) [23]. The USE clocking scheme enables feedback paths with small or large loops and allows for routing simplification owing to its flexibility. Current integrated circuit fabrication technologies can be utilized to realize USE clocking circuitry. The USE clocking scheme employs a four-phase QCA clock, where a complete QCA circuit can be realized with four different clock zones numbered from 1 to 4, as depicted in Figure 5. Here, each square is a clock zone that contains 5 × 5 QCA cells, while the arrows indicate the flow of information between the QCA cells located in adjacent clock zones. The USE clocking scheme is necessary to meet the standard cell specifications, develop placement and routing algorithms, and exploit the other resources that will allow QCA technology to advance [23]. One of the main problems in digital design is how to deal with the junctions of wires. In QCA technology, wires can be crossed either using the coplanar method, wherein rotating QCA cells are used at the crossed point, or by using the multilayer method, wherein two different layers are used to prevent crosstalk interference between the two crossing wires [24]. Although the coplanar approach is a classic advantage of the QCA paradigm and is used by most designs, the use of the multilayer method results in more robust circuits [25].

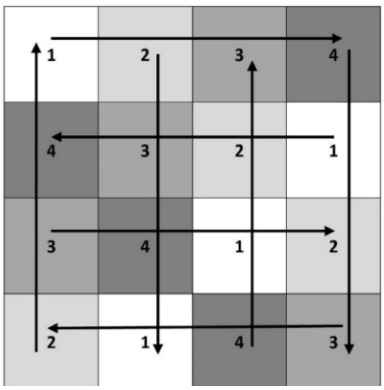

Figure 5: The USE clocking scheme (the squares express the clock zones, while the arrows show the dataflow)

In this study, all the designs employed the multilayer approach for wire crossing, as proposed by Bajec and Pecar (2012) [26].

Furthermore, to perform realistic energy analysis, we used the testbench proposed by Torres *et al.* (2018) to characterize the QCA circuits [18]. This testbench incorporates an input signal with a few additional buffer cells between the stimulated inputs and the actual inputs of the simulated circuit. Similarly, the circuit outputs are also connected to a few buffer cells. These cells were excluded from the overall energy analysis (see Figure 6).

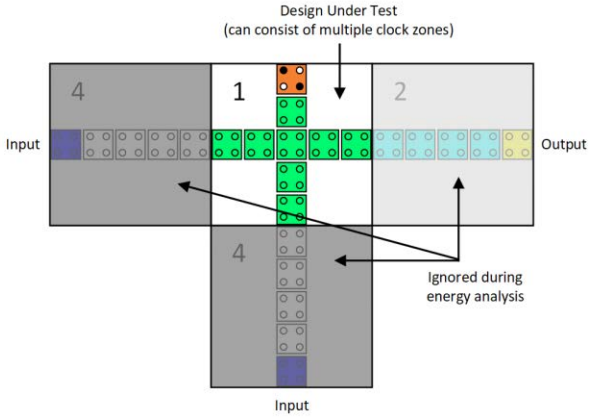

Figure 6: The used QCADesigner-E simulation testbench

The technology and simulation parameters in the QCADesigner-E tool can be modified to match a particular physical situation and enhance the simulation accuracy. The time step must be sufficiently small to decrease the simulation error related to the internal rounding errors. The simulation error can be monitored by ensuring that the condition of energy conservation is maintained numerically within the acceptable error bounds. A clock slope of 100 ps was used, and the time interval step for each iteration (Tstep) was adjusted to be Tstep = 0.1 τ = 0.1 fs, where τ is the relaxation time. This time step resulted in simulation errors with an acceptable numerical energy conservation violation, which was given by ϵenv $\leqslant$ 5%. The technology and simulation parameters used for the simulations in this study are listed in Tables 1 and 2, respectively.

The proposed designs for the XOR and XNOR gates and the half-adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder circuits are shown in the figures below. The truth tables and logic equations shown are the conventional irreversible standard versions.

However, the QCA circuits designed and simulated in this study are fully logically and physically reversible. The complete reversible truth tables and logic equations are not given owing to space limitations. Note that, in the QCA circuit design diagrams, the "cp" labels of the outputs refer to copies of the input information, while "g1" and "g2" indicate the so-called garbage outputs.

Table 1: Technology parameters used

Parameter	Description	Value
QD size	Quantum dot size	5 nm
Cell area	Dimensions of each cell	18 × 18 nm
Cell distance	Distance between two cells	20 nm
Layer separation	Distance between QCA layers in multilayer crossing	11.5 nm
Clock high	Max. saturation energy of clock signal	9.8E-22 J
Clock low	Min. saturation energy of clock signal	3.8E-23 J
Relative permittivity	Relative permittivity of material for QCA system (GaAs & AlGaAs)	12.9
Radius of effect	Maximum distance between cells whose interaction is considered	80 nm
Temp	Operating temperature	1 K

Table 2: Simulation parameter values considered in this study

Parameter	Description	Value
τ	Relaxation time	1E-15 s
T_{γ}	Period of the clock signal	1E-9 s
T_{in}	Period of input signals	1E-9 s
T_{step}	Time step for each iteration	1E-16 s
T_{sim}	Total simulation time	8E-9 s
γ_{shape}	Shape of clock-signal slope	GAUSSIAN
γ_{slope}	Rise/fall time of clock-signal slopes	1E-10 s

Next, we focus on the mechanism of the proposed design paradigm for reversible time-synchronized QCA circuits, which are simultaneously both logically and physically reversible. The proposed paradigm can solve the clock synchronization problem. First, we describe the inherently symmetric configuration of the first proposed reversible time-synchronized circuit, namely, the XOR circuit, which is illustrated in Figure 7. The key to time synchronization is the geometry of the design, which allows for symmetric data propagation. The reversible time-synchronized XOR circuit consists of two reversible OR gates and one reversible AND gate. Each of these gates has three binary inputs and three binary outputs. The Boolean expression for the proposed reversible time-synchronized XOR logic circuit output is the standard one and is given by Equation 1. Table 3 lists the circuit output responses for the various combinations of inputs.

$$Output = (A + B).(\overline{A} + \overline{B}) \quad (1)$$

Table 3: Truth table for XOR gate shown in Figure 7

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

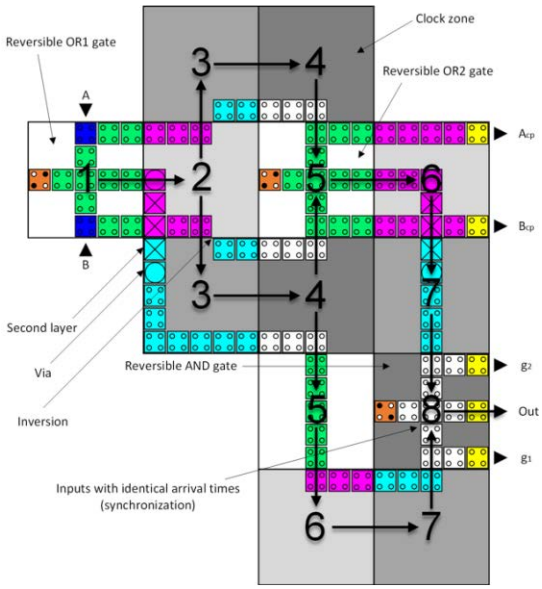

Figure 7: Reversible time synchronized XOR circuit (Acp and Bcp indicate copies of the inputs whereas g1 and g2 are so-called garbage outputs)

The two binary inputs, A and B, feed the first reversible OR gate (OR1) initially. The output from OR1 is transferred to the lower AND gate and finally routed to the output "pin" labeled "Out" through eight clock zones. Concurrently, inverted copies of the input data are transferred to the second reversible OR gate (OR2) through four clock zones of time delay. Next, the OR2 output is transferred to the lower AND gate and then to the output "pin" called "Out" through an additional four clock zones. Thus, the outputs of both reversible OR gates are transferred concurrently to the lower AND gate and then to the output "pin" called "Out" through eight clock zones. The arrival time for the bit information copies of OR2 labeled "Acp" and "Bcp" outputs to the end of the circuit corresponds to six clock zones. This symmetric design approach was applied to the other designs as well. Thus, the proposed designs ensure that there is a balance between the data propagation speed at all the circuit stages to achieve time synchronization.

The second introduced design is the reversible time-synchronized XNOR gate, which combines two reversible AND gates and one reversible OR gate, the corresponding QCA cell layout is shown in Figure 8. The circuit computation output is given by Boolean Equation 2, while Table 4 lists the truth table of the circuit.

$$Output = (A.B) + (\overline{A}.\overline{B}) \quad (2)$$

Table 4: Truth table for XNOR gate shown in Figure 8

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

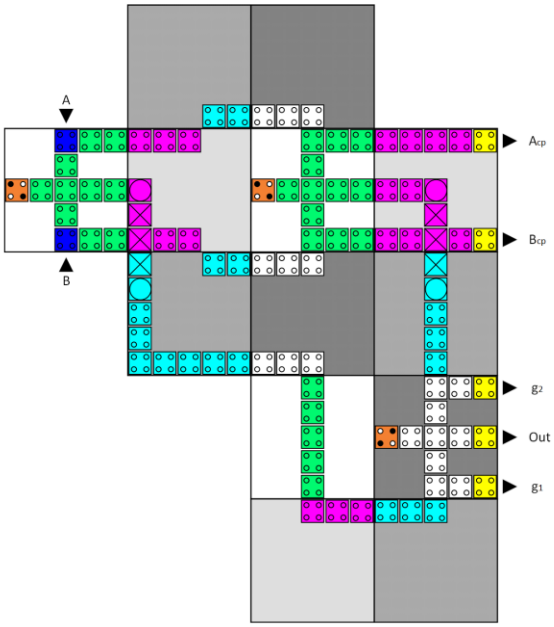

Figure 8: Reversible time synchronized XNOR circuit

Figure 9 depicts the third design, a reversible time-synchronized half-adder circuit comprising three AND gates and one OR gate. The proposed reversible time-synchronized design paradigm was applied to the Torres et al. [16] reversible non-synchronized half-adder design. An OR gate was relocating, and an additional clock zone was utilized, such that paths now have an equal length. Unlike the Torres et al. [16] reversible non-synchronized half-adder design, the sum operation now has two inputs that have identical arrival times. The reversible OR gate inputs arrive simultaneously after 12 clock zones. Thus, this new reversible half-adder circuit achieves the time synchronicity characteristic, that can guarantee circuit computation accuracy. The truth table for this circuit is presented in Table 5, while its Boolean expressions are described in Equation 3 as follows:

$$Sum = (A.\overline{B}) + (\overline{A}.B) \tag{3}$$

$$Carry = (A.B)$$

Table 5: Truth table for the half-adder shown in Figure 9

A	B	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

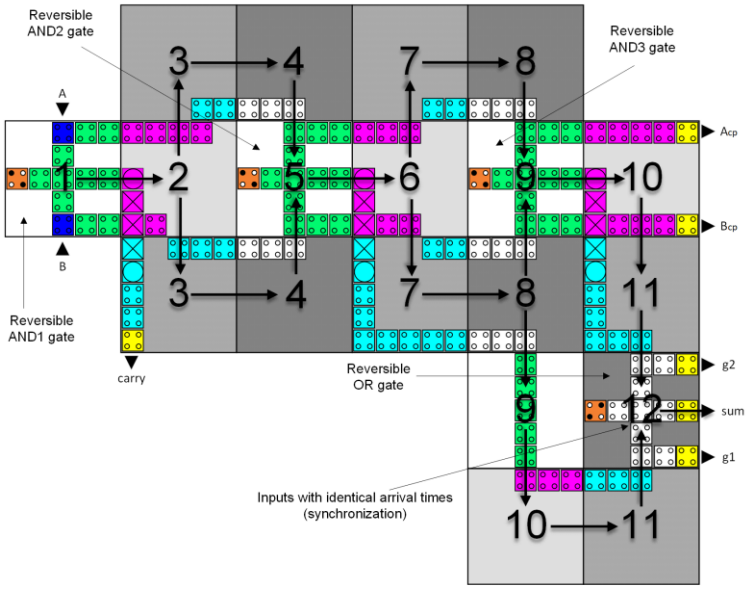

Figure 9: Reversible time synchronized half-adder circuit

The fourth circuit is a reversible time-synchronized half-subtractor, as illustrated in Figure 10, and it consists of two AND gates and one OR gate. Equation 4 defines the Boolean equations for the design outputs, while Table 6 shows the circuit output responses for the various combination inputs.

$$Diff = (\overline{A}.B) + (A.\overline{B}) \quad (4)$$

$$Borrow = (\overline{A}.B)$$

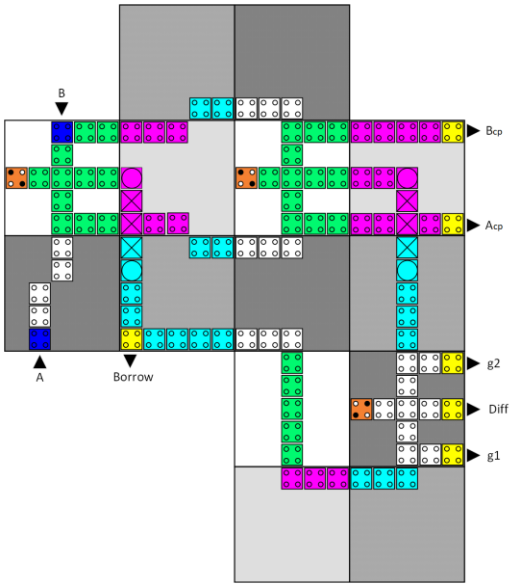

Figure 10: Reversible time synchronized half-subtractor circuit

Table 6: Truth table for half-subtractor shown in Figure 10

A	B	Borrow	Diff
0	0	0	0
0	1	1	1
1	0	0	1
1	1	0	0

A 2-to-1 reversible time-synchronized multiplexer is the fifth circuit (see Figure 11) and consists of two AND gates and one OR gate. The Boolean expression for this design output is given in Equation 5, where A and B are the two inputs, S is the selector input, and Mux is the circuit output. Table 7 presents the truth table for the circuit.

$$Mux = (A.\overline{S}) + (B.S) \quad (5)$$

Table 7: Truth table for 2-to-1 multiplexer shown in Figure11

S	A	B	Mux
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

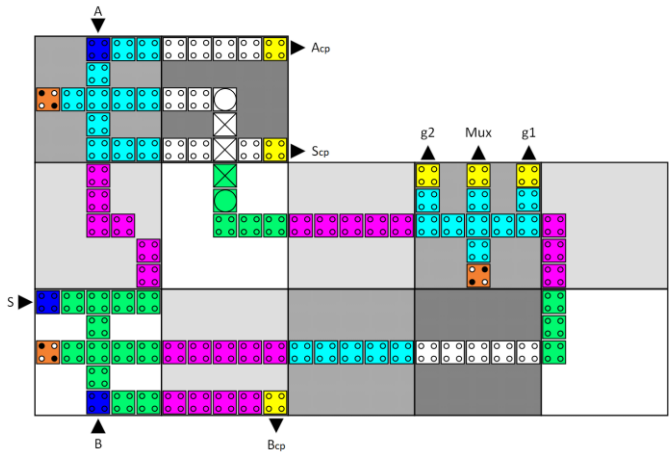

Figure 11: Reversible time synchronized 2-to-1 multiplexer

The sixth circuit is the 1-to-2 reversible time-synchronized demultiplexer shown in Figure 12, which contains only two AND gates. Equation 6 defines the Boolean functions for its design outputs, wherein S and DATA are the two inputs and Y0 and Y1 are the two outputs of the circuit. The circuit truth table is presented in Table 8.

$$Y0 = (S.DATA) \quad (6)$$

$$Y1 = (\overline{S}.DATA)$$

Table 8: Truth table for 1-to-2 demultiplexer shown in Figure 12

S	DATA	Y0	Y1
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

A reversible time-synchronized comparator is the seventh introduced circuit and is shown in Figure 13. This proposed circuit combines three AND gates and takes two binary input numbers, A and B, and determines whether one number is greater than, less than, or equal to the other number.

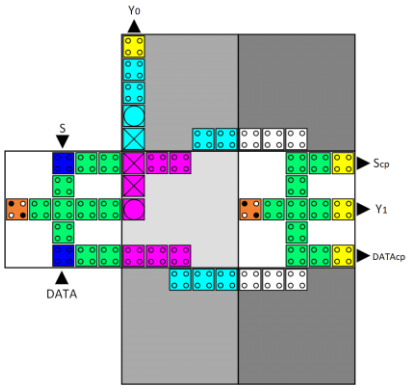

Figure 12: Reversible time synchronized 1-to-2 demultiplexer

The logic expressions for this comparator circuit are given by Equation 7, while the circuit output responses for the various combination of inputs are listed in Table 9.

$$(A < B) = (\overline{A}.B) \tag{7}$$

$$(A > B) = (A.\overline{B})$$

$$(A = B) = \overline{(\overline{A}.B)}.\overline{(A.\overline{B})}$$

Table 9: Truth table for comparator shown in Figure 13

A	B	A<B	A>B	A=B
0	0	0	0	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

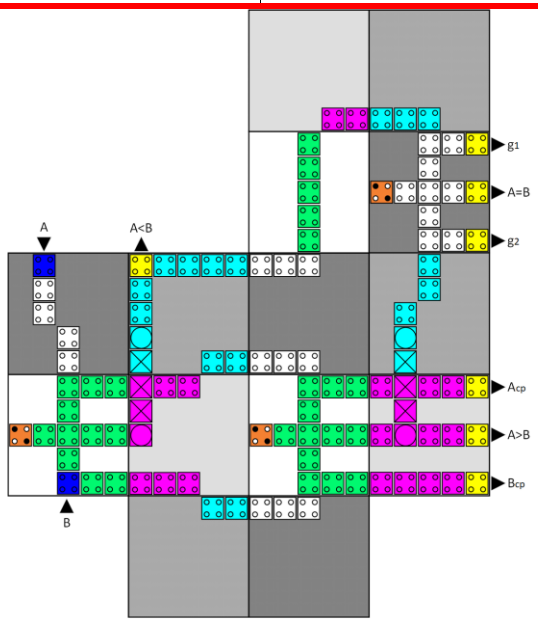

Figure 13: Reversible time synchronized comparator circuit

The reversible time-synchronized 2-to-4 line single-bit decoder shown in Figure 14 is the eighth proposed circuit. This circuit activates one of four output bits for each 2-bit input in the integer range. The proposed reversible time-synchronized QCA decoder design uses four AND gates. The logic expressions for this decoder circuit are provided by Equation 8 wherein A and B

denote the two inputs and D0, D1, D2, and D3 denote the circuit outputs. Table 10 presents the truth table for the decoder circuit.

$$D0 = (\overline{A}.\overline{B}) \quad (8)$$

$$D1 = (\overline{A}.B) \quad (8),$$

$$D2 = (A.\overline{B}) \quad (8),$$

$$D3 = (A.B) \quad (8),$$

Table 10: Truth table for 2-to-4 decoder shown in Figure 14

A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

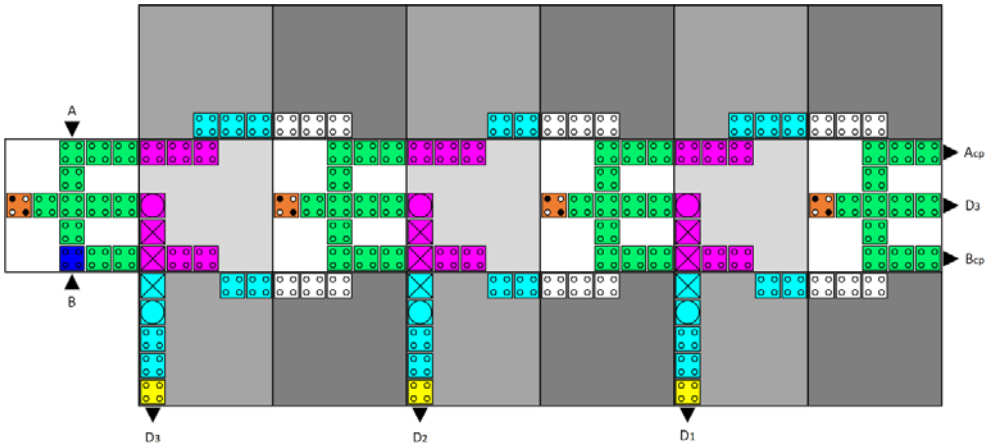

Figure 14: Reversible time synchronized 2-to-4 decoder

3 Simulation Results

This section describes the simulated input/output responses and energy dissipation values for the eight proposed reversible time-synchronized QCA combinational logic circuits. The computational reliability and delay time for each circuit were obtained from the simulation results. The area cost for each is also given. Table 11 lists the simulation results, which were obtained with the QCADesigner-E tool [18] using the technology and simulation parameters given in Tables 1 and 2, respectively. The energy dissipation for every input signal binary combination is given for all eight logic circuits in terms of meV as the unit. The area cost for each design was measured by counting the USE clocking tiles, such that every tile consisted of a grid of 5 × 5 QCA cells. The circuit latency was calculated by counting the clock zones of the critical path, where the critical path is defined as the longest route from an input pin to an output pin in the circuit. The clock zone represents a delay of a quarter of the clock period. In other words, four clock zones comprise one clock cycle. Figure 15 shows the simulation results for the efficiently designed reversible time-synchronized XOR gate, the first design introduced. The numerical output results reflect the true values listed in Table 3. Moreover, in keeping with the design shown in Figure 7, the XOR output

value arrived after a delay of eight clock zones (total time of two clock cycles). Furthermore, the circuit utilized an area of 13 tiles.

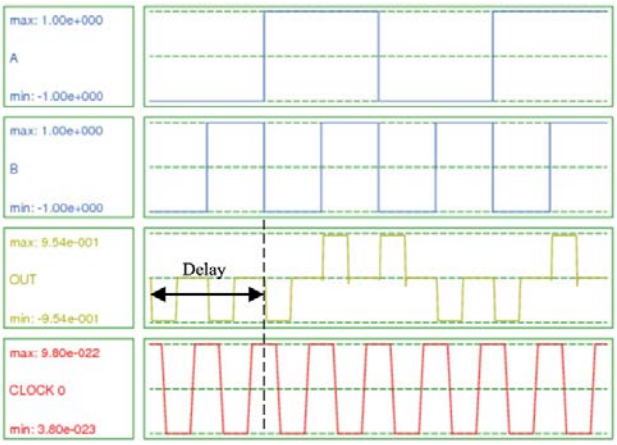

Figure 15: Simulation waveforms of the proposed reversible time synchronized XOR design (see Table 3)

Figure 16 shows the simulated waveforms for the reversible time-synchronized XNOR gate, which is the second proposed design. The polarization output correctly corresponds to the truth table values given in Table 4, thus confirming the soundness of the proposed XNOR design. The XNOR circuit design in Figure 8 has a circuit latency of eight clock zones (two clock cycles), which is consistent with the simulation results in Figure 16. The design had an area of 13 tiles.

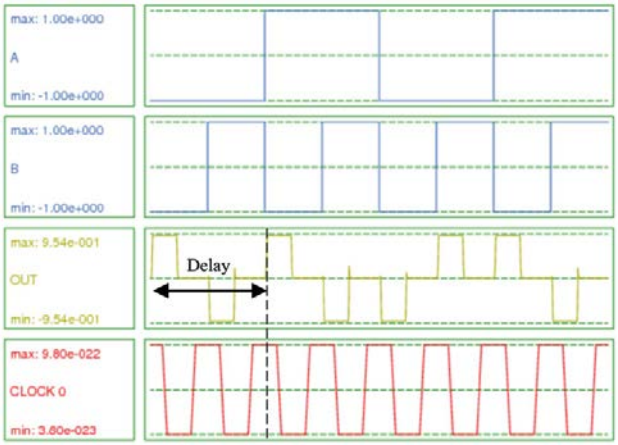

Figure 16: Simulation waveforms of the proposed reversible time synchronized XNOR design (see Table 4)

The simulation results in Figure 17 are for the third designed circuit, namely the reversible time-synchronized half-adder, the cell layout of which is illustrated in Figure 9. The numerical results obtained confirm that the design was consistent with its truth table (see Table 5). The proposed half-adder circuit provides the carry output after three clock zones (0.75 clock cycles) and the sum value after 12 clock zones (three clock cycles). Moreover, the circuit latency is three clock cycles, and the circuit requires an area of 19 tiles. Figure 18 shows the simulation results for the reversible time-synchronized half-subtractor, the fourth proposed design, with the corresponding QCA cell layout described in Figure 10. The numerical input/output results confirm that the circuit operation is compatible with the truth table shown in Table 6. The delay of the borrow output is three clock zones (0.75 clock cycles), while the delay of the difference value is eight clock zones (two clock cycles). Furthermore, the half-subtractor circuit requires an area of 14 tiles.

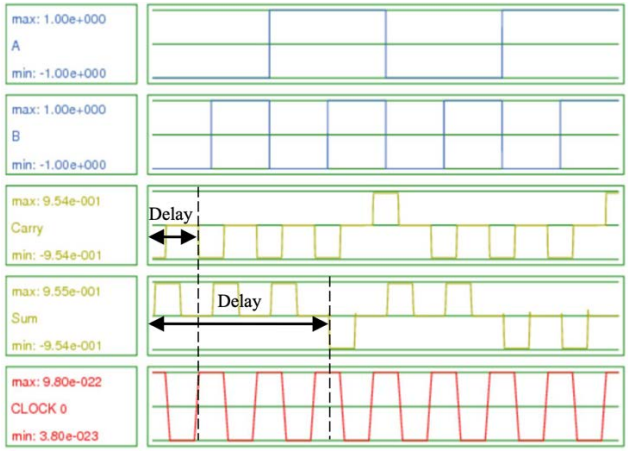

Figure 17: Simulation waveforms of the proposed reversible time synchronized half-adder design (see Table 5)

The waveform in Figure 19 is the simulation result for the reversible time-synchronized 2-to-1 multiplexer circuit, the fifth proposed design. The numerical input/output response corresponds to the truth table values in Table 7, thus confirming the reliability of the design. The circuit latency is seven clock zones (1.75 clock cycles) and consistent with the 2-to-1 multiplexer QCA layout design in Figure 11. Furthermore, this multiplexer design has an area of 12 tiles.

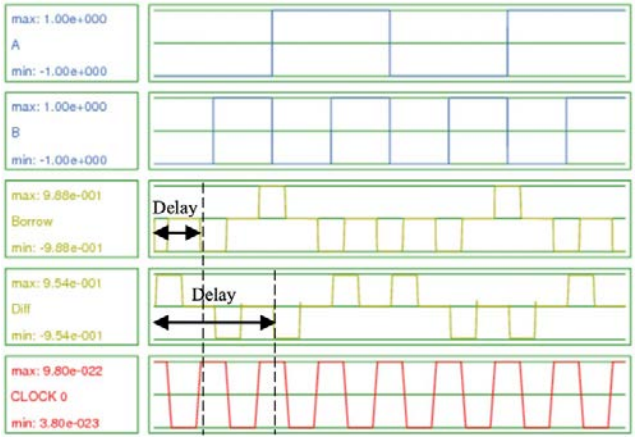

Figure 18: Simulation waveforms of the proposed reversible time-synchronized half-subtractor design (see Table 6)

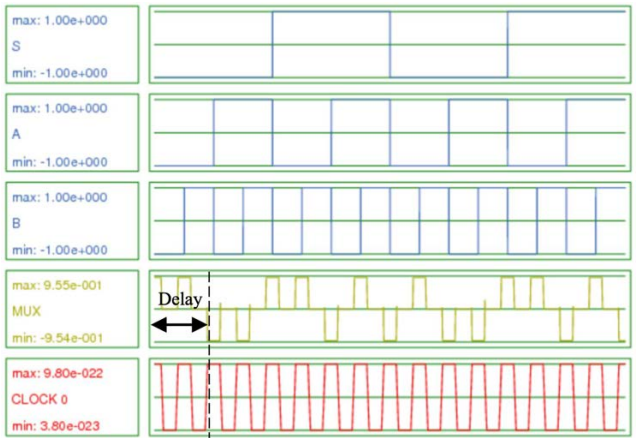

Figure 19: Simulation waveforms of the proposed reversible time synchronized multiplexer design (see Table 7)

Figure 20 shows the simulation results for the reversible time-synchronized 1-to-2 demultiplexer, the sixth proposed circuit, whose QCA layout is given in Figure 12. The input/output simulation results validate the desired circuit computation, and the response agrees with Table 8. Output Y0 is delayed by three clock zones (0.75 clock cycles), while Y1 has a latency of five clock zones (1.25 clock cycles). The area required for the reversible time-synchronized 1-to-2 demultiplexer QCA design is only seven tiles.

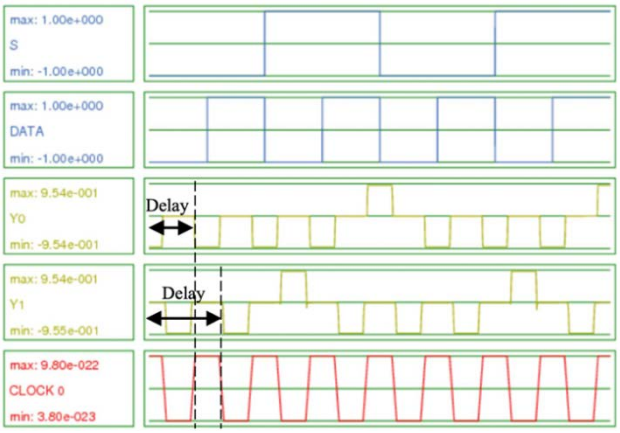

Figure 20: Simulation waveforms of the proposed reversible time synchronized demultiplexer design (see Table 8)

Figure 21 shows the simulation results for the reversible time-synchronized comparator, the seventh proposed circuit, whose QCA cell design is given in Figure 13. The input/output results obtained confirm that the circuit acts as a comparator. Moreover, the results are in keeping with the truth table in Table 9. This circuit takes two binary inputs, A and B. In case the output is A is less than B, the circuit takes three clock zones (0.75 clock cycles). In case it is A is greater than B, the circuit takes six clock zones (1.5 clock cycles). Finally, if A equals B, the circuit has a delay of eight clock zones (2 clock cycles). Furthermore, this comparator circuit requires an area of 14 tiles.

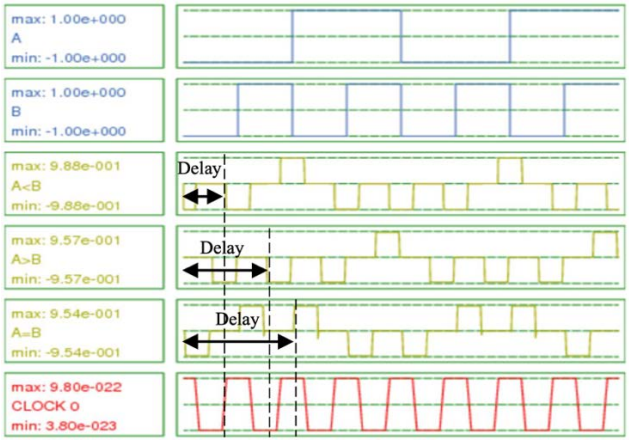

Figure 21: Simulation waveforms of the proposed reversible time synchronized comparator design (see Table 9)

Figure 22 shows the simulation results for the reversible time-synchronized 2-to-4 decoder, the eighth proposed design; the corresponding QCA cell layout is shown in Figure 14. The input/output results obtained show that the circuit works as desired and that the simulation results exhibit the correct logical behavior, as shown in Table 10. This circuit takes two input numbers, A

and B, in binary form, and gives output D3 after three clock zones (0.75 clock cycles), D2 after seven clock zones (1.75 clock cycles), D1 after 11 clock zones (2.75 clock cycles), and D0 after 13 clock zones (3.25 clock cycles). Furthermore, the designed circuit requires an area of 19 tiles.

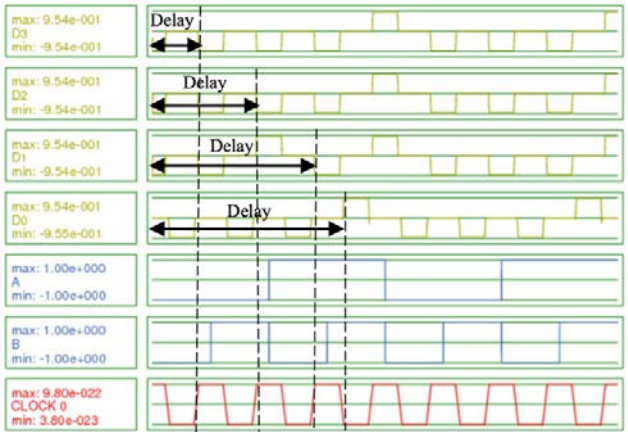

Figure 22: Simulation waveforms of the proposed reversible time synchronized decoder design (see Table 10)

Table 11: Values of energy dissipation, area cost, and delay time concerning reversible and synchronous QCA designs

Parameter	Area [tiles[1]]	Critical Path[2] Delay [clock zones[3]]	Energy Dissipation [meV] for input signal combinations							
			000	001	010	011	100	101	110	111
Reversible and synchronous XOR	13	8	0.014	0.014	0.013	0.013				
Reversible and synchronous XNOR	13	8	0.014	0.013	0.014	0.014				
Reversible and synchronous half-adder	19	12	0.027	0.018	0.027	0.027				
Torres et al. [19] reversible half-adder	18	9-13 (nonsynchronized)	0.022	0.025	0.029	0.022				
Reversible and synchronous half-subtractor	14	8	0.014	0.021	0.014	0.014				
Reversible and synchronous multiplexer	12	7	0.014	0.014	0.014	0.014	0.014	0.014	0.014	0.014
Reversible and synchronous demultiplexer	7	5	0.006	0.006	0.006	0.006				
Reversible and synchronous comparator	14	9	0.014	0.024	0.015	0.015				
Reversible and synchronous decoder	19	13	0.015	0.024	0.024	0.024				

1 Each tile contains 5 × 5 QCA cells measuring 18 × 18 nm; the spacing between the cells equals 2 nm.
2 Critical path represents the longest route between the input to output pins in the circuit.
3 Delay is measured in terms of the number of clock zones a signal must pass between the input and output pins. Notably, the clock zones shift by quarter clock periods.

The simulation results listed in Table 11 indicate an energy dissipation level lower than the Landauer energy limit of 0.06 meV for a temperature of 1 K for every input signal and circuit. Moreover, the area cost is 19 tiles for the largest circuits, which are the reversible half-adder and reversible decoder. On the other hand, the area cost is only seven tiles for the demultiplexer, which is the smallest circuit. Furthermore, the delay value as determined from the simulations for the demultiplexer, the least-delayed circuit, is only five clock zones, which is equivalent to 1.25 clock cycles. In contrast, the delay seen in the case of the decoder, the most-delayed circuit, is 13 clock zones, which is equivalent to 3.25 clock cycles. Thus, the simulation results confirmed that logically

and physically reversible QCA circuit implementations result in acceptable latency and area costs. In addition, the energy dissipation level is below (kBTln2) per operation. Thus, the proposed circuits constitute ultralow-power-consumption computing. The waveforms for the input/output responses for each of the eight proposed circuits show that the time synchronization design of the circuits guarantees the fidelity of the circuit output values. Hence, the simulations prove that it is possible to implement complex Boolean operations on XOR, XNOR, half-adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder circuits both reversibly and in a time-synchronized fashion. Moreover, these new logic designs exhibit ultralow heat dissipation and accurate computational operations.

4 Conclusion

This study investigated two significant aspects of QCA nanocomputing circuit design via simulations, namely, energy dissipation and computational accuracy. To ensure that the amount of heat dissipated is less than the Landauer energy limit (kBTln2), it is necessary to design logically and physically reversible circuits. In addition, to obtain the correct outputs for a logic circuit, time synchronization is necessary. QCA circuits can achieve the time synchronization characteristic and yield accurate computation if and only if the input data of each logic gate in the circuit have arrived within four clock phases, i.e., in the same clock cycle. To this end, for the first time, we introduced QCA logically and physically reversible and time-synchronized designs for eight different combinational logic circuits. A universal, standard, and efficient (USE) clocking scheme was employed, and the QCADesigner-E tool was used to perform simulations. The QCADesigner-E tool calculated both the polarization input/output waveform response and the energy dissipated for the simulated QCA designs based on a microscopic quantum mechanical model of the QCA cell. The proposed reversible QCA combinational digital circuit designs, which show intrinsic time synchronization are the XOR and XNOR gates and a half adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder. The simulation results confirmed that it is possible to design QCA circuits that are logically and physically reversible and concurrently synchronized. Moreover, these circuits show ultralow energy dissipation levels, which are lower than the Landauer limit of 0.06 meV at a temperature of 1 K.

The encouraging results obtained for these eight reversible time-synchronized QCA combinational designs should motivate additional research on the application of the reversible time-synchronized paradigm to more sophisticated QCA digital circuit designs. The tackling of sequential logic circuits and shift registers/counters based on the proposed QCA reversible time-synchronized technique represents a natural next step in this direction.

5 Availability of Data and Material

Data can be made available through the corresponding author.

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