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Designing Outphasing RF Power Amplifier (LINC PA) for IoT Applications in Low Power 5G Wireless Network

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Abstract

This article describes the Class E power amplifier (PA) that operates in Silterra's 130nm CMOS. The radio frequency (RF) performance uses low frequencies between 600MHz and 700MHz, the low voltage supplied at 1.3V. A few other sorts of circuit classes, including Class A, B, C, and F for analogue circuits and Class E for switching systems, are obtained from the outphasing RF PA. Classes E and F make up the majority of the classes that were implemented as components of the outphasing circuit. Through this suggestion, it was gradually demonstrated that a portion of a Class E circuit can generate an output that is acceptable for use in a circuit that can increase the semiconductor's performance parameter in the 5G region. This power amplifier (PA) uses a multi-cascode stage and capacitor and inductor as part of the circuit to enhance the frequency network in addition to adding the classified class. In addition, an RF power amplifier combiner has also been developed, which suffers from significant loss when the applied signal's peak-to-average power ratio is larger. The circuits and architectures will be implemented directly in LtSpice in order to evaluate the results and achieve the parameter values of the output power of 164.8 W, power gain of 1.29, power dissipation of 165 W, and efficiency of 82.42 percent.

Discipline: Electrical Engineering and Information Technology

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1 Introduction

Modern mobile gadgets, which include high-tech smartphones, tablets, and laptops, help individuals in many ways, including their daily activities, social contacts, and the gathering and processing of their vital private data and information. The development of CMOS, nanotechnology, integrated circuits (IC), embedded systems, and the Internet of Things (IoT) contributes to the availability of data and information for the various smartphone apps and utilities in both the consumer and business sectors of the economy [1][2][3].

However, limited bandwidth has an impact on battery life, storage, and data transmission speed, which limits the functionality of current consumer electronics. Extensive research into the fifth generation of wireless communication networks is now advancing in a number of ways. Around 2020, it is anticipated that 5G technology, which was developed over a lengthy period of time with the purpose of achieving high data speeds with extremely low latency in immediate communication, will be employed [4][5][6]. However, because of its high degree of integration, low cost, and ongoing performance development, the deployment of the 5G network in the CMOS has long been a choice for analogue and digital integrated circuits [7][8][9].

Usually, the RF circuits were mainly designed in GaAs and bipolar silicon due to improving RF performance [10]. However, the modifications are attributable to the significant scaling of the MOS transistors where frequency has been forwarded beyond 100GHz [11]. In addition, the use of MOS transistors in RF applications has been a strong demand for speed improvement. RF is commonly used in wireless applications, thus despite the efficient introduction of digital baseband circuits in CMOS and the long-term improvement of efficiency achieved by PA.

There are a few classified circuits that are compatible to implement in the outphasing RF power amplifier circuit, for example, Class A, B, AB, and C for analogue designs and Class E and F for switching designs, in the process of designing outphasing RF power amplifier that can obtain the requirements of achieving bandwidth and efficiency in the 5G network region [12][13]. The development of the 5G region can also be aided by the employment of circuit types such as multistage, multi-cascode, capacitor parallel, and others. Different classes provide various types of results based on these circuits, which have an impact on the circuit as a whole.

In order to achieve the bandwidth within the 5G network region and to obtain the output power and efficiency from the circuit, a Class E outphasing amplifier is designed in this study. This amplifier is then used to investigate the efficiency optimization of Advanced CMOS RF power amplifier architecture in low-power 5G wireless networks. The frequency and efficiency to achieve the range of the 5G network may have been amplified by creating these power amplifiers, which may have been partially implemented in integrated circuit (IC) technology. The compatible circuit that may generate results and outputs that are appropriate to conduct the circuit and gain semiconductor performance metrics like bandwidth, efficiency, and others is explained.

2 Literature Review

Modern wireless communication systems required high data rates over restricted bandwidth, effective spectrum usage, low cost and high integration capacity. The name of LINC PA stands for linear amplification using non-linear components, a method where two constant amplitudes phase modulated signals to achieve amplification of power [14][15]. The outphasing modulation technique was invented by Henri Chireix in 1935 in order to improve both efficiency and linearity of AM broadcast transmitters. Later, the LINC PA applications were extended up to microwave frequencies. The outphasing PA is capable of linear power amplification using a highly efficient non-linear power amplifier and also uses multiple phase-shift power saturated or switched-mode branch power amplifiers to provide a modulated output of the radio frequency [16][17]. Interaction with the lossless non-isolating power combiner generates the modulation of the load branch amplifiers which modulate the performance of the system output. Besides that, an outphasing Class F power amplifier (PA) with a Chireix power combiner with a floating load can provide output from a 1.8V power supply [18]. In these classes, if the switching stages had been implemented through the load network, it provides a high termination impedance and the voltage across the switch exhibits sharper edges than the sinusoid wave, therefore it reduced the power loss in the transistor. Modern wireless communication systems required high data rates over restricted bandwidth, effective spectrum usage, low cost and high integration capacity. The name of LINC PA stands for linear amplification using non-linear components, a method where two constant amplitudes phase modulated signals to achieve amplification of power. The outphasing modulation technique was invented by Henri Chireix in 1935 in order to improve both efficiency and linearity of AM broadcast transmitters. Later, the LINC PA applications was extended up to microwave frequencies.

The outphasing PA is capable of linear power amplification using a highly efficient non-linear power amplifier and also uses multiple phase-shift power saturated or switched-mode branch power amplifiers to provide a modulated output of the radio frequency. Interaction with the lossless non-isolating power combiner produces a modulation of the load branch amplifiers that modulates the performance of the device. Table 1 shows the advantages and disadvantages of outphasing PA.

Table 1: The advantages and disadvantages of outphasing PA [19].

Advantages	Disadvantages
The simplicity of architecture, consisting of SCS, two parallel amplifiers and a power combiner.	Narrow bandwidth.
Output improved without improvements to hardware.	High-precision synchronization between parallel RF for maximum performance.
Pre-distortion methods are used to increase overall device linearity.	Practical efficiency compared to theoretical, which has been significantly decreased due to losses in passive components.
Possible integration a single AIC.	Specific power combiner required.

Besides that, an outphasing Class F power amplifier (PA) with a Chireix power combiner with a floating load also can provide output from a 1.8V power supply. In these class, if the switching stages had been implemented through the load network, it provides a high termination impedance and the voltage through the switch has finer sharper edges than a sinusoid wave, which decrease the power loss in the transistor.

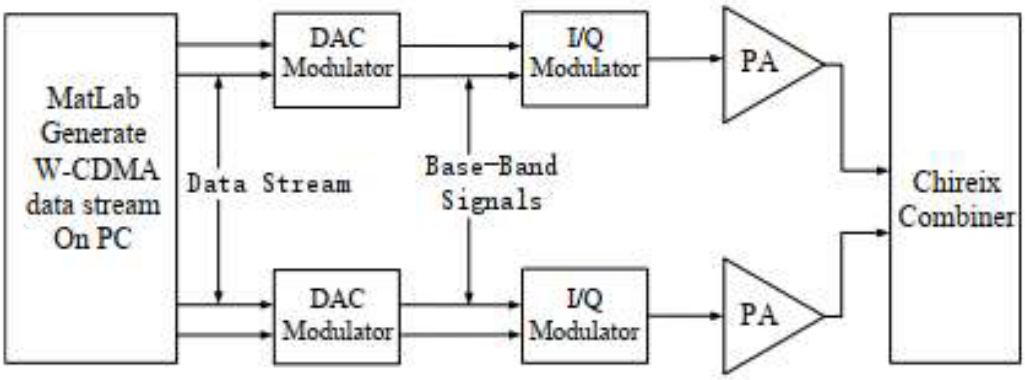

Figure 1: Block diagram of simulation process.

Based on Figure 1, these outphasing Class F specified the simulation by using Matlab software to generate a digital W-CDMA data stream [18]. W-CDMA basically uses GSM and EDGE as UMTS and also resulted in high-level internet speed. It signified the leap from 2G to 3G and it push forward in terms of speed. From WCDMA through DAC modulator to produce I/Q signal as system base-band signals. I/Q signals referred to two sinusoids that have the same frequency and are 90° out of the phase. Basically, the I/Q can produce any form of modulation that can be performed by varying the amplitude, the amplitude of in-phase and quadrature, and combining both of it together to amplify the amplitude.

Thus, Class E power amplifier (PA) topology have various advantage such as high efficiency, low-cost portable applications with high convergence standard and also supplied voltage up to 1.3V [20]. It is also a Class E switching power amplifier which provides higher efficiency. In addition, researchers have demonstrated that tunable capacitors in the power-combining network significantly improved [21]. On the other hand, some of the research projects regarding in wideband operation of an outphasing transmitter where it can deliver its power to a floating load or similar to a transformer-based combiner as shown in Figure 2.

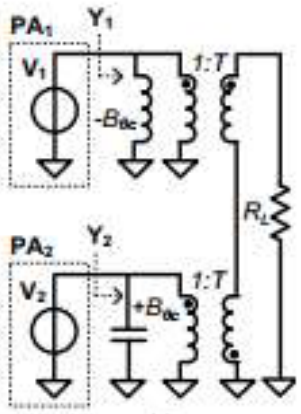

Figure 2: A transformer-based combiner [22].

The work mentioned in the figure above shows an outphasing system with Class E GaN PAs and a transformer-based Chireix combiner made with wire bonding which is a tool used to create contacts between IC or other semiconductor devices and their packaging during the manufacturing process [7]. In order to maintain high output over a broad RF bandwidth, both the power combiner and the branch amplifier must be used to influence bandwidth. Class E is a convenient and compatible classified circuit for branch amplifiers that can be used for network service.

2.1 The Outphasing Topology

The outphasing power amplifier is a technique where improvement is needed in the average efficiency and linearity of AM broadcast transmitter. The LINC created to identify the linear amplifier intermediate stages of RF power amplification may supply the highly non-linear devices in which the relationship between input and output power does not plot on a graph as a straight line.

The shortcomings for the practical implementation of an outphasing PA are expressed by the divergence of the actual transistor characteristics and behaviour from the ideal voltage source which is usually assumed for Chireix PA theoretical analysis. In addition, some functional ones are connected to the output combiner and the input network which are responsible for producing the two opposite phase modulated signals from the amplitude modulate (AM) one at the input.

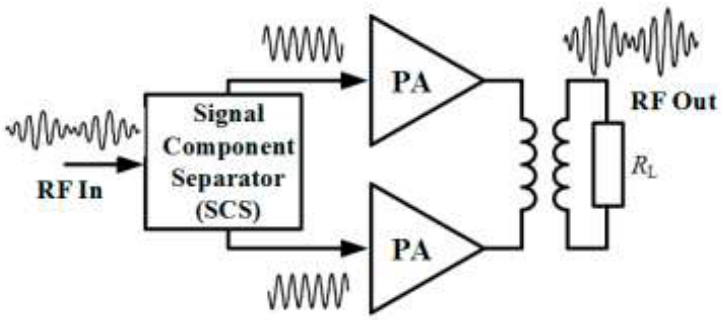

Figure 3: Simplified outphasing PA architecture diagram [7].

Figure 3 above shows the concept of the outphasing architecture where the amplitude modulated (AM) signal is divided by the signal component separator (SCS) into two phases

modulated (PM) signals with equal constant envelopes and opposite modulated phase variations. These constant envelope PM signals are amplified independently by two distinct, equivalent PA signals. Finally, the output of the PAs is combined to create an amplified AM signal. In addition, the force of the RF power amplifier is normally designed for peak

efficiency under maximum output power conditions. Outphasing can also be seen as a desirable candidate as it enables the use of highly efficient switch-mode PAs (SMPAs) while also being able to provide linear amplification without the need for DC-DC converters, which appear limits the attainable instantaneous bandwidth [7]. The advantage of the outphasing PA is having an area-efficient architecture consisting of a signal component separator, two parallel amplifiers and a power combiner. The power combiner requires a strict margin phase in order to split and combine the RF signals accurately. Therefore, the combiner restricts the bandwidth of the outphasing PA which creates applicable for narrow-band applications only.

Plus, it required high precision synchronization between the parallel RF paths to obtain high efficiency. Thus, the PA is compatible and achieves a maximum output power where reduced power consumption to utilize a 5G network. In a nutshell, the outphasing RF PA operation provides a clear and simple solution for simultaneously achieving high efficiency and linearity in a power amplifier system.

3 Method

3.1 Design Process

Progress of work consists of simulating several testing circuits, designing the Outphasing power amplifier Silterra's 130nm CMOS and a certain part of the circuit types such as Class E, parallel multi-cascode PMOS stages, capacitors parallel and combiner load resistor had been implemented with supplying voltage of 1.3V to obtain the results of each of the parameters. Each part of the elements contributes functionally based on each of their functions. Therefore, small calculations are needed to obtain the specific value of parameters. Thus, other concepts were all simulated regarding the output waveform of the circuit. By testing and simulating the circuit, the results of two types of simulation had been obtained. In the AC analysis, the output is to obtain the frequency of the circuit. The bandwidth of the circuit obtains and is produced in the 5G region which is 24GHz to 100GHz. Bandwidth is the amount of data that will transmit across the network. The larger the amount of data that can be transferred, the higher the quality of the product development. If the frequency is in the range of 5G region, the data will be kept and forwarded to data analysis but if the range of the bandwidth does not achieve the requirement of a 5G region network, the values of the components need to be changed due to the effect of the performance.

Besides that, the transient analysis will simulate the circuit to obtain the results for output power, the efficiency of about 100% and gain near 1. If the results do not achieve the performance of the 5G network, the steps are similar to the AC analysis where the value of the components needs to change to achieve the target of the 5G region. Thus, the data will be kept when the performance parameters are acceptable. All of the

data will be analysed and checked whether it is a balance to be implemented in an integrated circuit (IC). If the data are available to use, the process will continue but if the data are not well balanced, the circuit and the

values of the component need to be changed due to the impact of the results obtained. Through these processes, a lot of changes were made to require balances for both simulations to fully complete the circuit.

3.2 Outphasing Power Amplifier Diagram

According to Figure 4, the circuit was created with an AC source as the input supply to generate the power amplifier's frequency. The outphasing power amplifier, which contains two power amplifiers, will be used to amplify the signal after it has been separated into its component parts using the Signal Component Separator (SCS). This amplifier improves performance at low output power amplitudes by simulating input signal period saturation in each of the amplifiers. Branch-level PA cells with high peak efficiencies.

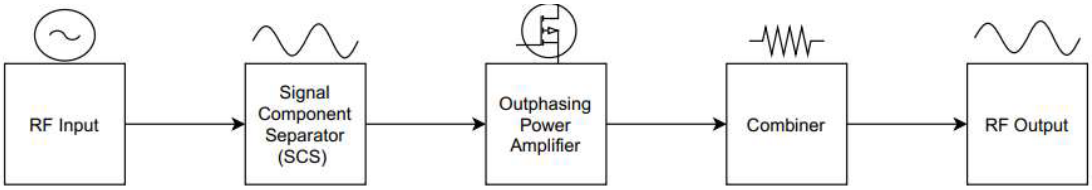

Figure 4: Block Diagram of the Outphasing PA.

In essence, Chireix's outphasing PA system can be used as an efficiency-enhancing strategy to deliver high-efficiency performances. The output signal will then combine into the combiner to provide the output parameters needed in the 5G network region after the signal has been split between each of the two outphasing power amplifiers. Both the PAs and the power combiner must be efficient over the obtained bandwidth in order to maintain high efficiency in a wide PA bandwidth. Class E is a flexible and compatible class that can be used to configure amplifiers for network operation.

As a result, the overall system can be highly linear over the spectrum of signal levels provided by the SCS and power combiner that do not induce non-linear signal distortion. For outphasing amplifiers, stronger high-level efficiency PAs or also constant-amplitude phase-locked oscillators can be used to perform linear amplification.

Figure 5 shows the whole schematic circuit of an outphasing RF power amplifier. It consists of multi-cascode amplifiers, a Class E circuit, combiner that acts as an output stage. The cascode amplifiers contain PMOS transistors with the size of W=14µm and L=130nm for the first stage while in the second stage of the cascode amplifiers contain PMOS transistors with the size of W=24µm and L=130nm, similar to the last stage of the cascode amplifiers. Different sizes of transistors affect the performance and efficiency of the circuit. Through these components, the voltage supplied for the circuit is 1.3V. The voltage supply for the circuit is sufficient as the features can be upgraded to a low voltage which saves power consumption. Therefore, through this simulation, the voltage supplied needs to provide a power supply for each of the cascade amplifiers stages to obtain the output waveform.

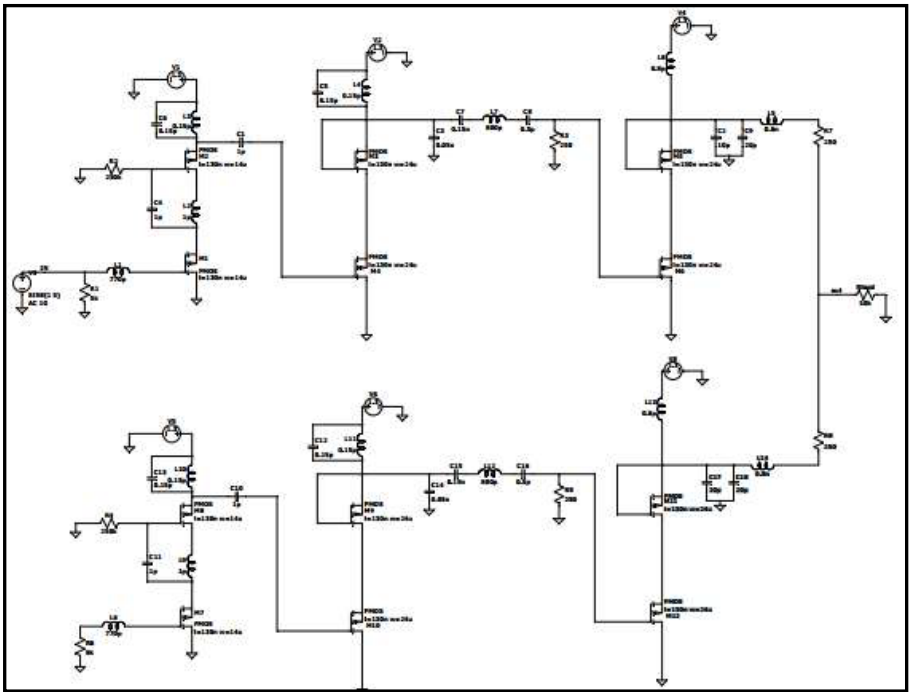

Figure 5: Outphasing Power Amplifier.

3.3 Class E Amplifier

Class E stages as shown in Figure 6 are non-linear components where it contributes to achieving efficiencies of about 100% while providing full power. Class E amplifiers deal with the finite input and output transition times by load design. In order to maintain the efficiency of the circuit, the Class E stage consists of an output transistor, M3 followed by their own sizes featured. Then, it also contains a grounded capacitor or acts as a shunt capacitor, C3 and a series network C7, L7 and C8. Technically, the capacitor, C5 parallel with the inductor, L4 is to supply the PMOS high frequency and signals to give achievable bandwidth at the Rload.

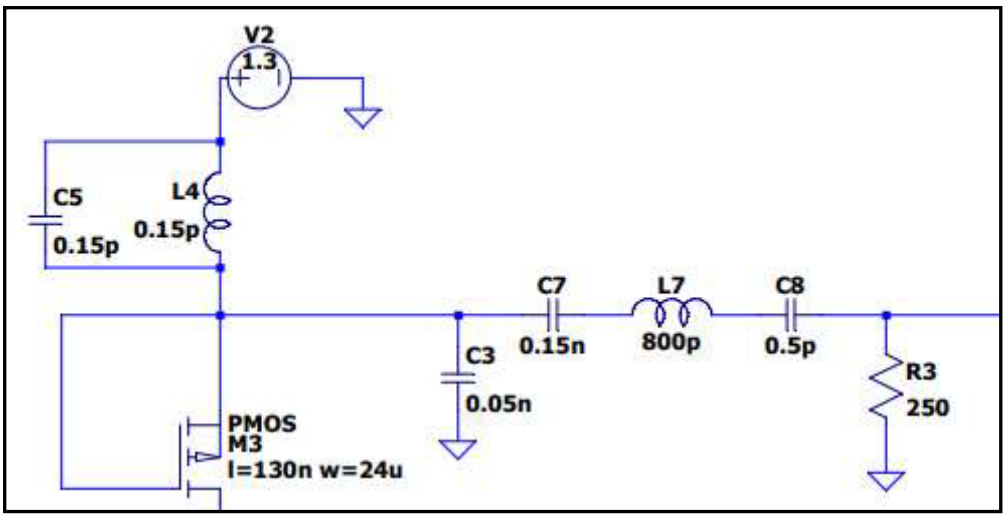

Figure 6: Part of the Class E used in the circuit

3.4 Multicascode amplifiers

Essentially, the typical outphasing PAs are at the drawback of reducing the efficiency with power back-off capacity. The multi-cascode outphasing PA is introduced in this simulation circuit to increase performance at low power levels by switching between various configurations. Figure 7

shows the connection from the first stage of the multi-cascode amplifier to the next stage, the capacitor was added at the center between the stages. This is to maintain the power consumption obtain between both stages.

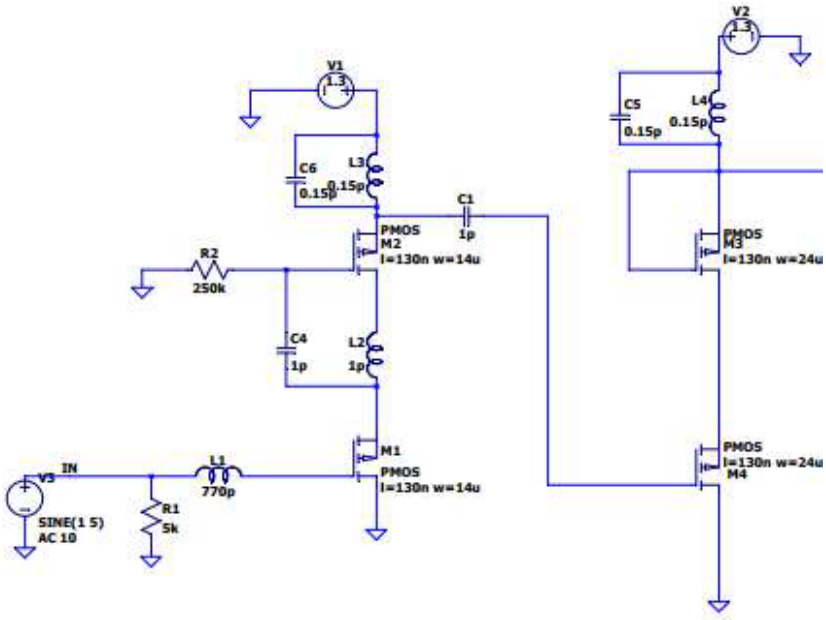

Figure 7: Part of multi-cascode amplifier stages.

As the capacitor functions to store and discharge the electricity in a circuit. Moreover, it also flows an AC without passing the DC. The capacitors can handle power loss efficiently and produce power production at a low cost. Meanwhile, for a circuit containing the inductors, the component is capable of storing electrical energy in the form of magnetic energy storage devices in a variety of switched-mode DC power supplies. The inductor has an opposite feature to the capacitor where the current flowed during the "off" switching time which allows topography when the voltage is greater than the input voltage.

4 Result and Discussion

4.1 Simulation Results

The outphasing PA used Silterra's 130nm CMOS process with a voltage supply of 1.3V to the circuit. Based on Figure 8, wave A is the magnitude of the bandwidth frequency of the waveform which is in the range from 30GHz to 50GHz while wave B is the phase of the frequency waveform. At the rise peak edge of wave A, wave B increased proportionally when it reached over 10GHz as the performance is affected by the capacitors, inductors and the combined amplifiers from the circuit. The measurement of the bandwidth can be identified accurately using the LtSpice command.

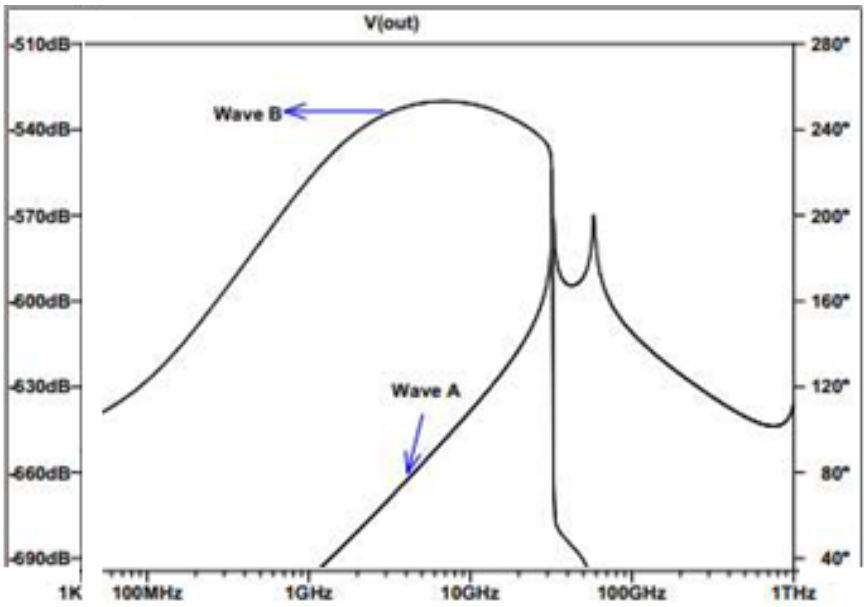

Figure 8: Bandwidth waveform of the outphasing PA

Therefore, the range of bandwidth is from 32.42GHz to 58.54GHz and the average is 26.12GHz, as proved in Figure 9. By referring to the data range of the 5G bandwidth network which is from 24GHz to 100GHz, the outphasing circuit bandwidth is achievable to be implemented for the performance of the 5G network. Furthermore, due to the effect of the bandwidth throughout the circuit, the input power and output power also can be measured using the LtSpice command to generate accurately the values of the power from the waveform. Thus, the input power is 200µW and the output power is 164.83µW.

```
tmp: MAX(mag(v(out)))=(-569.933dB,0°) FROM 1000 TO 1e+012
bw=2.61197e+010 FROM 3.2422e+010 TO 5.85417e+010
```

Figure 9: Measurement range of bandwidth and average

4.2 Calculated Result

The formula for calculating the efficiency of the circuit is by taking the data from the input power and output power as shown in (1) below:

$$\eta = \frac{P_{out}}{P_{in}} X\ 100\% \qquad (1)$$

Hence, the value of the efficiency is 82.42% which is in better transitions because the high performance of efficiency is 100% which cannot be obtained due to any defect that occurs in the circuit. Therefore, the data are highly recommended almost to perfection.

$$gain = \frac{V_{out}}{V_{in}} \qquad (2)$$

Next, the formula stated in (2) is to obtain the gain from the circuit design. The value for Vout is 1.28V while Vin is 1V. In order to get the precision value of the gain is 1, therefore, the gain of the circuit design is 1.28 which is only a 28% of increasing and considered in low voltage region as shown in Figure 10.

```
pin: AVG(-v(in)*i(v3))=0.0002 FROM 0 TO 0.1
pout: AVG(v(out)*i(rload))=-0.000164831 FROM 0 TO 0.1
eff: pout/pin=-0.824155
gain: v(out)/v(in)=1.28395
```

Figure 10: The value for efficiency and gain proven

4.3 Performance Analysis

Table 2: Performance comparison of PAs

Reference	Frequency	Technology	Classification	Vdd
This work	26GHz	130nm CMOS	Class E	1.3V
[23]	18GHz	130nm CMOS	Class E	1.5V
[23]	20GHz	130nm CMOS	Class E	1.5V
[18]	3.5GHz	130nm CMOS	Class F	1.1V
[24]	850MHz	130nm CMOS	Class E	1.1V

Comparing the outphasing circuits of Class-E and Class-F based on Table 2 reveals that they differ depending on the circuit design and Vdd power supplied using the same technology. Therefore, it is demonstrated in this project that theoretically, the frequency can be obtained at higher values than other frequencies, even though frequency results can vary depending on the type of circuit implementation used in the circuit. The value of each component is tested throughout the tested circuit design and encounters numerous mistakes. By observing the multi-cascode process from stage to stage and deducing the capacitors and inductors, it is possible to spot the faults that occur in the circuit design.. Additionally, several types of circuits are employed in part to improve the circuit's performance and effectiveness in order to reach the 5G region's aim.

5 Conclusion

As for conclusions, the outphasing circuit amplifier project's goals have been accomplished. The statistics from the AC analysis are all within the permitted limits of a 5G network. In the LtSpice software, the amplifier's circuit architecture is well illustrated. Fundamentally, this circuit design is based on theory, with each of the output parameters—bandwidth, efficiency, output power, and gain—being obtained through simulations. This is supported by measurements made using the LtSpice software, which has been calculated and verified. The implementation of this outphasing PA circuit can be improved by observing it in action and measuring the output using an oscillator or other measurement tools. If the measured process resembles the theoretical process, thus the circuit can proceed into the layout process which can be implemented in the IC. Therefore, the outphasing RF power amplifier can be used to be part of the 5G wireless network and IOT applications.

6 Availability of Data and Material

Data can be made available by contacting the corresponding author.

7 Acknowledgement

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