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The Design of Power Harvester for Passive RFID Tags

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Abstract

This paper presents the design of a power harvester for passive RFID Tags. An impedance matching circuit chooses a high-pass L network inserted between the antenna and rectifier circuit to maximize the power transferred to Tags, using an impedance transformation technique. A simple circuit including only a shunt inductance was selected as a matching. The rectifier utilizes a Self-Vth-Cancellation (SVC) circuit is an archived self-threshold voltage cancellation and self-power regulation function with a simple circuit design. An antenna is modeled as an RF source with a series impedance Z_S of 50Ω while the rectifier is modeled as a load impedance Z_L, which is estimated from the process and design parameters of the NMOS and PMOS transistors used in the SVC rectifier. As the combined circuit was simulated using input in the UHF band of 953 MHz and the devices' model of the 0.35μm CMOS technology. The simulation results were compared with the single-stage rectifier of the SVC technique in the issue of the Power Conversion Efficiency (PCE). The achieved DC output of the rectifier yields the power conversion efficiency of 43.7% at input RF power -10.22dBm while a DC output voltage of around 643.8mV and a current load of 64.4μA.

Keywords: Power Harvester; Passive RFID Tag; Power Conversion Efficiency; Matching Circuit

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1. Introduction

Energy harvesting is the process in which energy is derived from a system's environment and converted into usable electric power. Energy harvesting allows electronics to operate where conventional power sources are not available without the need for frequent wiring or battery replacement. Energy storage from the environment is an attractive alternative to battery-operated systems. Especially for long-life electronic systems, low-power consumption, and can be self-sustaining.

An energy harvesting systems generally consist of circuits to charge the energy storage cells and manage the energy by providing control and protection. The efficiency and potential of energy storage devices are highly dependent on the efficiency and specific properties of the material. Examples of energy sources are radio energy, light, temperature differences, vibration or pressure, and even biochemically produced energy.

Nowadays, the development of power harvesting in the technology of Radio Frequency Identification (RFID) has been increasingly applied in various application domains such as security, robot, warehouse, transportation management, IT asset tracking, animal management, medical management, and others [1], [2].

The RFID technology can be seen that these devices have played a very important role in the development of economy and human.

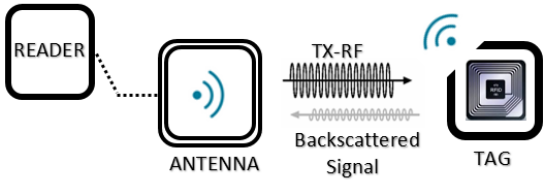

Fig. 1 RFID Systems

An RFID system consists of a reader unit and RFID tags, also called transponders, as shown in **Fig. 1**. The RFID systems use the principle of communication with the transfer of data between the reader unit and moveable objects or tags, via propagation of electromagnetic waves between a reader and tags. Tags can be divided into three type's active, semi-passive, and passive tags depending on the power for RF transmission and signal processing. Active tags need a battery to supply power for RF transmission and signal processing unit. Active tags are appropriate for applications that need to transmit data in a long-range transmission such as wireless sensor networks. However, active tag costs are high and complexly fabricated. On the other hand, an advantage of a passive tag does not need a battery. As a result, passive tags can be produced at low cost, small size, low maintenance, and high volume [3]. In between these two types, semi-passive tags need a small battery for signal processing while using the induced RF power for the transmission. **Table 1** concludes with a comparison of the RFID types [4].

Table 1 Comparison of active, semi-passive, and passive RFID tags

Limitations	Tag type		
	Active	***Semi-passive***	***Passive***
Distance of communication	Long	Moderate	Short
Incorporation of sensor	Easy	Possible	Difficult
Necessity of Battery	Require	Require	Not require
Volume	Large	Moderate	Small
Cost	High	Moderate	Low
Maintenance	Require	Require	Not require

In this paper, the passive tag was selected for implementation because of its advantages such as can be produced at low cost, small size, low maintenance, and high volume. An experiment design was used to apply and discover the main factors affecting the RFID interrogation range. The anti-collision mechanisms are applied for avoiding or solving collisions due to interference that might occur among readers and tags [5], [6].

This paper can be classified as follows: Section 2 introduces the research methodology. In Section 3, the circuit design and analysis are described by reference to the analysis of conventional NMOS-based rectifier circuits, and the conceptual design of the research. The circuit design and simulation results are proposed. Finally, Section 4 concludes the paper.

2. Research Methodology

This section explains the research methodology which can be divided into four sub-sections including a basic theorem on communication range, motivation, a general problem in power harvester, and a problem statement, which are introduced as follows:

2.1 Communication Theorem

In general, an RFID system uses an operating frequency in the Industrial Science and Medical (ISM) band. The RFIDs can be categorized from a range of RF frequencies. HF band (13.56MHz) is coupled for power and data transfer utilizes near-field magnetic, but still has communicated distance of short-range. Therefore, a high-frequency range, such as far-field electromagnetic wave transmission, Ultra-High Frequency (UHF) band (860-960MHz) has been used more because it needs smaller antenna and can communicate in a longer range [7]. The theoretical communication range R is determined from the Friis transmission equation (1) [8]:

$$R \leq \frac{\lambda}{4\pi}\sqrt{\frac{EIRP_{reader}G_{tag}\eta_{rectifier}}{P_{tag}}} \qquad (1)$$

Where R is the communication distance, $EIRP_{reader}$ is the "Effective Isotropic Radiated Power" of a reader unit, G_{tag} is the tag antenna gain, P_{tag} is the power required for the tag operation, and $\eta_{rectifier}$ is the Power Conversion Efficiency (PCE) of the "Radio Frequency to Direct Current" called RF-DC rectifier. From equation (1), it is obvious that they are many ways to increase the communication distance between a reader and tags.

Firstly, equation (1) can increase the reader's power which in turn increases an $EIRP_{reader}$. Secondly, can increase the antenna gain (G_{tag}). Next, attempt to reduce the power consumption of tag operations and finally, can increase the PCE of the rectifier circuit or using the impedance matching network. The power harvester unit consists of a matching network and rectifier circuit shown in **Fig. 2**.

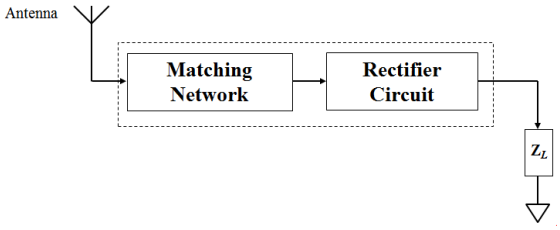

Fig. 2 Block diagram of power harvester unit

2.2 Motivation

Improving the PCE is the most important technique to increase the communication distance, refer to equation (1). Firstly, because an $EIRP_{reader}$ is usually limited by regional regulations, such as not over $4W_{EIRP}$ for the US and Japan, is the maximum transmitted power, as G_{tag} is almost determined by the allowable antenna area, such as about 1.64 for *λ/2* dipole antenna [8], and P_{tag} is also determined by the functions implemented in the tag. In general, it varies from 10 to 100μW, an internal block diagram of the RFID tag is shown in **Fig. 3**. The best PCE from the previous works is about 38% at a practical $EIRP_{reader}$ [9]. Moreover, the PCE is less than 30% for most conditions. Therefore, there is room for improvement. Based on these reasons, this research an interested in improving the PCE on the power harvester units when there is a weak RF input signal.

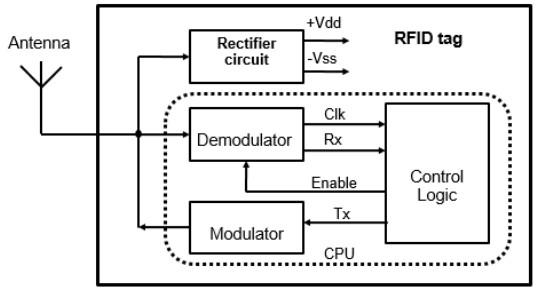

Fig. 3 Block diagram of the RFID tag

2.3 General Problem in Power Harvester Unit

As shown in **Fig. 2** and **Fig. 3**, a power harvester unit consists of a dipole antenna, matching network, and rectifier circuit. Given an antenna, designing a power harvester involves characterizing both the impedance network and the rectifier circuit in order to choose optimal parameters which lead to achieving maximum sensitivity of the circuit. Since the output impedance of the antenna is not usually match well with the input impedance of the rectifier, the matching circuit is used to maximize the power transfer from the antenna to the rectifier. The fundamental problem regarding the design of a matching circuit is the change of rectifier's input impedance due to variation of active devices' operating points. This variation is because of the changes in the RF signal level at its input and the DC load.

The rectifier's circuits convert an AC signal to a DC signal. For the rectifier in an RFID tags, the fundamental problem is two folds. Firstly, the frequency of the AC signal is very or ultrahigh. This leads to the difficulty of designing or choosing active switching devices. Secondly, the level of the input RF signal is very low. This leads to the problem of turning on the active switches and increasing the DC voltage level.

Traditionally, a voltage multiplier circuit based on multiple-stage voltage doublers [10], as shown in **Fig 4** is applied to increase the DC voltage level.

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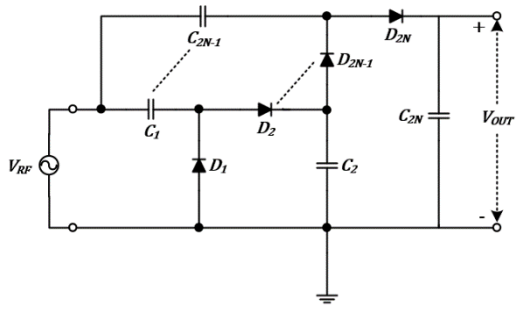


Fig. 4 An N-stage voltage doublers

For, N-stage voltage doublers, the output DC voltage is approximately obtained by equation (2) [11].

$$V_{out} = N(V_{RF} - V_{th}) \quad (2)$$

Where V_{RF} is a peak of the input RF signal and V_{th} is a threshold or turn-on voltage of the chosen switching devices. Most of the previous work has focused on designing multistage multiplier circuits. The first technique is to improve the PCE value by reducing the threshold voltage (Vth) of the switching devices, of which Schottky diodes were shown to be the best choice. The other techniques used so-called Vth-cancellation techniques in which MOS transistors are used as switching devices. The MOS-based rectifiers are more attractive because the fabrication process is the same as that of the processing unit.

2.4 Problem Statement

The main problems of power harvester design using a Vth-cancellation based rectifier are (1) how to design a Vth-cancellation technique, and (2) how to design a maximal-power-transfer by using impedance matching. In this research, the Vth-cancellation based CMOS rectifier proposed by K. Kotani, et al. [8] and [9] is adopted as the rectifier part because of its strength of threshold voltage cancellation and simple design. Then, the research problem is how to design a matching circuit inserted between an antenna and the rectifier circuit.

This paper proposed a design of a power harvester for the passive RFID tags. When, an external matching unit is put on the first stage of the rectifier circuit to maximize the power delivered to a tag, as block diagram shown in **Fig. 2**. From the previous works, the focus of power harvester design for increasing PCE has been on either rectifier or matching circuits. For a rectifier, the main problem is the turn-on or threshold voltage of the diodes used in the rectifier. The differential-drive technique, called "cross-coupled bridge configuration" is proposed [9]. This circuit has completely

the largest efficiency as the differential-drive technique needs no additional diodes and external battery. However, the reported differential-drive technique is just assumed for the analysis of rectifier circuits under the condition of perfect impedance matching. With reconsider to the impedance matching with an antenna, a matching circuit needs to design so as to match this impedance to complete the largest total efficiency [10]. Therefore, in this research two interesting techniques are the Self-Vth-Cancelation (SVC) technique [8], [9] and the L-Matching technique [11], because the SVC technique is simple design when compared with the differential-drive technique, As a result, the SVC is the most advanced conventional voltage booster. The SVC, on the other hand, maintains a reverse leakage current at the high RF signal voltage range, which still affects the low voltage across the low input signal range. Therefore, this research attempts to combine the two techniques, SVC and L-Matching, due to their simplicity and optimal design with passive tags.

The challenges of this problem are two folds. Firstly, the rectifier's input impedance, which acts as the load of the matching circuit, changes due to both RF input and load impedance changes. Secondly, the designed matching circuit must be able to maximize the power transfer to the rectifier and minimize reflections from the antenna input port. In other words, the matching circuit's area can be automatic tuning, which is a challenge because it is utilized to analyze the influence of the dynamic load on the performance of the power harvesting circuit.

3. Circuit Design and Analysis

3.1 Matching Network

The matching network functions impedance transformation to convince maximum power transfer [11] and [12]. **Fig. 5** shows the part of the impedance transformer where V_{in} and Z_{in} are the induce voltage and input impedance of the impedance transformer respectively. The part of the output side consists of the input voltage and input admittance defined by V_{IC} and Y_{IC} of the rectifier respectively.

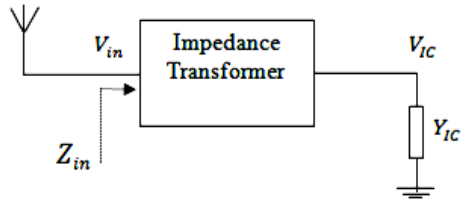


Fig. 5 The picture does not need frame

Assume the impedance transform is comprised of reactive component and lossless.

$$V_{IC} = \left(\sqrt{Re\{Y_{in}\}/Re\{Y_{IC}\}}/2\right)V_{IN} \quad (3)$$

$$Re\{Y_{in}\} = (1 + Q^2)Re\{Y_{IC}\} \quad (4)$$

A quality factor of the matching network at resonating frequency is the Q variable. For a matching network used L-type topology to consider, that when a lossless network consisted of L and C, $Q = \omega_0 C/Re\{Y_{IC}\}$ was defined. Where

ω_0 is the resonate frequency. Therefore, the input of the rectifier is determined as

$$V_{IC} = \left(\sqrt{1 + Q^2/2}\right)V_{IN} \quad (5)$$

A high Q is required in order to achieve a high voltage gain. Nevertheless, Q is realistically determined by the compromises between several design parameters such as characteristics of the antenna, the system bandwidth, and the input impedance of the rectifier.

3.2 Analysis of Conventional NMOS-based Rectifier Circuit

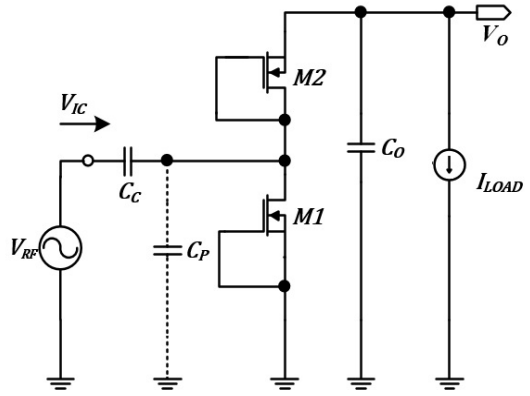


Fig. 6 Simplified model of a single-stage NMOS-Based rectifier

Fig. 6 shows the simplified model of a single-stage NMOS-Based rectifier [13]. The DC output equation of an ideal one-stage circuit for conventional NMOS rectifier is $2(V_{IC} - V_D)$, where the gate-source voltage V_D is not constant but, in actuality, determined by the drain current, the reverse bias leakage current, the parasitic components, and the body effect. Hence, the DC output voltage of the one-stage rectifier can be expressed as

$$V_O = 2(\beta V_{IC} - V_{in} - V_{loss}) \quad (6)$$

When the value of

$$\beta = C_C/(C_P + C_C) \quad (7)$$

When C_C is the plate capacitance and C_P is the sum of parasitic capacitance at the source. The value of V_{loss} is voltage loss resulting from the current loss which is dependent on I_{LOAD} as well as the transistor reverse-biased leakage current. In consequence, for an n-stage rectifier, the output voltage can be expressed as

$$V_{O,N} = 2N(\beta V_{IC} - V_{in} - V_{loss}) \quad (8)$$

As a result, find the integrated relationship between the input power at the antenna and the output voltage of the rectifier as equation (9).

$$V_{O,N} = 2N(\beta\sqrt{2P_\gamma \,\mathrm{Re}\{Z_{IC}\}} - V_{in} - V_{loss} \quad (9)$$

Note that V_{loss} will increase followed by *N* because, with larger *N*, the parasitic components would cause extra losses. Thus, as *N* increases, the growth rate of $V_{O,N}$ drops; as a result, $V_{O,N}$ will not always increase along with *N*. In the other word, the resistance of the input impedance $Re\{Z_{IC}\}$ of the rectifier decreases with increasing *N* due to the parallel structure of the rectifier.

3.3 Conceptual Design of the Research

The concept and design of the research are arranged as follows. The act

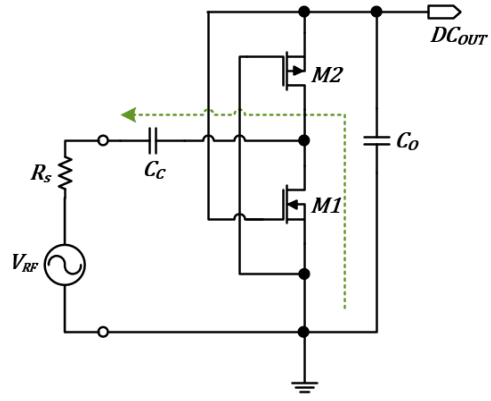
of the SVC is described in section 3.3.1, the L-Matching selected as a matching circuit design, presented in section 3.3.2, starts with a brief on the SVC-Based CMOS rectifier circuit combined with the matching unit and continues with the design of the proposed rectifier in section 3.3.3. Simulation and results are presented and discussed in section 3.3.4, followed by conclusions in section 4.

3.3.1 The SVC Rectifier Circuit

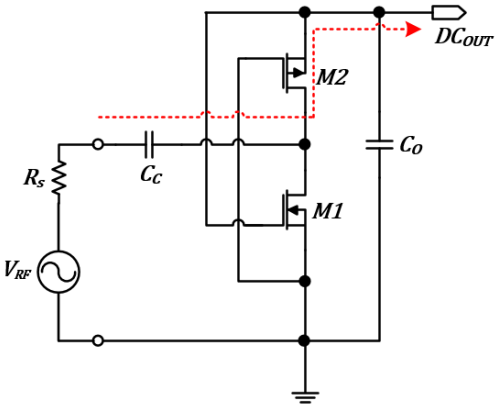
K. Kotani and T. Ito proposed [8] adapted a CMOS rectifier stage to achieve Self-Vth-Cancellation (SVC). The schematic shown in **Fig. 7** has an adapted rectifier circuit with SVC technique. RF input signal can model each stage of the CMOS rectifier as NMOS and PMOS transistors in parallel, of which one is in the turn-on stage for the saturation region and the other is in the turn-off stage for the cutoff region, as shown above, **Fig. 7**. A diode-connected NMOS is in the saturation region when V_{GS}, which is equal to V_{DS}, is greater than Vth; else, it is cut off. Therefore, in the negative half of the signal, the transistor NMOS is in the saturation region and the transistor PMOS is cut off as shown in **Fig. 7(a)**. The opposite is true for the positive half of the signal as shown in **Fig. 7(b)**.

3.3.2 The Design of Matching network

The matching network functions impedance transformation to convince maximum power transfer. A very simple circuit including only a shunt inductance was selected as a matching circuit. Then, the SVC rectifier was characterized to get all parasitic capacitances and resistances all parts as shown in **Fig 8**.



(a) Negative phase, NMOS turning on



(b) Positive phase, PMOS turning on

Fig. 7 Diode connected NMOS and PMOS (a) Negative phase (b) Positive phase

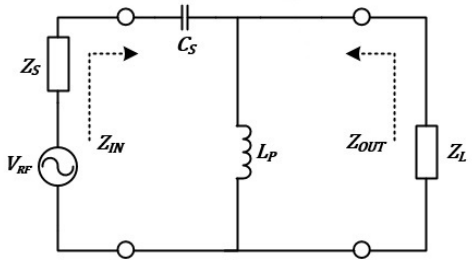


Fig. 8 Schematic of the L-Matching circuit

Fig. 8 shows the schematic of the L-Matching circuit. The aim of designing an L matching network is to deliver maximum power transfer at 953 MHz. In this design, the antenna is modeled as an RF source with internal series impedance Z_S of 50Ω. On the output side of the matching circuit, the input impedance of the rectifier is considered as the complex impedance Z_L. The lossless network with only reactive components is achieved by setting the complex output impedance of the network Z_{OUT} to be equal to the complex conjugate of the load impedance Z_L and the input impedance of the network Z_{IN} to be the complex conjugate of the source impedance Z_S calculates from equation (10), and (11).

$$Z_{IN} = Z_S^* \tag{10}$$

$$Z_{OUT} = Z_L^* \tag{11}$$

To obtain equation (10) and (11), we ignore the series resistance of the inductors and the capacitors [8], [9]. While the value of Z_{IN}, and Z_{OUT} is shown in the following equation.

$$Z_{IN} = \left(\left(Z_L \| j\omega L_P \right) + \frac{1}{j\omega C_S} \right) \tag{12}$$

$$Z_{OUT} = \left(\left(Z_S + \frac{1}{j\omega C_S} \right) \| j\omega L_P \right) \tag{13}$$

For, the requirement of high Q in order to achieve a high voltage gain. However, Q is realistically determined by the compromises between several design parameters such as characteristics of the antenna, the system bandwidth, and the input impedance of the rectifier.

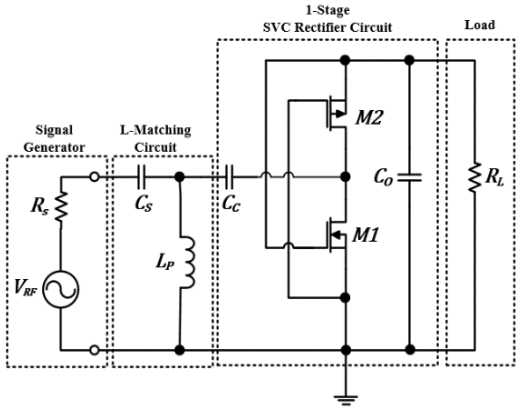


Fig. 9 Schematic of the 1-stage SVC Rectifier with L-Matching circuit

3.3.3 Proposed Circuit Design

This paper proposes a design of a power harvester for passive RFID Tags. Then, the matching unit is put on the first stage of the SVC rectifier circuit to maximize the power delivered to a tag, as the schematic shown in **Fig. 9**. From the previous works, the focus of power harvester design for increasing PCE has been on either rectifiers or matching circuits. Therefore, this research work tried to combine the two techniques, SVC rectifier, and L-Matching circuits, because of their simplicity and suitable design with passive tag.

In the first step, the value of Z_L in the matching circuit is calculated using the RF Impedance Matching Network Designer Tool to determine the matching circuit parameters [14]. An antenna is modeled as an RF source with a series

impedance Z_S of 50Ω while the rectifier has modeled as a load impedance Z_L, which is approximated from the process and design parameters of the NMOS and PMOS transistors used in the SVC rectifier. Both of these impedances are used to find optimal matching parameters of the chosen L matching circuit.

In the second step, the parameters of the rectifier circuit is taken from [8], and [9], presented by the design and fabrication of an SVC CMOS rectifier using 0.35µm CMOS 2P3M technology. Where the parameters of the SVC circuit used in the design are obtained from actual measurements of the impedance of the input rectifier's Z_{RECT}, including the coupling capacitor C_C of 4pF and the filter capacitor C_O of 7.8pF while the parameters of the L-Matching circuit can be calculated as a capacitor C_S of 0.82pF and an inductor L_P of 35.72nH.

3.3.4 Simulation Result

To estimate the proposed design, the circuit simulations using the LTspice of the Linear Technology Corporation and the Electric VLSI Design System are supported using the proposed circuit [15], [16], and [17]. The RF input voltage is set V_{IN} as the various around 380mV$_{rms}$ until to 770mV$_{rms}$ for the testing power delivery to load, as a summary of the power conversion efficiency (PCE %) displayed in **Table 2**.

From **Table 2**, PCE is the power conversion efficiency proposed in SVC with an L-matching circuit. Therefore, the percentage of PCE [%] can be calculated as follows in equation (14).

Table 2 Summary of the power conversion efficiency (PCE %)

V_{IN} (mV)	P_{IN} (µW)	V_{OUT} (mV)	I_{OUT} (µA)	P_{OUT} (µW)	PCE %
380.4	6.8	31.4	3.1	0.1	1.4
484.8	34.0	236.9	23.7	5.6	16.5
581.1	94.9	643.8	64.4	41.4	43.7
611.1	250.0	783.8	78.4	61.4	24.6
648.0	463.4	862.5	86.3	74.4	16.1
690.6	697.0	918.7	91.9	84.4	12.1
737.4	976.7	963.8	96.4	92.9	9.5
769.3	1230	1000	100.4	100.9	8.2

$$\text{PCE}[\%] = \left[\frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{OUT}}{P_{IN}} \right] \times 100 \qquad (14)$$

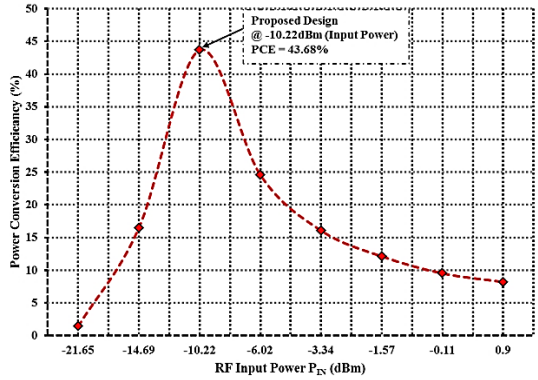


Fig. 10 Measured PCE (%) as a various RF input power

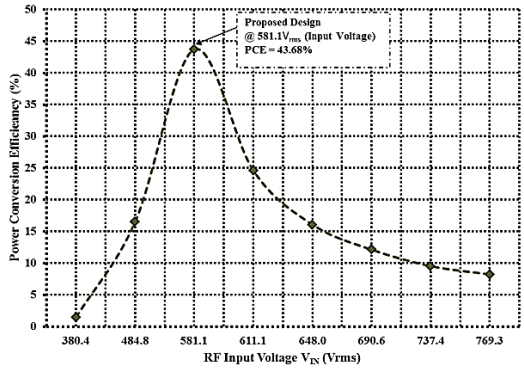


Fig. 11 Measured PCE (%) as a various RF input voltage

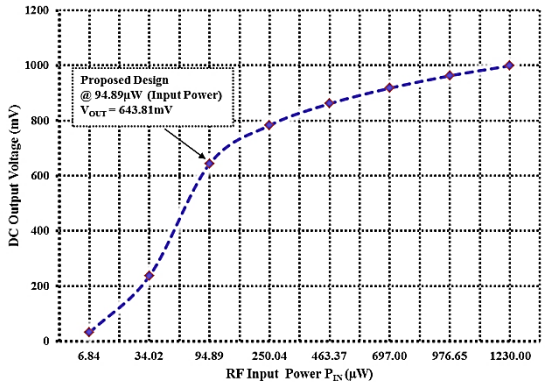


Fig. 12 Measured DC output voltage as a various RF input power

4. Conclusion

Results of the simulations are provided in **Fig. 10**, **Fig.11**, and **Fig 12**. This proposes a design procedure of a power harvester for a passive tag. The idea proposed in this research is to insert an effective L matching circuit type given that an antenna and rectifier are chosen. **Table 2** concludes the results in terms of power conversion efficiencies. The results show that DC load change has smaller effects than does the input RF power, by comparing the simulation results with the conventional SVC technique on the PCE issue. In **Table 2** and graph **Fig. 10-12**, the DC output of the rectifier yields the power conversion efficiency of 43.7% for the input RF power -10.22dBm at the output voltage of 643.8mV and the output current 64.4μA which corresponds to the output power of 41.4μW, as the load resistance connected with a 10 kΩ resistor.

5. Acknowledgement

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