ภาคผนวก

ภาคผนวก ก

โปรแกรมฝึกโครงข่ายประสาทเทียม

```
%Train Back-Propagation Neural Networks for current controller in Active Power Filter.
%3 input(3x8 patterns), 1 hidden layer(5 units), 3 output(3x8 patterns)
%3-5-3
echo off
clear
%P defines 3x8 input vectors:
P = [1 -1  1  1  1 -1 -1 -1;
   1  1 -1  1 -1  1 -1 -1;
   1  1  1 -1 -1 -1  1 -1];
 %T defines the associated 3-element targets:
T = [1  -1   1   1   1  -1  -1  -1;
   1   1  -1   1  -1   1  -1  -1;
   1   1   1  -1  -1  -1   1  -1];
 %Plot input vector(P) and target vector(T)
%plot(P,T,'+');
title('Training Vectors');
xlabel('Input Vector P');
ylabel('Target Vector T');

%DESIGN THE NETWORK
%=================================================================
%A two-layer tansig/tansig networks will be trained.
%The number of hidden TANSIG neurons should reflect the complexity of the problem.
S1 = 5;
%INITFF is used to initialize the weights and biases for the tansig/tansig network.

[w1,b1,w2,b2] = initff(P,S1,'tansig',T,'tansig');

%TRAINING THE NETWORK
%=================================================================
%TRAINBPX uses backpropagation to train feed-forward networks.

df = 10;                    %Frequency of progress displays (in epochs).
me = 50000;                 %Maximum number of epochs to train.
eg = 0.000001;              %Sum-squared error goal.
lr = 0.1;                   %Learning rate.
tp = [df me eg lr];
%Training begins...please wait (this takes a while!)...
[w1,b1,w2,b2,ep,tr] = trainbp(w1,b1,'tansig',w2,b2,'tansig',P,T,tp);
%...and finally finishes.
```

```
%TRAINBP has returned new weight and bias values, the number
%of epochs trained EP, and a record of training errors TR.
%USING THE PATTERN ASSOCIATOR
%=============================================================
%We can now test the associator with one of the origonal
%inputs, [1;1;-1] , and see if it returns the target, [1;1;0].
p = [1;1;-1]
a = simuff(p,w1,b1,'tansig',w2,b2,'tansig')
%The result is fairly close.  Training to a lower error
%goal would result in a closer approximation.
echo off
disp('End of Train_BP_tan.m')
%train_bp_tan.mat


%w1 =
%   1.0243   0.2292   1.1732
%  -1.8007  -0.2161   0.4498
%   0.3395  -1.9305   0.4748
%  -0.3453   0.7187   1.5214
%   1.1155   0.3458  -0.9562
%b1 =
%  -0.0679
%   0.4831
%   0.0834
%  -0.0112
%   0.4069
%w2 =
%   1.5894  -2.5048   0.4874  -0.1813   1.3151
%  -0.2344  -0.2420  -3.6488   0.6789   0.3060
%   2.0552   0.1714   0.6434   2.5816  -0.8976
%b2 =
%   0.0260
%   0.0021
%   0.2365
```

ภาคผนวก ข

โปรแกรมจำลองการทำงาน

โปรแกรมจำลองการทำงานประกอบด้วยการจำลองการทำงานของวงจรกรองกำลังแอกทีฟ โดยใช้วิธีควบคุมกระแสวิธีฮีสเตอริซีสเปรียบเทียบกับวิธีโครงข่ายประสาทเทียม โดยการทำงานของโปรแกรมทั้งสองวิธีมีการเรียกใช้โปรแกรมย่อยได้แก่

ก. apf.m เพื่อคำนวณค่ากระแสของวงจรกรองกำลัง และแรงดันบัสกระแสตรง

ข. conda.m, condb.m และ conc.m เพื่อคำนวณค่ากระแสโหลดเฟส A B และ C กรณีไดโอดนำกระแส

ค. notconda.m, notcondb.m และ notcondc.m เพื่อคำนวณค่ากระแสโหลดเฟส A B และ C กรณีไดโอดไม่นำกระแส

โดยการควบคุมกระแสทั้ง 2 วิธีใช้โปรแกรมการทำงานหลักคล้ายกัน ต่างกันเพียงรายละเอียดของวิธีที่ใช้ในการควบคุมกระแส ซึ่งในภาคผนวกนี้ได้แสดงโปรแกรมหลักทั้งหมดในวิธีฮีสเตอริซีส ส่วนวิธีโครงข่ายประสาทเทียมแสดงเฉพาะส่วนที่แตกต่างจากวิธีฮีสเตอริซีสเท่านั้น

1. วิธีฮีสเตอริซีส

```
echo off
%Frequency 50 Hz.
%Cdc=5000e-6
%Use Hysteresis Band for current controller.
%Use PI controller for control Vdc.
%Use low-pass filter for Vdc (average Vdc from 10 values before).
%Calculation and plot
%1.current of non-linear load >>> Ila, Ilb, Ilc and Inl.
%2.current of APF >>> I_ca, I_cb, I_cc and I_nc.
%3.current of source >>> I_sa, I_sb, I_sc and I_ns after using APF.
%4.voltage at DC bus of Active Power Filter >>> V_dc.
%5.THD of current of non-linear load and source.
%6.Count the switching times of the IGBT.
clear
global Rc Lc;
```

```
%For APF.
global Vsa Vsa_max Ica Ica_ref Icad Vca;
global Vsb Vsb_max Icb Icb_ref Icbd Vcb;
global Vsc Vsc_max Icc Icc_ref Iccd Vcc;
global I_ca I_cb I_cc V_dc I_sa I_sb I_sc I_ns      %Matrix.
global Isa_ref Isb_ref Isc_ref
global Isa_ref_ Isb_ref_ Isc_ref_                   %Matrix.
global Ica_ref_ Icb_ref_ Icc_ref_                   %Matrix.
global Cdc Vdc Vdc_ref Vdca;                        %For DC bus.
global Oi Op Opi                                    %Matrix for PI controller.
                                                    %Oi=Integral controller.
                                                    %Op=Propotional controller.
                                                    %Opi=Propotional+Integral controller.
global hb;                                          %Hysteresis band.
global T zeta;          %Half cycle period of supply current and displacement factor.
global w dt t_start t_stop t_simulation;            %For simulation.
global SAL SAR SBL SBR SCL SCR;                     %Switching function, the value is 0 or 1.
global SAL_ SAR_ SBL_ SBR_ SCL_ SCR_;               %Matirx of switching function.
global count_swa count_swb count_swc;  %For counting the switching times of IGBT.
global count_swa_ count_swb_ count_swc_%Matrix of the counting of switching times.
global Rsa Rla Lsa Cla Vsa Vsa_max;                 %For source and non-linear load.
global Rsb Rlb Lsb Clb Vsb Vsb_max;                 %For source and non-linear load.
global Rsc Rlc Lsc Clc Vsc Vsc_max;                 %For source and non-linear load.
global F start stop N max_freq_display max_sw_  %For plot THD and switching times.
global AA_l BB_l CC_l THD_A_l THD_B_l THD_C_l    %For THD of load.
global AA_s BB_s CC_s THD_A_s THD_B_s THD_C_s   %For THD of source.
%For voltage source.
f=50;
w=2*pi*f;
%Parameter for time.
dt=2e-4;                                            %Time step.
t_start=0;                                          %Start time for simulation.
t_stop=0.1;                                         %Stop time for simulation.
t_simulation=t_start:dt:t_stop;
%Parameter of phase A.
Vsa_max=220*sqrt(2);                                %V source max.
Rsa=1;                                              %R source.
Lsa=0.25e-3;                                        %L source.
Rla=8;                                              %R of non-linear load.
Cla=470e-6;                                         %C of non-linear load.
%Parameter of phase B.
Vsb_max=220*sqrt(2);                                %V source max.
Rsb=1;                                              %R source.
Lsb=0.25e-3;                                        %L source.
Rlb=8;                                              %R of non-linear load.
Clb=470e-6;                                         %C of non-linear load.
%Parameter of phase C.
Vsc_max=220*sqrt(2);                                %V source max.
Rsc=1;                                              %R source.
Lsc=0.25e-3;                                        %L source.
Rlc=8;                                              %R of non-linear load.
```

```
Clc=470e-6;                          %C of non-linear load.
%Parameter for APF.
Rc=0.1;
Lc=3e-3;
Cdc=5000e-6;                         %Capacitor at DC bus.
hb=0.01;                             %Hysteresis band.
Vdc_ref=350;
%Parameter for PI controller.
Kp=1;                                %Proportional band. (no unit)
Ki=20;                               %Integration constant. (per unit)
Oi(1)=0;
Op(1)=0;
Opi(1)=34;
%Initial value and first value for simulation.
Ica=0;
Icb=0;
Icc=0;
I_ca(1)=Ica;
I_cb(1)=Icb;
I_cc(1)=Icc;
V_dc(1)=Vdc_ref;
V_dca(1)=Vdc_ref;
x0=[Ica Icb Icc Vdc_ref]';           %Initial condition of APF >>> [Ica Icb Icc Vdc].
x0a=[0 75]';                         %Initial condition of load phase A >> [Ila VRla].
x0b=[0 120]';                        %Initial condition of load phase B >> [Ilb VRlb].
x0c=[20 150]';                       %Initial condition of load phase C >> [Ilc VRlc].
Ila(1)=x0a(1);
VRla(1)=x0a(2);
Ilb(1)=x0b(1);
VRlb(1)=x0b(2);
Ilc(1)=x0c(1);
VRlc(1)=x0c(2);
Ica_ref=Ica;
Icb_ref=Icb;
Icc_ref=Icc;
Ica_ref_(1)=Ica_ref;
Icb_ref_(1)=Icb_ref;
Icc_ref_(1)=Icc_ref;
I_sa(1)=Ila(1)+I_ca(1);
I_sb(1)=Ilb(1)+I_cb(1);
I_sc(1)=Ilc(1)+I_cc(1);
Isa_ref_(1)=0;                       %Do not use this value for calculating.
Isb_ref_(1)=0;                       %Do not use this value for calculating.
Isc_ref_(1)=0;                       %Do not use this value for calculating.
err_a_(1)=Ica_ref_(1)-I_ca(1);
err_b_(1)=Icb_ref_(1)-I_cb(1);
err_c_(1)=Icc_ref_(1)-I_cc(1);
answer_(1,1)=0;
answer_(2,1)=0;
answer_(3,1)=0;
i=2;                                 %Start simulation at the value number 2,
```

```
                                        %the value number 1 is zero (0).
%Switching function of APF.
%Initial value.
SAL=1;
SAR=0;
SBL=1;
SBR=0;
SCL=1;
SCR=0;
count_swa=0;
count_swb=0;
count_swc=0;
%First value.
SAL_(1)=SAL;
SAR_(1)=SAR;
SBL_(1)=SBL;
SBR_(1)=SBR;
SCL_(1)=SCL;
SCR_(1)=SCR;
count_swa_(1)=0;
count_swb_(1)=0;
count_swc_(1)=0;
options=odeset('RelTol',1e-6);          %Set options of "ode" function.
%*************************************************************************
%*************************************************************************
%*****************************Main loop***********************************
%*************************************************************************
%*************************************************************************
for time=t_start:dt:t_stop
  t0=time;
  t_final=time+dt;
      tspan=[t0 t_final];
 %Calculat Ila, Ilb and Ilc before calculat Ica, Icb Icc and Vdc.
 %*************************************************************************
 %*************************************************************************
 %Condition for Ila.
  Vsa=Vsa_max*sin(w*t0);          %Use for comparing with VRla.
  if x0a(2)<=abs(Vsa)             %When VRla <= Vsa, diode conduct.
                                  %This Vsa is Vsa before the time for calculat=t0.
 %But Vsa that have to use for calculating in this loop is Vsa at t_final.
  Vsa=abs(Vsa_max*sin(w*t_final));          %Set new value of Vsa to 'conda'.
 %xa(1)=Ila is non-linear load current of Phase A drawn from AC main.
 %xa(2)=VRla is voltage across Rla.
  [t,xa]=ode23('conda',tspan,x0a,options);
 %Due to have a lot of "t" value between t0 to t_final
 %in addition to "dt", ode will separate "t" by itself.
 %So xa have a lot of value same as length of t.
 %Then set new initial value,x0a,from final value of xa.
  x0a=[xa(max(length(xa)),1) xa(max(length(xa)),2)]';
  %For keep value of xa,(Ila and VRla) in new matrix name "Ila" and "VRla".
  %And chech condition of Ila, When Vsa is negative, Ila have to be negative.
```

```
Vsa=Vsa_max*sin(w*t_final);              %For check condition.
if Vsa>0
    Ila(i)=x0a(1);
  else
       Ila(i)=-x0a(1);
   end %if

 VRla(i)=x0a(2);                  %x0a(2) is VRla
  else                            %When VRla > Vsa, diode not conduct.
%Calculating new value of VRla when diode not conduct.
%And za is new value of VRla.
 z0a=[x0a(2)];            %Initial value of new VRla is the last value of VRla.
 [t,za]=ode23('notconda',tspan,z0a);
 %Set new initial value,z0a,from final value of za.
 z0a=[za(max(length(za)))];
 %For keep value of z,(VRla) in new matrix name Ila.
 x0a(1)=0;                        %Change initial value of Ila=0.
 Ila(i)=x0a(1);
 x0a(2)=z0a;                      %New initial value of VRla is z0a.
 VRla(i)=x0a(2);
 end %if of Ila.
 %Condition for Ilb.
 Vsb=Vsb_max*sin(w*t0-2*pi/3);
 if x0b(2)<=abs(Vsb)              %When VRlb <= Vsb, diode conduct.
                                  %This Vsb is Vsb before the time for calculate=t0.
 %But Vsb that have to use for calculating in this loop is Vsb at t_final.
  Vsb=abs(Vsb_max*sin(w*t_final-2*pi/3));       %Set new value of Vsb to 'condb'.
  %xb(1)=Ilb is non-linear load current of Phase A drawn from AC main.
  %xb(2)=VRlb is voltage across Rlb.
  [t,xb]=ode23('condb',tspan,x0b,options);
  x0b=[xb(max(length(xb)),1) xb(max(length(xb)),2)]';
  %For keep value of xb,(Ilb and VRlb) in new matrix name "Ilb" and "VRlb".
  %And chech condition of Ilb, When Vsb is negative, Ilb have to be negative.
   Vsb=Vsb_max*sin(w*t_final-2*pi/3);          %For check condition.
   if Vsb>0
     Ilb(i)=x0b(1);
   else
        Ilb(i)=-x0b(1);
     end %if
    VRlb(i)=x0b(2);                %x0b(2) is VRlb.
   else                            %When VRlb > Vsb, diode not conduct.
   %Calculating new value of VRlb when diode not conduct.
   %And zb is new value of VRlb.
   z0b=[x0b(2)];          %Initial value of new VRlb is the last value of VRlb.
   [t,zb]=ode23('notcondb',tspan,z0b);
   %Set new initial value,z0b,from final value of zb.
   z0b=[zb(max(length(zb)))];
   %For keep value of zb,(VRlb) in new matrix name Ilb.
   x0b(1)=0;                      %Change initial value of Ilb=0.
   Ilb(i)=x0b(1);
   x0b(2)=z0b;                    %New initial value of VRlb is z0b.
```

```
VRlb(i)=x0b(2);
end %if of Ilb.
%Condition for Ilc
Vsc=Vsc_max*sin(w*t0+2*pi/3);          %Use for comparing with VRlc.
if x0c(2)<=abs(Vsc)                    %When VRlc <= Vsc, diode conduct.
                                       %This Vsc is Vsc before the time for calculat=t0.
%But Vsc that have to use for calculating in this loop is Vsc at t_final.
Vsc=abs(Vsc_max*sin(w*t_final+2*pi/3));        %Set new value of Vsc to 'condc'.
%xc(1)=Ilc is non-linear load current of Phase A drawn from AC main.
%xc(2)=VRlc is voltage across Rlc.
[t,xc]=ode23('condc',tspan,x0c,options);
x0c=[xc(max(length(xc)),1) xc(max(length(xc)),2)]';
%For keep value of xc,(Ilc and VRlc) in new matrix name "Ilc" and "VRlc".
%And chech condition of Ilc, When Vsc is negative, Ilc have to be negative.
Vsc=Vsc_max*sin(w*t_final+2*pi/3);              %For check condition.
if Vsc > 0
    Ilc(i)=x0c(1);
  else
      Ilc(i)=-x0c(1);
   end %if
    VRlc(i)=x0c(2);                    %x0c(2) is VRlc.
  else                              %When VRlc > Vsc, diode not conducting.
  %Calculating new value of VRlc when diode not conducting.
  %And zc is new value of VRlc.
  z0c=[x0c(2)];                     %Initial value of new VRlc is the last value of VRlc.
  [t,zc]=ode23('notcondc',tspan,z0c);
  %Set new initial value,z0c,from final value of zc.
  z0c=[zc(max(length(zc)))];
 %For keep value of zc,(VRlc) in new matrix name Ilc.
  x0c(1)=0;                          %Change initial value of Ilc=0.
  Ilc(i)=x0c(1);
  x0c(2)=z0c;                        %New initial value of VRlc is z0c.
  VRlc(i)=x0c(2);
  end %if of Ilc
 %Calculating Ica, Icb Icc and Vdc.
%*************************************************************************
%*************************************************************************
Vsa=Vsa_max*sin(w*t_final);
Vsb=Vsb_max*sin(w*t_final-2*pi/3);
Vsc=Vsc_max*sin(w*t_final+2*pi/3);
%*************************************************************************
%Use Hysteresis Band for current control.
%*************************************************************************
%Use the value of Ic_ref and Ic from the previous loop.
err_a=Ica_ref-Ica;
err_b=Icb_ref-Icb;
err_c=Icc_ref-Icc;
k=1;                                %Gain of error
err_a=k*err_a;
err_b=k*err_b;
err_c=k*err_c;
```

```
err_a_(i)=err_a;
err_b_(i)=err_b;
err_c_(i)=err_c;
%Switching function of APF
%phase A
%If even err_a ~< -hb and err_a ~> hb use the previous value of SAL and SAR
%that don't have to declare.
%but, SAL_(i) and SAR_(i) have to declare again (in "else" of second "if" condition).
if err_a<-hb
  SAL=1;
  SAR=0;
  SAL_(i)=SAL;
  SAR_(i)=SAR;
end
if err_a>hb
  SAL=0;
  SAR=1;
  SAL_(i)=SAL;
  SAR_(i)=SAR;
else
  SAL_(i)=SAL;
  SAR_(i)=SAR;
end
%phase B
if err_b<-hb
  SBL=1;
  SBR=0;
  SBL_(i)=SBL;
  SBR_(i)=SBR;
end
if err_b>hb
  SBL=0;
  SBR=1;
  SBL_(i)=SBL;
  SBR_(i)=SBR;
else
  SBL_(i)=SBL;
  SBR_(i)=SBR;
end
%phase C
if err_c<-hb
  SCL=1;
  SCR=0;
  SCL_(i)=SCL;
  SCR_(i)=SCR;
end
if err_c>hb
  SCL=0;
  SCR=1;
  SCL_(i)=SCL;
  SCR_(i)=SCR;
```

```
 else
   SCL_(i)=SCL;
   SCR_(i)=SCR;
 end
%*************************************************************************
%End of Using  Hysteresis Band for current control.
%*************************************************************************
 %For count the switching times of IGBT.
 %phase A.
 if SAL_(i)~=SAL_(i-1)
   count_swa=count_swa+1;
   count_swa_(i)=count_swa;
 else
   count_swa=count_swa;
   count_swa_(i)=count_swa;
 end
 %phase B.
 if SBL_(i)~=SBL_(i-1)
   count_swb=count_swb+1;
   count_swb_(i)=count_swb;
 else
   count_swb=count_swb;
   count_swb_(i)=count_swb;
 end
 %phase C.
 if SCL_(i)~=SCL_(i-1)
   count_swc=count_swc+1;
   count_swc_(i)=count_swc;
 else
   count_swc=count_swc;
   count_swc_(i)=count_swc;
 end
 %Calculating Ica, Icb Icc and Vdc.
 %x=[Ica Icb Icc Vdc].
 [t,x]=ode23('apf',tspan,x0,options);
  x0=[x(max(length(x)),1) x(max(length(x)),2) x(max(length(x)),3) x(max(length(x)),4)]';
 %For keep the value of Ica Icb Icc and Vdc in new matrix name.
 %"I_ca I_cb I_cc and V_dc", for this loop.
 I_ca(i)=x0(1,1);
 I_cb(i)=x0(2,1);
 I_cc(i)=x0(3,1);
 V_dc(i)=x0(4,1);
 I_sa(i)=Ila(i)+I_ca(i);
 I_sb(i)=Ilb(i)+I_cb(i);
 I_sc(i)=Ilc(i)+I_cc(i);
 %Change value of Ica Icb Icc and Vdc for the next loop.
 Ica=x0(1,1);
 Icb=x0(2,1);
 Icc=x0(3,1);
 Vdc=x0(4,1);
 %Use the value of Vdca from average the value of Vcd from 10 values before.
```

```
%***** Low pass filter.*****
if i>=11
  Vdca=mean(V_dc(i-10:i-1));
  V_dca(i)=Vdca;                    %Keep value for matrix V_dca.
else
  Vdca=Vdc;
  V_dca(i)=Vdca;                    %Keep value for matrix V_dca in case of i<11.
end
%PI controller.
 %*************************************************************************
%Caculating Is_ref for the next loop.
V_err=Vdc_ref-V_dca(i);
Op(i)=Kp*V_err;
Oi(i)=Oi(i-1)+Ki*V_err*dt;
Opi(i)=Opi(1)+Op(i)+Oi(i);          %If no error Opi=Opi(1)
if time<0.01
  Opi(i)=Opi(1);                    %Protecting for transient response.
end
%Protecting for phase invert.
if Opi(i)<0.00001
  Opi(i)=0.00001;
end
Isa_ref=Opi(i)*Vsa/Vsa_max;
Isb_ref=Opi(i)*Vsb/Vsb_max;
Isc_ref=Opi(i)*Vsc/Vsc_max;
%Calculating Ic_ref for the next loop.
Ica_ref=Isa_ref-Ila(i);
Icb_ref=Isb_ref-Ilb(i);
Icc_ref=Isc_ref-Ilc(i);
%Keep value for this loop.
Isa_ref_(i)=Isa_ref;
Isb_ref_(i)=Isb_ref;
Isc_ref_(i)=Isc_ref;
Ica_ref_(i)=Ica_ref;
Icb_ref_(i)=Icb_ref;
Icc_ref_(i)=Icc_ref;
i=i+1;
end
%*************************************************************************
%*************************************************************************
%*************************End Main loop*********************************
%*************************************************************************
%*************************************************************************
%Current in neutral.
Inl=Ila+Ilb+Ilc;
I_nc=I_ca+I_cb+I_cc;
I_ns=I_sa+I_sb+I_sc;
%Figure 1, plot.....
%*************************************************************************
max_i=60;
y_axis=max_i+20*max_i/100;
```

```
figure(1)
clf
subplot(11,1,1),plot(t_simulation,I_sa(1:length(t_simulation)),'r',t_simulation,I_sb(1:length
(t_simulation)),'b',t_simulation,I_sc(1:length(t_simulation)),'m'),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Is (A) RBM')
grid
subplot(11,1,2),plot(t_simulation,I_ns(1:length(t_simulation))),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Ins (A)')
grid
subplot(11,1,3),plot(t_simulation,Ila(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ila (A)')
grid
subplot(11,1,4),plot(t_simulation,Ilb(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ilb (A)')
grid
subplot(11,1,5),plot(t_simulation,Ilc(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ilc (A)')
grid
subplot(11,1,6),plot(t_simulation,Inl(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Inl (A)')
grid
subplot(11,1,7),plot(t_simulation,I_ca(1:length(t_simulation))),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Ica (A)')
grid
subplot(11,1,8),plot(t_simulation,I_cb(1:length(t_simulation))),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Icb (A)')
grid
subplot(11,1,9),plot(t_simulation,I_cc(1:length(t_simulation))),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Icc (A)')
grid
subplot(11,1,10),plot(t_simulation,I_nc(1:length(t_simulation))),axis([0,t_stop,-
y_axis,y_axis])
ylabel('Inc (A)')
grid
subplot(11,1,11),plot(t_simulation,V_dc(1:length(t_simulation))),axis([0,t_stop,Vdc_ref-
10,Vdc_ref+10])
ylabel('Vdc (V)')
grid
xlabel('Time (second)')
shg
%Figure 2, plot Isa, Isb, Isc, Ins and switching times of each phase.
%*************************************************************************
figure(2)
clf
subplot(411),plot(t_simulation,I_sa(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Isa (A)')
```

```
text(0.001, min(I_sa)*2/3,sprintf('%0.5g %s',count_swa,'T'))
grid
subplot(412),plot(t_simulation,I_sb(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Isb (A)')
text(0.001, min(I_sa)*2/3,sprintf('%0.5g %s',count_swb,'T'))
grid
subplot(413),plot(t_simulation,I_sc(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Isc (A)')
text(0.001, min(I_sa)*2/3,sprintf('%0.5g %s',count_swc,'T'))
grid
subplot(414),plot(t_simulation,I_ns(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ins (A)')
grid
xlabel('Time (second)')
%Figure 3, plot Ila, Ilb, Ilc and Inl.
%*************************************************************************
figure(3)
clf
subplot(411),plot(t_simulation,Ila(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ila (A)')
grid
subplot(412),plot(t_simulation,Ilb(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ilb (A)')
grid
subplot(413),plot(t_simulation,Ilc(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Ilc (A)')
grid
subplot(414),plot(t_simulation,Inl(1:length(t_simulation))),axis([0,t_stop,-y_axis,y_axis])
ylabel('Inl (A)')
grid
xlabel('Time (second)')
%Figure 4, plot Vdc and Opi
%*************************************************************************
figure(4)
clf
subplot(411),plot(t_simulation,V_dc(1:length(t_simulation)),'r',t_simulation,V_dca(1:length
(t_simulation)),'b'),axis([0,t_stop,Vdc_ref-10,Vdc_ref+10])
ylabel('Vdc (V,red) Vdca (V,blue)')
grid
subplot(412),plot(t_simulation,Op(1:length(t_simulation)))
ylabel('Op (per sec)')
grid
subplot(413),plot(t_simulation,Oi(1:length(t_simulation)))
ylabel('Oi (per sec)')
grid
subplot(414),plot(t_simulation,Opi(1:length(t_simulation)))
ylabel('Opi (per sec)')
grid
xlabel('Time (second)')
shg
```

```
%Figure 5, plot error A,B and C.
%*************************************************************************
figure(5)
clf
subplot(411),plot(t_simulation,err_a_(1:length(t_simulation))),axis([0,t_stop,-
y_axis/2,y_axis/2])
ylabel('Error A')
grid
subplot(412),plot(t_simulation,err_b_(1:length(t_simulation))),axis([0,t_stop,-
y_axis/2,y_axis/2])
ylabel('Error B')
grid
subplot(413),plot(t_simulation,err_c_(1:length(t_simulation))),axis([0,t_stop,-
y_axis/2,y_axis/2])
ylabel('Error C')
grid
subplot(414),plot(t_simulation,Opi(1:length(t_simulation)))
ylabel('Opi (per sec)')
grid
xlabel('Time (second)')
shg
%Figure 6, calculate and plot THD and switching times of each phase.
%*************************************************************************
figure(6)
clf
%Start point and stop point for find FFT.
start=0.02/dt-mod(0.02/dt,1);
stop=(length(Ila)-1);
%Number of point to find FFT.
N=1024;
%For find FFT of non-linear load
Ya_l=fft(Ila(start:stop),N);
Yb_l=fft(Ilb(start:stop),N);
Yc_l=fft(Ilc(start:stop),N);
 A_l=abs(Ya_l);
 B_l=abs(Yb_l);
 C_l=abs(Yc_l);
 AA_l=A_l/(N/2);
 BB_l=B_l/(N/2);
 CC_l=C_l/(N/2);
%For find FFT of source
Ya_s=fft(I_sa(start:stop),N);
Yb_s=fft(I_sb(start:stop),N);
Yc_s=fft(I_sc(start:stop),N);
 A_s=abs(Ya_s);
 B_s=abs(Yb_s);
 C_s=abs(Yc_s);
 AA_s=A_s/(N/2);
 BB_s=B_s/(N/2);
 CC_s=C_s/(N/2);
 %Frequency
```

```
F=1/dt*(0:N/2-1)/N;
%Find THD
start=4;
step=7;
THD_A_l=sqrt((AA_l(start+step).^2+AA_l(start+2*step).^2+AA_l(start+3*step).^2+AA_l
(start+4*step).^2+AA_l(start+5*step).^2+AA_l(start+6*step).^2+AA_l(start+7*step).^2+AA
_l(start+8*step).^2+AA_l(start+9*step).^2+AA_l(start+10*step).^2+AA_l(start+11*step).^2
+AA_l(start+12*step).^2+AA_l(start+13*step).^2+AA_l(start+14*step).^2+AA_l
(start+15*step).^2+AA_l(start+16*step).^2+AA_l(start+17*step).^2)/(AA_l(start).^2))*100;
THD_B_l=sqrt((BB_l(start+step).^2+BB_l(start+2*step).^2+BB_l(start+3*step).^2+BB_l
(start+4*step).^2+BB_l(start+5*step).^2+BB_l(start+6*step).^2+BB_l(start+7*step).^2+BB
_l(start+8*step).^2+BB_l(start+9*step).^2+BB_l(start+10*step).^2+BB_l(start+11*step).^2+
BB_l(start+12*step).^2+BB_l(start+13*step).^2+BB_l(start+14*step).^2+BB_l
(start+15*step).^2+BB_l(start+16*step).^2+BB_l(start+17*step).^2)/(BB_l(start).^2))*100;
THD_C_l=sqrt((CC_l(start+step).^2+CC_l(start+2*step).^2+CC_l(start+3*step).^2+CC_l
(start+4*step).^2+CC_l(start+5*step).^2+CC_l(start+6*step).^2+CC_l(start+7*step).^2+CC
_l(start+8*step).^2+CC_l(start+9*step).^2+CC_l(start+10*step).^2+CC_l(start+11*step).^2+
CC_l(start+12*step).^2+CC_l(start+13*step).^2+CC_l(start+14*step).^2+CC_l
(start+15*step).^2+CC_l(start+16*step).^2+CC_l(start+17*step).^2)/(CC_l(start).^2))*100;
THD_A_s=sqrt((AA_s(start+step).^2+AA_s(start+2*step).^2+AA_s(start+3*step).^2+AA_s
(start+4*step).^2+AA_s(start+5*step).^2+AA_s(start+6*step).^2+AA_s(start+7*step).^2+A
A_s(start+8*step).^2+AA_s(start+9*step).^2+AA_s(start+10*step).^2+AA_s(start+11*step).
^2+AA_s(start+12*step).^2+AA_s(start+13*step).^2+AA_s(start+14*step).^2+AA_s
(start+15*step).^2+AA_s(start+16*step).^2+AA_s(start+17*step).^2)/(AA_s(start).^2))*100;
THD_B_s=sqrt((BB_s(start+step).^2+BB_s(start+2*step).^2+BB_s(start+3*step).^2+BB_s
(start+4*step).^2+BB_s(start+5*step).^2+BB_s(start+6*step).^2+BB_s(start+7*step).^2+BB
_s(start+8*step).^2+BB_s(start+9*step).^2+BB_s(start+10*step).^2+BB_s(start+11*step).^2
+BB_s(start+12*step).^2+BB_s(start+13*step).^2+BB_s(start+14*step).^2+BB_s
(start+15*step).^2+BB_s(start+16*step).^2+BB_s(start+17*step).^2)/(BB_s(start).^2))*100;
THD_C_s=sqrt((CC_s(start+step).^2+CC_s(start+2*step).^2+CC_s(start+3*step).^2+CC_s
(start+4*step).^2+CC_s(start+5*step).^2+CC_s(start+6*step).^2+CC_s(start+7*step).^2+CC
_s(start+8*step).^2+CC_s(start+9*step).^2+CC_s(start+10*step).^2+CC_s(start+11*step).^2
+CC_s(start+12*step).^2+CC_s(start+13*step).^2+CC_s(start+14*step).^2+CC_s
(start+15*step).^2+CC_s(start+16*step).^2+CC_s(start+17*step).^2)/(CC_s(start).^2))*100;
mag_I=[AA_l,BB_l,CC_l,AA_s,BB_s,CC_s];
max_mag_I=max(mag_I);
max_mag_I=max_mag_I+10;
max_freq_display=5000;
%For non-linear load
subplot(421),plot(F,AA_l(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Ila (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_A_l,'%'))
subplot(423),plot(F,BB_l(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Ilb (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_B_l,'%'))
subplot(425),plot(F,CC_l(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Ilc (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_C_l,'%'))
```

```
xlabel('Frequency (Hertz)')
%For source
subplot(422),plot(F,AA_s(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Isa (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_A_s,'%'))
subplot(424),plot(F,BB_s(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Isb (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_B_s,'%'))
subplot(426),plot(F,CC_s(1:N/2)),axis([0,max_freq_display,0,max_mag_I])
ylabel('Isc (A)')
text(max_freq_display-max_freq_display*2.2/3,2*max_mag_I/3,sprintf('THD is %0.5g
%s',THD_C_s,'%'))
xlabel('Frequency (Hertz)')
%For switching times
subplot(414),plot(t_simulation,count_swa_(1:length(t_simulation)),'r',t_simulation,count_sw
b_(1:length(t_simulation)),'b',t_simulation,count_swc_(1:length(t_simulation)),'m')
ylabel('Switching times,R,B,M')
xlabel('Time')
mag_sw=[count_swa,count_swb,count_swc];
max_sw_=max(mag_sw);
text(t_stop*1/3,max_sw_*8/10,sprintf('Switching of A is %0.5g %s',count_swa,'Times'))
text(t_stop*1/3,max_sw_*5/10,sprintf('Switching of B is %0.5g %s',count_swb,'Times'))
text(t_stop*1/3,max_sw_*2/10,sprintf('Switching of C is %0.5g %s',count_swc,'Times'))
shg
echo off
```

2. วิธีโครงข่ายประสาทเทียม

```
%*************************************************************************
%Use Neural Networks for current control.
%*************************************************************************
 %Use the value of Ic_ref and Ic from the previous loop.
  err_a=Ica_ref-Ica;
  err_b=Icb_ref-Icb;
  err_c=Icc_ref-Icc;
   k=1;                                  %Gain of error
  err_a=k*err_a;
  err_b=k*err_b;
  err_c=k*err_c;
  err_a_(i)=err_a;
  err_b_(i)=err_b;
  err_c_(i)=err_c;
  p=[err_a;err_b;err_c];                          %Input for NN.
  %Pattern 0 0 0
  if err_a==0 & err_b==0 & err_c==0
```

```
        p=[-1;-1;-1];                          %Input for NN.
end
%Simulate feed forward of NN, by use the weight and bias that caculated before this calculating.
answer=simuff(p,w1,b1,'tansig',w2,b2,'tansig');
a=answer(1);
b=answer(2);
c=answer(3);
answer_(1,i)=a;
answer_(2,i)=b;
answer_(3,i)=c;
%Switching function of APF
%phase A .
%if output of NN < 0 then Charge.
%if output of NN >= 0 then Discharge.
if a<0
  SAL=1;
  SAR=0;
  SAL_(i)=SAL;
  SAR_(i)=SAR;
else
  SAL=0;
  SAR=1;
  SAL_(i)=SAL;
  SAR_(i)=SAR;
end
%phase B.
if b<0
  SBL=1;
  SBR=0;
  SBL_(i)=SBL;
  SBR_(i)=SBR;
else
  SBL=0;
  SBR=1;
  SBL_(i)=SBL;
  SBR_(i)=SBR;
end
%phase C.
if c<0
  SCL=1;
  SCR=0;
  SCL_(i)=SCL;
  SCR_(i)=SCR;
```

```
 else
   SCL=0;
   SCR=1;
   SCL_(i)=SCL;
   SCR_(i)=SCR;
 End
%*****************************************************************
%End of Using Neural Networks for current control.
%*****************************************************************
```

3. โปรแกรมย่อยอื่นๆ

apf.m

```
%3-single phase current of APF and Vdc
function xdot = apf(t,x)
global Rc Lc Cdc;
global Vsa Vsb Vsc;
global SAL SAR SBL SBR SCL SCR;
xdot=[(-Rc*x(1)+Vsa-x(4)*(SAL-SAR))/Lc,(-Rc*x(2)+Vsb-x(4)*(SBL-SBR))/Lc,(-Rc*x(3)+Vsc-x
(4)*(SCL-SCR))/Lc,(x(1)*(SAL-SAR)+x(2)*(SBL-SBR)+x(3)*(SCL-SCR))/Cdc]';
```

conda.m, condb.m และ conc.m

```
%For diode conducting of phase A
function xadot = conda(t,xa)
global Rsa Rla Lsa Cla Vsa;
xadot = [(Vsa-Rsa*xa(1)-xa(2))/Lsa,(xa(1)-xa(2)/Rla)/Cla]';

%For diode conducting of phase B
function xbdot = condb(t,xb)
global Rsb Rlb Lsb Clb Vsb;
xbdot = [(Vsb-Rsb*xb(1)-xb(2))/Lsb,(xb(1)-xb(2)/Rlb)/Clb]';

%For diode conducting of phase C
function xcdot = condc(t,xc)
global Rsc Rlc Lsc Clc Vsc;
xcdot = [(Vsc-Rsc*xc(1)-xc(2))/Lsc,(xc(1)-xc(2)/Rlc)/Clc]';
```

notconda.m, notcondb.m และ notcondc.m

```
%For diode not conducting of phase A
function zadot=notconda(t,za)
global Rla Cla;
zadot=(-za)/(Rla*Cla);

%For diode not conducting of phase B
```

```
function zbdot=notcondb(t,zb)
global Rlb Clb;
zbdot=(-zb)/(Rlb*Clb);

%For diode not conducting of phase C
function zcdot=notcondc(t,zc)
global Rlc Clc;
zcdot=(-zc)/(Rlc*Clc);
```

ภาคผนวก ค

โปรแกรมภาษาซีเพื่อทำหน้าที่เป็นโครงข่ายประสาทเทียม

```
#include<stdio.h>
#include<conio.h>
#include<dos.h>
#define OUTPORT 0x318

int PORT[4]={0,0x300,0x308,0x310};
int input_in1,input_in2,input_in3;
int input1,input2,input3;
int h_in1,h_in2,h_in3,h_in4,h_in5;
int h1,h2,h3,h4,h5;
int o_in1,o_in2,o_in3;
int o1,o2,o3;
int output;
void main()
{
    int i;
    while(1)
    {
                    input_in1=inportb(PORT[1]);
                    input_in2=inportb(PORT[2]);
                    input_in3=inportb(PORT[3]);

                    input1=(int)(input_in1-128)/51;
                    input2=(int)(input_in2-128)/51;
                    input3=(int)(input_in3-128)/51;

                    h_in1 =  input1*102+input2*22 +input3*117-7 ;
                    h_in2 = -input1*181-input2*22 +input3*44 +48;
                    h_in3 =  input1*33 -input2*194+input3*47 +8 ;
                    h_in4 = -input1*35 +input2*71 +input3*152-2 ;
                    h_in5 =  input1*111+input2*34 -input3*96 +40;

                    if(h_in1>=0)
                     {
                     h1=1;
                     }
                    else
                     {
                     h1=-1;
```

```
 }
if(h_in2>=0)
 {
 h2=1;
 }
 else
 {
 h2=-1;
 }
if(h_in3>=0)
 {
 h3=1;
 }
 else
 {
 h3=-1;
 }
if(h_in4>=0)
 {
 h4=1;
 }
 else
 {
 h4=-1;
 }
if(h_in5>=0)
 {
 h5=1;
 }
 else
 {
 h5=-1;
 }

 o_in1 =  h1*158-h2*251+h3*48 -h4*19 +h5*131+2 ;
 o_in2 = -h1*24 -h2*25 -h3*365+h4*67 +h5*30   ;
 o_in3 =  h1*205+h2*17 +h3*64 +h4*258-h5*90 +23;

 if(o_in1>=0)
  {
  o1=1;
  }
  else
  {
  o1=0;
  }
 if(o_in2>=0)
  {
  o2=1;
  }
  else
```

```
  {
  o2=0;
  }
 if(o_in3>=0)
  {
  o3=1;
  }
  else
  {
  o3=0;
  }

output=o1+o2*2+o3*4;
outportb(OUTPORT,output);
```

ภาคผนวก ง

ตัวเชื่อมต่อผ่านแสง เบอร์ 6N137

High CMR, High Speed TTL Compatible Optocouplers

Technical Data

6N137
HCNW137 **HCPL-0631**
HCNW2601 **HCPL-0661**
HCNW2611 **HCPL-2601**
HCPL-0600 **HCPL-2611**
HCPL-0601 **HCPL-2630**
HCPL-0611 **HCPL-2631**
HCPL-0630 **HCPL-4661**

Features

- **5 kV/μs Minimum Common Mode Rejection (CMR) at V_{CM} = 50 V for HCPL-X601/X631, HCNW2601 and 10 kV/μs Minimum CMR at V_{CM} = 1000 V for HCPL-X611/X661, HCNW2611**
- **High Speed:** 10 MBd Typical
- **LSTTL/TTL Compatible**
- **Low Input Current Capability: 5 mA**
- **Guaranteed ac and dc Performance over Temperature:** -40°C to +85°C
- **Available in 8-Pin DIP, SOIC-8, Widebody Packages**
- **Strobable Output (Single Channel Products Only)**
- **Safety Approval**
  UL Recognized - 2500 V rms for 1 minute and 5000 V rms* for 1 minute per UL1577
  CSA Approved
  VDE 0884 Approved with V_{IORM} = 630 V peak for HCPL-2611 Option 060 and V_{IORM} = 1414 V peak for HCNW137/26X1
  BSI Certified (HCNW137/26X1 Only)
- **MIL-STD-1772 Version Available (HCPL-56XX/66XX)**

Applications

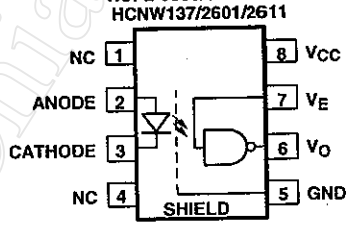
- **Isolated Line Receiver**
- **Computer-Peripheral Interfaces**
- **Microprocessor System Interfaces**
- **Digital Isolation for A/D, D/A Conversion**
- **Switching Power Supply**
- **Instrument Input/Output Isolation**
- **Ground Loop Elimination**
- **Pulse Transformer Replacement**
- **Power Transistor Isolation in Motor Drives**
- **Isolation of High Speed Logic Systems**

Description

The 6N137, HCPL-26XX/06XX/4661, HCNW137/26X1 are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. An enable input allows the detector to be strobed. The output of the detector IC is

Functional Diagram

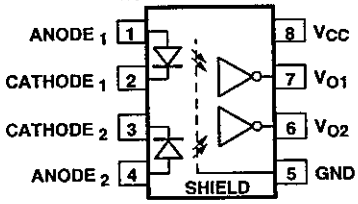
6N137, HCPL-2601/2611
HCPL-0600/0601/0611
HCNW137/2601/2611



TRUTH TABLE
(POSITIVE LOGIC)

LED	ENABLE	OUTPUT
ON	H	L
OFF	H	H
ON	L	H
OFF	L	H
ON	NC	L
OFF	NC	H

HCPL-2630/2631/4661
HCPL-0630/0631/0661



TRUTH TABLE
(POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

*5000 V rms/1 Minute rating is for HCNW137/26X1 and Option 020 (6N137, HCPL-2601/11/30/31, HCPL-4661) products only.

A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 5,000 V/µs for the HCPL-X601/X631 and HCNW2601, and 10,000 V/µs for the HCPL-X611/X661 and HCNW2611.

This unique design provides maximum ac and dc circuit isolation while achieving TTL compatibility. The optocoupler ac and dc operational parameters are guaranteed from -40°C to +85°C allowing troublefree system performance.

The 6N137, HCPL-26XX, HCPL-06XX, HCPL-4661, HCNW137, and HCNW26X1 are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Selection Guide

Minimum CMR		Input On-Current (mA)	Output Enable	8-Pin DIP (300 Mil)		Small-Outline SO-8		Widebody (400 Mil)	Hermetic
dV/dt (V/µs)	V_{CM} (V)			Single Channel Package	Dual Channel Package	Single Channel Package	Dual Channel Package	Single Channel Package	Single and Dual Channel Packages
NA	NA	5	YES	6N137		HCPL-0600		HCNW137	
			NO		HCPL-2630		HCPL-0630		
5,000	50		YES	HCPL-2601		HCPL-0601		HCNW2601	
			NO		HCPL-2631		HCPL-0631		
10,000	1,000		YES	HCPL-2611		HCPL-0611		HCNW2611	
			NO		HCPL-4661		HCPL-0661		
1,000	50		YES	HCPL-2602[1]					
3,500	300		YES	HCPL-2612[1]					
1,000	50	3	YES	HCPL-261A[1]		HCPL-061A[1]			
			NO		HCPL-263A[1]		HCPL-063A[1]		
1,000[2]	1,000		YES	HCPL-261N[1]		HCPL-061N[1]			
			NO		HCPL-263N[1]		HCPL-063N[1]		
1,000	50	12.5	[3]						HCPL-193X[1] HCPL-56XX[1] HCPL-66XX[1]

Notes:
1. Technical data are on separate HP publications.
2. 15 kV/µs with V_{CM} = 1 kV can be achieved using HP application circuit.
3. Enable is available for single channel products only, except for HCPL-193X devices.

Ordering Information

Specify Part Number followed by Option Number (if desired).

Example:

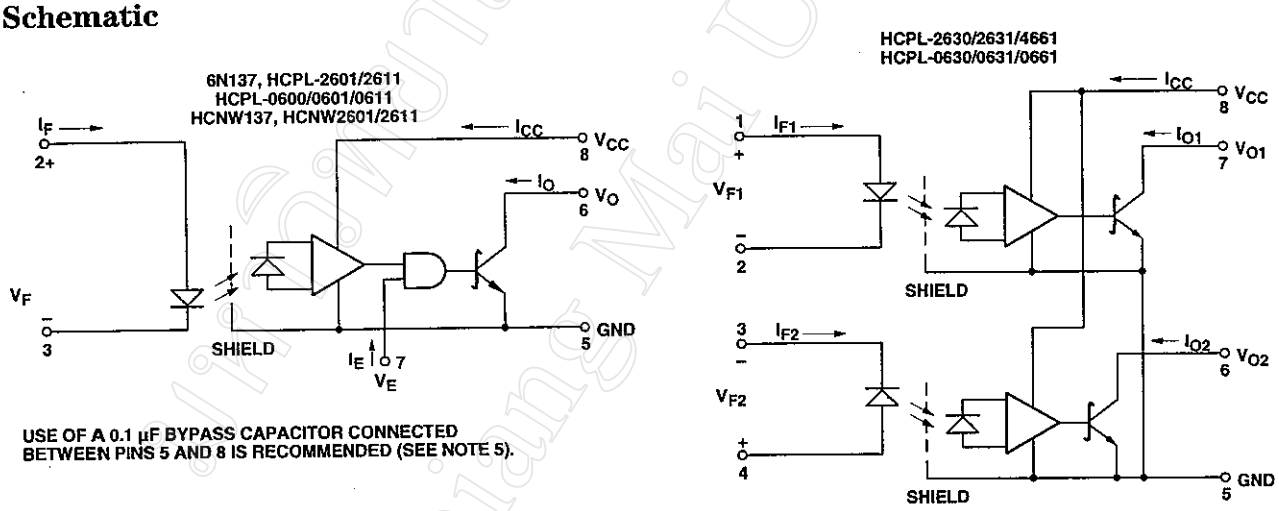
HCPL-2611#XXX

- 020 = 5000 V rms/1 minute UL Rating Option*
- 060 = VDE 0884 V_{IORM} = 630 Vpeak Option**
- 300 = Gull Wing Surface Mount Option†
- 500 = Tape and Reel Packaging Option

Option data sheets available. Contact Hewlett-Packard sales representative or authorized distributor for information.

*For 6N137, HCPL-2601/11/30/31 and HCPL-4661 (8-pin DIP products) only.
**For HCPL-2611 only. Combination of Option 020 and Option 060 is not available.
†Gull wing surface mount option applies to through hole parts only.

Schematic



Regulatory Information

The 6N137, HCPL-26XX/06XX/46XX, and HCNW137/26XX have been approved by the following organizations:

UL

Recognized under UL 1577, Component Recognition Program, File E55361.

CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

VDE

Approved according to VDE 0884/06.92. (HCPL-261 1 Option 060 and HCNW137/26X1 only)

BSI

Certification according to BS415:1994 (BS EN60065:1994), BS7002:1992 (BS EN60950:1992) and EN41003:1993 for Class II applications. (HCNW137/26X1 only)

Insulation and Safety Related Specifications

Parameter	Symbol	8-pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	200	200	200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings* (No Derating Required up to 85°C)

Parameter	Symbol	Package**	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature†	T_A		-40	85	°C	
Average Forward Input Current	I_F	Single 8-Pin DIP Single SO-8 Widebody		20	mA	2
		Dual 8-Pin DIP Dual SO-8		15		1, 3
Reverse Input Voltage	V_R	8-Pin DIP, SO-8		5	V	1
		Widebody		3		
Input Power Dissipation	P_I	Widebody		40	mW	
Supply Voltage (1 Minute Maximum)	V_{CC}			7	V	
Enable Input Voltage (Not to Exceed V_{CC} by more than 500 mV)	V_E	Single 8-Pin DIP Single SO-8 Widebody		V_{CC} + 0.5	V	
Enable Input Current	I_E			5	mA	
Output Collector Current	I_O			50	mA	1
Output Collector Voltage (Selection for Higher Output Voltages up to 20 V is Available.)	V_O			7	V	1
Output Collector Power Dissipation	P_O	Single 8-Pin DIP Single SO-8 Widebody		85	mW	
		Dual 8-Pin DIP Dual SO-8		60		1, 4
Lead Solder Temperature (Through Hole Parts Only)	T_{LS}	8-Pin DIP	260°C for 10 sec., 1.6 mm below seating plane			
		Widebody	260°C for 10 sec., up to seating plane			
Solder Reflow Temperature Profile (Surface Mount Parts Only)		SO-8 and Option 300	See Package Outline Drawings section			

*JEDEC Registered Data (for 6N137 only).
Ratings apply to all devices except otherwise noted in the **Package column.
†0°C to 70°C on JEDEC Registration.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	4.5	5.5	V
Low Level Enable Voltage†	V_{EL}	0	0.8	V
High Level Enable Voltage†	V_{EH}	2.0	V_{CC}	V
Operating Temperature	T_A	-40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.
†For single channel products only.

Electrical Specifications

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. All Typicals at V_{CC} = 5 V, T_A = 25°C. All enable test conditions apply to single channel products only. See note 5.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*	All		5.5	100	µA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 5.5 V, I_F = 250 µA	1	1, 6, 19
Input Threshold Current	I_{TH}	Single Channel Widebody		2.0	5.0	mA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2, 3	19
		Dual Channel		2.5					
Low Level Output Voltage	V_{OL}*	8-Pin DIP SO-8		0.35	0.6	V	V_{CC} = 5.5 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2, 3, 4, 5	1, 19
		Widebody		0.4					
High Level Supply Current	I_{CCH}	Single Channel		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V; I_F = 0 mA		7
				6.5			V_E = V_{CC}		
		Dual Channel		10	15		Both Channels		
Low Level Supply Current	I_{CCL}	Single Channel		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V; I_F = 10 mA		8
				8.5			V_E = V_{CC}		
		Dual Channel		13	21		Both Channels		
High Level Enable Current	I_{EH}	Single Channel		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*			-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		9
High Level Enable Voltage	V_{EH}		2.0			V			19
Low Level Enable Voltage	V_{EL}				0.8	V			
Input Forward Voltage	V_F	8-Pin DIP SO-8	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	6, 7	1
			1.3		1.80				
		Widebody	1.25	1.64	1.85		T_A = 25°C		
			1.2		2.05				
Input Reverse Breakdown Voltage	BV_R*	8-Pin DIP SO-8	5			V	I_R = 10 µA		1
		Widebody	3				I_R = 100 µA, T_A = 25°C		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	8-Pin DIP SO-8		-1.6		mV/°C	I_F = 10 mA	7	1
		Widebody		-1.9					
Input Capacitance	C_{IN}	8-Pin DIP SO-8		60		pF	f = 1 MHz, V_F = 0 V		1
		Widebody		70					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.

Electrical Specifications

Over recommended temperature (T_A = -40°C to +85°C) unless otherwise specified. All Typicals at V_{CC} = 5 V, T_A = 25°C. All enable test conditions apply to single channel products only. See note 5.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*	All		5.5	100	µA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 5.5 V, I_F = 250 µA	1	1, 6, 19
Input Threshold Current	I_{TH}	Single Channel Widebody		2.0	5.0	mA	V_{CC} = 5.5 V, V_E = 2.0 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2, 3	19
		Dual Channel		2.5					
Low Level Output Voltage	V_{OL}*	8-Pin DIP SO-8		0.35	0.6	V	V_{CC} = 5.5 V, V_E = 2.0 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	2, 3, 4, 5	1, 19
		Widebody		0.4					
High Level Supply Current	I_{CCH}	Single Channel		7.0	10.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 0 mA		7
				6.5			V_E = V_{CC}		
		Dual Channel		10	15		Both Channels		
Low Level Supply Current	I_{CCL}	Single Channel		9.0	13.0*	mA	V_E = 0.5 V; V_{CC} = 5.5 V, I_F = 10 mA		8
				8.5			V_E = V_{CC}		
		Dual Channel		13	21		Both Channels		
High Level Enable Current	I_{EH}	Single Channel		-0.7	-1.6	mA	V_{CC} = 5.5 V, V_E = 2.0 V		
Low Level Enable Current	I_{EL}*			-0.9	-1.6	mA	V_{CC} = 5.5 V, V_E = 0.5 V		9
High Level Enable Voltage	V_{EH}		2.0			V			19
Low Level Enable Voltage	V_{EL}				0.8	V			
Input Forward Voltage	V_F	8-Pin DIP	1.4	1.5	1.75*	V	T_A = 25°C; I_F = 10 mA	6, 7	1
		SO-8	1.3		1.80				
		Widebody	1.25	1.64	1.85		T_A = 25°C		
			1.2		2.05				
Input Reverse Breakdown Voltage	BV_R*	8-Pin DIP SO-8	5			V	I_R = 10 µA		1
		Widebody	3				I_R = 100 µA, T_A = 25°C		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$	8-Pin DIP SO-8		-1.6		mV/°C	I_F = 10 mA	7	1
		Widebody		-1.9					
Input Capacitance	C_{IN}	8-Pin DIP SO-8		60		pF	f = 1 MHz, V_F = 0 V		1
		Widebody		70					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to +70°C. HP specifies -40°C to +85°C.

Switching Specifications (AC)

Over Recommended Temperature (T_A = -40°C to +85°C), V_{CC} = 5 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 5 V.

Parameter	Sym.	Package**	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}		20	48	75* 100	ns	T_A = 25°C, R_L = 350 Ω, C_L = 15 pF	8, 9, 10	1, 10, 19
Propagation Delay Time to Low Output Level	t_{PHL}		25	50	75* 100	ns	T_A = 25°C		1, 11, 19
Pulse Width Distortion	$\|t_{PHL} - t_{PLH}\|$	8-Pin DIP SO-8 Widebody		3.5	35 40	ns		8, 9, 10, 11	13, 19
Propagation Delay Skew	t_{PSK}				40	ns			12, 13, 19
Output Rise Time (10-90%)	t_r			24		ns		12	1, 19
Output Fall Time (90-10%)	t_f			10		ns		12	1, 19
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	Single Channel		30		ns	R_L = 350 Ω, C_L = 15 pF, V_{EL} = 0 V, V_{EH} = 3 V	13, 14	14
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}	Single Channel		20		ns			15

*JEDEC registered data for the 6N137.
Ratings apply to all devices except otherwise noted in the **Package column.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	15	1, 16, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	6N137 HCPL-2630 HCPL-0600/0630 HCNW137		10,000	V/µs	$\|V_{CM}\|$ = 10 V	V_{CC} = 5 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	15	1, 17, 18, 19
		HCPL-2601/2631 HCPL-0601/0631 HCNW2601	5,000	10,000		$\|V_{CM}\|$ = 50 V			
		HCPL-2611/4661 HCPL-0611/0661 HCNW2611	10,000	15,000		$\|V_{CM}\|$ = 1 kV			

Package Characteristics

All Typicals at T_A = 25°C.

Parameter	Sym.	Package	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Input-Output Insulation	I_{I-O}*	Single 8-Pin DIP Single SO-8			1	μA	45% RH, t = 5 s, V_{I-O} = 3 kV dc, T_A = 25°C		20, 21
Input-Output Momentary Withstand Voltage**	V_{ISO}	8-Pin DIP, SO-8	2500			V rms	RH ≤ 50%, t = 1 min, T_A = 25°C		20, 21
		Widebody	5000						20, 22
		OPT 020†	5000						
Input-Output Resistance	R_{I-O}	8-Pin DIP, SO-8		10^{12}		Ω	V_{I-O} = 500 V dc		1, 20, 23
		Widebody	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Input-Output Capacitance	C_{I-O}	8-Pin DIP, SO-8		0.6		pF	f = 1 MHz, T_A = 25°C		1, 20, 23
		Widebody		0.5	0.6				
Input-Input Insulation Leakage Current	I_{I-I}	Dual Channel		0.005		μA	RH ≤ 45%, t = 5 s, V_{I-I} = 500 V		24
Resistance (Input-Input)	R_{I-I}	Dual Channel		10^{11}		Ω			24
Capacitance (Input-Input)	C_{I-I}	Dual 8-Pin DIP		0.03		pF	f = 1 MHz		24
		Dual SO-8		0.25					

*JEDEC registered data for the 6N137. The JEDEC Registration specifies 0°C to 70°C. HP specifies -40°C to 85°C.
**The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification or HP Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
†For 6N137, HCPL-2601/2611/2630/2631/4661 only.

Notes:

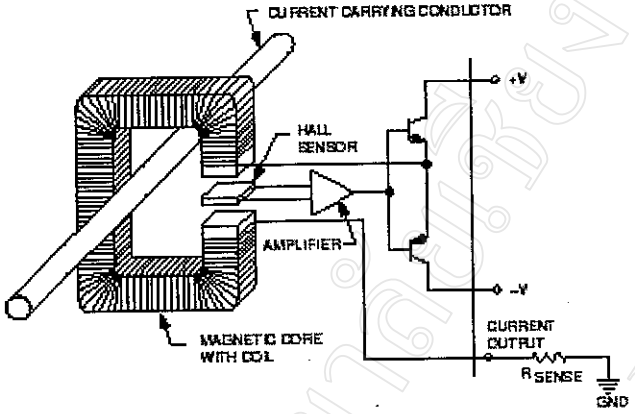
1. Each channel.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
3. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
4. Derate linearly above 80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
5. Bypassing of the power supply line is required, with a 0.1 μF ceramic disc capacitor adjacent to each optocoupler as illustrated in Figure 17. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
6. The JEDEC registration for the 6N137 specifies a maximum I_{OH} of 250 μA. HP guarantees a maximum I_{OH} of 100 μA.
7. The JEDEC registration for the 6N137 specifies a maximum I_{CCH} of 15 mA. HP guarantees a maximum I_{CCH} of 10 mA.
8. The JEDEC registration for the 6N137 specifies a maximum I_{CCL} of 18 mA. HP guarantees a maximum I_{CCL} of 13 mA.
9. The JEDEC registration for the 6N137 specifies a maximum I_{EL} of –2.0 mA. HP guarantees a maximum I_{EL} of -1.6 mA.
10. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
11. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
12. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
13. See application section titled "Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew" for more information.
14. The t_{ELH} enable propagation delay is measured from the 1.5 V point on the falling edge of the enable input pulse to the 1.5 V point on the rising edge of the output pulse.
15. The t_{EHL} enable propagation delay is measured from the 1.5 V point on the rising edge of the enable input pulse to the 1.5 V point on the falling edge of the output pulse.
16. CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state (i.e., V_O > 2.0 V).
17. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_O < 0.8 V).
18. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM(p\text{-}p)}$.

ภาคผนวก จ

ตัวตรวจจับกระแสเบอร์ CLN-25

Closed Loop Current Sensors

A closed loop current sensor consists of a Hall sensor mounted in an air gap of a magnetic core, a coil wound around the core and a current amplifier. The current carrying conductor placed through the aperture of the sensor produces a magnetic field that is proportionate to the current. This field is concentrated by the core and sensed by the Hall sensor. The Hall sensor is connected to the input of the current amplifier, which drives the coil. The current through the coil produces an opposing field to that provided by the current through the aperture, thus the flux in the core is constantly driven to zero. The coil connects to the output of the sensor. Therefore the output is a current proportional to the aperture current, multiplied by the number of turns on the coil. A sensor with a 1000 turn coil provides an output of 1mA per ampere. The current output is converted to a voltage by connecting a resistor between the output of the sensor and ground. The output is scaled by selecting the resistor value. Closed loop sensors measure DC and AC currents and provide electrical isolation. They offer fast response, high linearity and low temperature drift. The current output of the closed loop sensor is relatively immune to electrical noise. They are the sensor of choice when high accuracy is essential.



• Fast Response • Excellent linearity • Wide bandwidth • Low temperature drift

Model	Nominal Current (IN)	Linearity (%)	Frequency	Output (mA at IN)	Aperture Inches (mm)	Page(s)
CLS-25	25	0.5	dc to 150 kHz	50	PCB Connection	30-31
CLN-25	25	0.2	dc to 150 kHz	25	PCB Connection	32-33
CLN-50	50	0.1	dc to 150 kHz	50	0.63 x 0.39	34-35
CLN-50SP1	50	0.1	dc to 150 kHz	50	PCB Connection	36-37
CLN-100	100	0.1	dc to 150 kHz	100	0.63 x 0.39	34-35
CLN-100SP1	25	0.2	dc to 150 kHz	100	PCB Connection	36-37
CLN-200	200	0.1	dc to 150 kHz	100	0.63 x 0.39	38-39
CLN-300	300	0.1	dc to 150 kHz	150	0.9	38-39
CLN-300SP1	50	0.1	dc to 150 kHz	150	Bussbar	40-41
CLN-500	500	0.1	dc to 150 kHz	100	1.02	42-43
CLN-500SP1	100	0.1	dc to 150 kHz	100	Bussbar	40-41
CLN-1000	1000	0.1	dc to 150 kHz	100	1.02	42-43
CLO-300	300	0.1	dc to 150 kHz	150	0.905	44-45
CLO-500	500	0.1	dc to 100 kHz	100	1.025	44-45

Note: Due to continuous process improvement, all specifications listed in this catalog subject to change without notice.

Model CLN-25

Description

The Model CLN-25 is a closed loop Hall effect current sensor that accurately measures dc and ac currents and provides electrical isolation between the current carrying conductor and the output of the sensor.

Electrical Specifications

Nominal current (I_N)	25 Ampere turns rms	
Measuring range *	0 to 36 Ampere turns (A.t.)	
Sense resistor	**R. min.**	**R. max.**
with ± 12 V at 25 A.t. peak	100 ohms	200 ohms
at 36 A.t. peak	100 ohms	140 ohms
with ± 15 V at 25 A.t. peak	100 ohms	320 ohms
at 36 A.t. peak	100 ohms	190 ohms
Nominal analog output current	25 mA	
Turns ratio	1-2-3-4-5:1000	
Overall accuracy at 25 °C and ±12 V	± 0.7% of I_N	
Overall accuracy at 25 °C and ± 15 V	± 0.5% of I_N	
Supply voltage (Vdc)	± 12 to ± 15 (± 5%)	
Dielectric strength	between the current carrying conductor and the output of the sensor: 5 kV rms/50 Hz/1 min.	

Accuracy-Dynamic Performance

	Typical	**Max.**
Zero current offset at 25 °C (± 15V)	± 0.05 mA	± 0.15 mA
Residual current offset after an overload of 3 x I_N	± 0.05 mA	± 0.15 mA
Offset current temperature drift (± 15V)		
(between 0 °C and +25 °C)	± 0.06 mA	± 0.25 mA
(between +25 °C and +70 °C)	± 0.1 mA	± 0.35 mA
Linearity	better than ±0.2%	
Response time	less than 1 µs	
di/dt accurately followed	better than 50 A/µs	
Bandwidth	0 to 150 kHz (- 1 dB)	

General Information

Operating temperature	-40 °C to +85 °C
Storage temperature	-40 °C to +90 °C
Current drain	10 mA (at ± 15 V) plus output current
Coil resistance	110 ohms (at 70 °C)
Package	Flame retarded plastic case
Weight	16 grams
Mounting	Designed to mount directly on PCB via through hole connection pins
Output reference	To obtain a positive output on the terminal marked "O/P", current must flow from terminals 1,2,3,4 and 5 to terminals 10,9,8,7 and 6 (conventional flow)

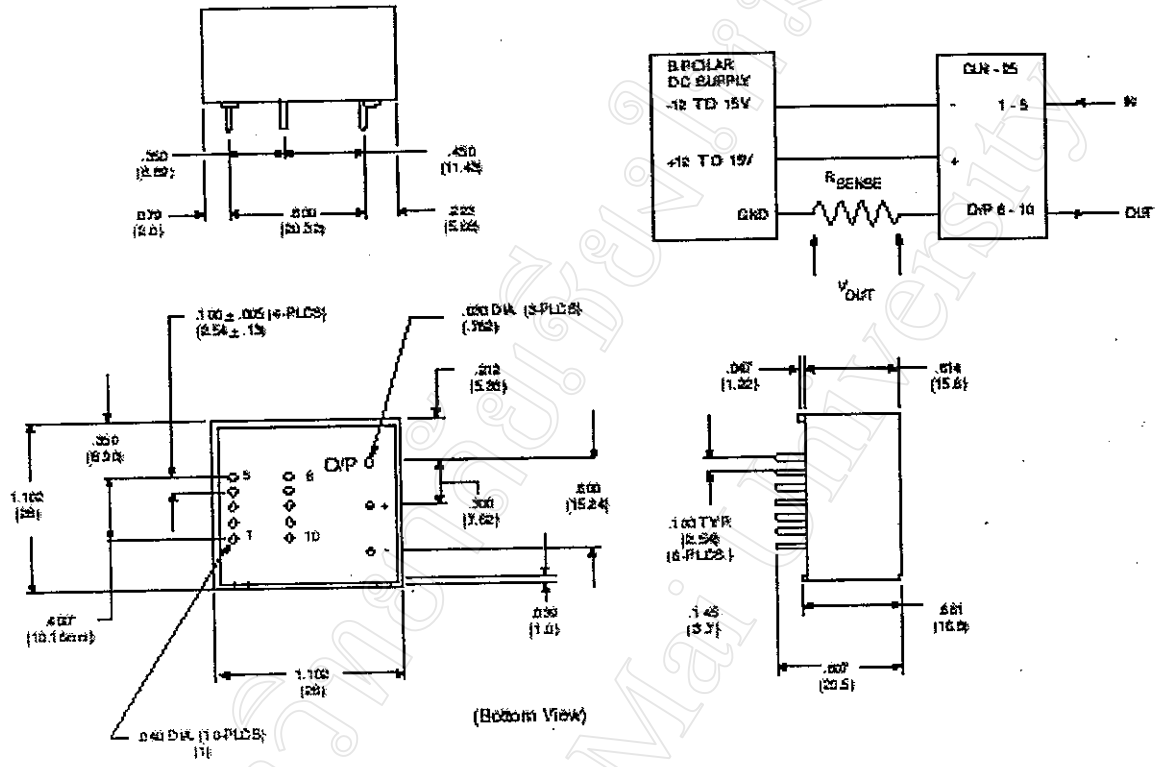
Notes

1. The CLN-25 offers a choice of 5 measuring ranges (see table)
2. Due to continuous process improvement, all specifications listed in this catalog subject to change without notice.

Model CLN-25

Mechanical Dimensions

All dimensions are in inches (millimeters)



Measuring Range Table

Number of Turns of I_M	I_M(A)	Peak (A)	Normal output Current (mA)	Turn Ratio	Insertion Loss Resistance (mΩ)	Insertion Loss Inductance (uH)	Recommended Connections
1	25	38	25	1/1000	0.5	0.023	IN / OUT
2	12	18	24	2/1000	1.1	0.09	IN / OUT
3	8	12	24	3/1000	2.5	0.21	IN / OUT
4	6	9	24	4/1000	4.4	0.37	IN / OUT
5	5	7	25	5/1000	6.3	0.58	IN / OUT

Note: Due to continuous process improvement, all specifications listed in this catalog subject to change without notice.

ภาคผนวก ฉ

วงจรขยายสำหรับแยกโคด เบอร์ HCPL-7800

High CMR Isolation Amplifiers

Technical Data

HCPL-7800
HCPL-7800A
HCPL-7800B

Features

- **15 kV/μs Common-Mode Rejection at V_{CM} = 1000 V***
- **Compact, Auto-Insertable Standard 8-pin DIP Package**
- **4.6 μV/°C Offset Drift vs. Temperature**
- **0.9 mV Input Offset Voltage**
- **85 kHz Bandwidth**
- **0.1% Nonlinearity**
- **Worldwide Safety Approval: UL 1577 (3750 V rms/1 min), VDE 0884 and CSA**
- **Advanced Sigma-Delta (ΣΔ) A/D Converter Technology**
- **Fully Differential Circuit Topology**
- **1 μm CMOS IC Technology**

Applications

- **Motor Phase Current Sensing**
- **General Purpose Current Sensing**
- **High-Voltage Power Source Voltage Monitoring**
- **Switch-Mode Power Supply Signal Isolation**
- **General Purpose Analog Signal Isolation**
- **Transducer Isolation**

*The terms common-mode rejection (CMR) and isolation-mode rejection (IMR) are used interchangeably throughout this data sheet.

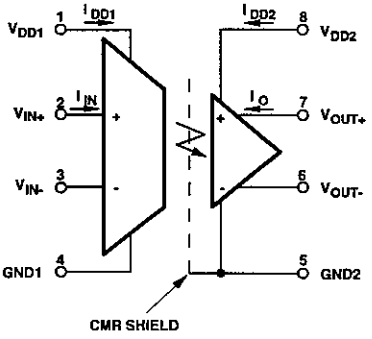
Description

The HCPL-7800 high CMR isolation amplifier provides a unique combination of features ideally suited for motor control circuit designers. The product provides the precision and stability needed to accurately monitor motor current in high-noise motor control environments, providing for smoother control (less "torque ripple") in various types of motor control applications.

This product paves the way for a smaller, lighter, easier to produce, high noise rejection, low cost solution to motor current sensing. The product can also be used for general analog signal isolation applications requiring high accuracy, stability and linearity under similarly severe noise conditions. For general applications, we recommend the HCPL-7800 which exhibits a part-to-part gain tolerance of ± 5%. For precision applications, HP offers the HCPL-7800A and HCPL-7800B, each with part-to-part gain tolerances of ± 1%.

The HCPL-7800 utilizes sigma-delta (ΣΔ) analog-to-digital converter technology, chopper stabilized amplifiers, and a fully differential circuit topology fabricated using HP's 1 μm CMOS IC process. The part also couples our high-efficiency, high-speed AlGaAs LED to a high-speed, noise-shielded detector

Functional Diagram



CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

using our patented "light-pipe" optocoupler packaging technology.

Together, these features deliver unequaled isolation-mode noise rejection, as well as excellent offset and gain accuracy and stability over time and temperature. This performance is delivered in a compact, auto-insertable, industry standard 8-pin DIP package that meets worldwide regulatory safety standards (gull-wing surface mount option #300 also available).

Ordering Information:

HCPL-7800x

- No Specifier = ± 5% Gain Tol.; Mean Gain Value = 8.00
- A = ± 1% Gain Tol.; Mean Gain Value = 7.93
- B = ± 1% Gain Tol.; Mean Gain Value = 8.07

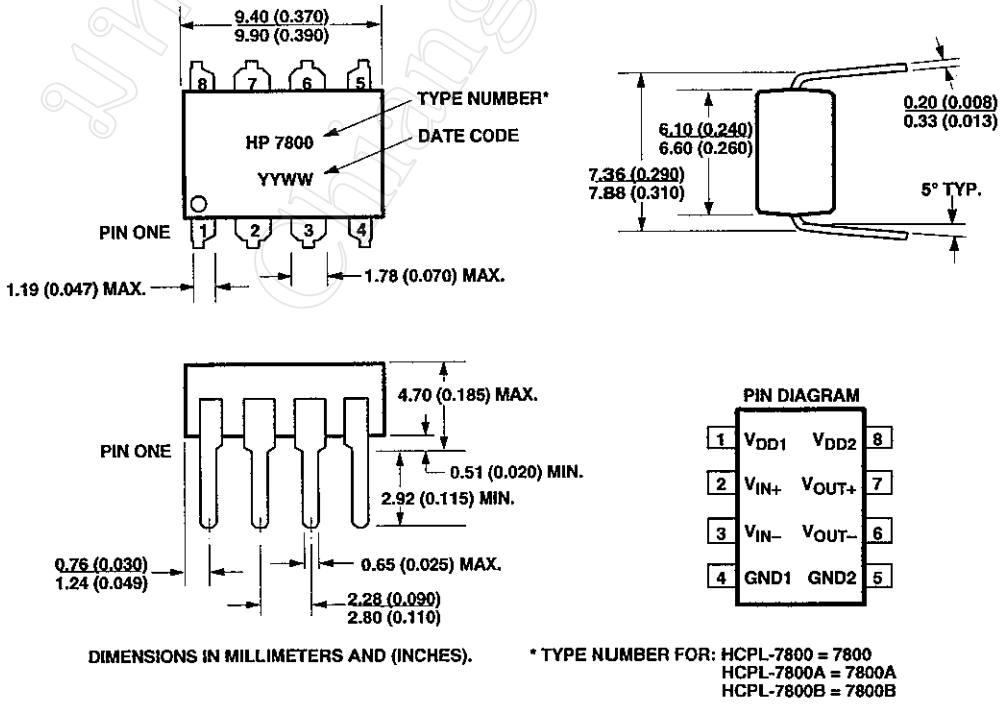
Option yyy

- 300 = Gull Wing Surface Mount Lead Option
- 500 = Tape/Reel Package Option (1 k min.)

Option datasheets available. Contact your Hewlett-Packard sales representative or authorized distributor for information.

Package Outline Drawings

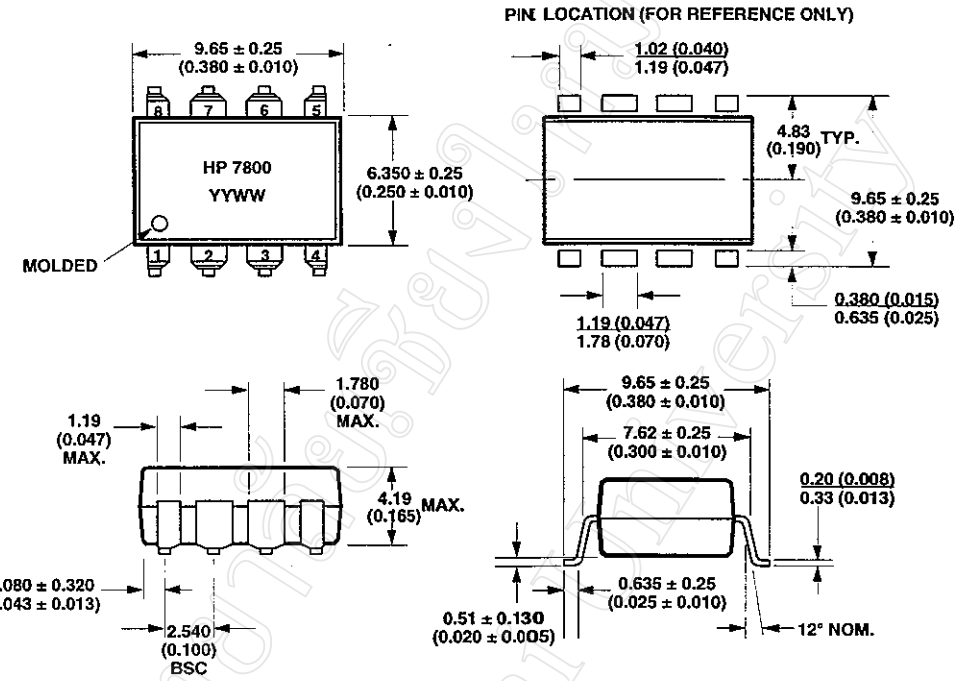
Standard DIP Package



DIMENSIONS IN MILLIMETERS AND (INCHES).

* TYPE NUMBER FOR: HCPL-7800 = 7800
HCPL-7800A = 7800A
HCPL-7800B = 7800B

Gull Wing Surface Mount Option 300*

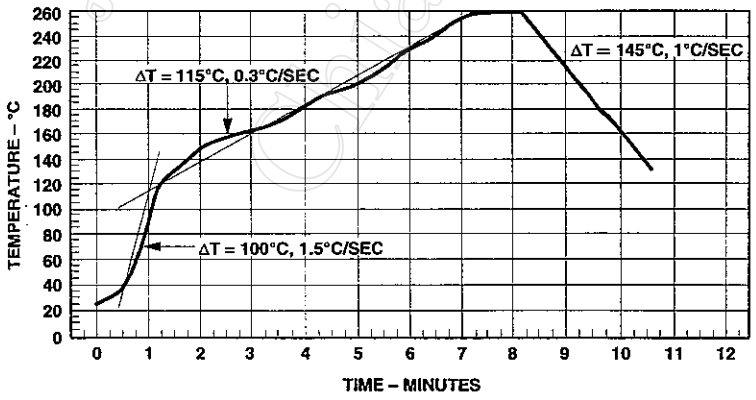


DIMENSIONS IN MILLIMETERS (INCHES).
TOLERANCES (UNLESS OTHERWISE SPECIFIED): xx.xx = 0.01
xx.xxx = 0.005

LEAD COPLANARITY
MAXIMUM: 0.102 (0.004)

* REFER TO OPTION 300 DATA SHEET FOR MORE INFORMATION.

Maximum Solder Reflow Thermal Profile



(NOTE: USE OF NON-CHLORINE ACTIVATED FLUXES IS RECOMMENDED.)

Regulatory Information

The HCPL-7800 has been approved by the following organizations:

UL	CSA	VDE
Recognized under UL 1577, Component Recognition Program, File E55361.	Approved under CSA Component Acceptance Notice #5, File CA 88324.	Approved according to VDE 0884/06.92.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (External Clearance)	L(IO1)	7.4	mm	Measured from input terminals to output terminals, shortest distance through air
Min. External Tracking Path (External Creepage)	L(IO2)	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body
Min. Internal Plastic Gap (Internal Clearance)		0.5	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity
Tracking Resistance (Comparative Tracking Index)	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		III a		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

VDE 0884 (06.92) Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 300 V rms for rated mains voltage ≤ 600 V rms		 I-IV I-III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110, Table 1)*		2	
Maximum Working Insulation Voltage	V_{IORM}	848	V peak
Input to Output Test Voltage, Method b** V_{PR} = 1.875 x V_{IORM}, Production test with t_p = 1 sec, Partial discharge < 5 pC	V_{PR}	1591	V peak
Input to Output Test Voltage, Method a** V_{PR} = 1.5 x V_{IORM}, Type and sample test with t_p = 60 sec, Partial discharge < 5 pC	V_{PR}	1273	V peak
Highest Allowable Overvoltage** (Transient Overvoltage t_{TR} = 10 sec)	V_{TR}	6000	V peak
Safety-limiting values (Maximum values allowed in the event of a failure, also see Figure 27) Case Temperature Input Power Output Power	 T_S $P_{S,Input}$ $P_{S,Output}$	 175 80 250	 °C mW mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 1 \times 10^{12}$	Ω

*This part may also be used in Pollution Degree 3 environments where the rated mains voltage is ≤ 300 V rms (per DIN VDE 0110).
**Refer to the front of the optocoupler section of the current catalog for a more detailed description of VDE 0884 and other product safety requirements.

Note: Optocouplers providing safe electrical separation per VDE 0884 do so only within the safety-limiting values to which they are qualified. Protective cut-out switches must be used to ensure that the safety limits are not exceeded.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage Temperature	T_S	-55	125	℃	
Ambient Operating Temperature	T_A	-40	100	℃	
Supply Voltages	V_{DD1}, V_{DD2}	0.0	5.5	V	
Steady-State Input Voltage	V_{IN+}, V_{IN-}	-2.0	V_{DD1} +0.5	V	
Two Second Transient Input Voltage		-6.0			
Output Voltages	V_{OUT+}, V_{OUT-}	-0.5	V_{DD2} +0.5	V	
Lead Solder Temperature (1.6 mm below seating plane, 10 sec.)	T_{LS}		260	℃	1
Reflow Temperature Profile	See **Package Outline Drawings** Section				

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Ambient Operating Temperature	T_A	-40	85	℃	2
Supply Voltages	V_{DD1}, V_{DD2}	4.5	5.5	V	3
Input Voltage	V_{IN+}, V_{IN-}	-200	200	mV	4
Output Current	$\|I_O\|$		1	mA	5

DC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input Offset Voltage	V_{OS}	-1.8	-0.9	0.0	mV		1	
Input Offset Drift vs. Temperature	dV_{OS}/dT		-2.1		µV/°C		1, 2	6
Abs. Value of Input Offset Drift vs. Temperature	$\|dV_{OS}/dT\|$		4.6		µV/°C		1	7
Input Offset Drift vs. V_{DD1}	dV_{OS}/dV_{DD1}		30		µV/V		1, 3	8
Input Offset Drift vs. V_{DD2}	dV_{OS}/dV_{DD2}		-40		µV/V		1, 4	9
Gain (± 5% Tol.)	G	7.61	8.00	8.40		-200 mV < V_{IN+} < 200 mV	1, 5	10
Gain - A Version (± 1% Tol.)	G_A	7.85	7.93	8.01				
Gain - B Version (± 1% Tol.)	G_B	7.99	8.07	8.15				
Gain Drift vs. Temperature	dG/dT		0.001		%/°C		5, 6	11
Abs. Value of Gain Drift vs. Temperature	$\|dG/dT\|$		0.001		%/°C		5	12
Gain Drift vs. V_{DD1}	dG/dV_{DD1}		0.21		%/V		5, 7	13
Gain Drift vs. V_{DD2}	dG/dV_{DD2}		-0.06		%/V		5, 8	14
200 mV Nonlinearity	NL_{200}		0.2	0.35	%		5, 9	15
200 mV Nonlinearity Drift vs. Temperature	dNL_{200}/dT		-0.001		% pts/°C		5, 10	16
200 mV Nonlinearity Drift vs. V_{DD1}	dNL_{200}/dV_{DD1}		-0.005		% pts/V		5, 11	17
200 mV Nonlinearity Drift vs. V_{DD2}	dNL_{200}/dV_{DD2}		-0.007		% pts/V		5, 12	18
100 mV Nonlinearity	NL_{100}		0.1	0.25	%	-100 mV< V_{IN+} < 100 mV	5, 13	19
Maximum Input Voltage Before Output Clipping	$\|V_{IN+}\|_{max}$		300		mV		14	
Average Input Bias Current	I_{IN}		-670		nA		15, 16	20
Input Bias Current Temperature Coefficient	dI_{IN}/dT		3		nA/°C			
Average Input Resistance	R_{IN}		530		kΩ		15	20
Input Resistance Temperature Coefficient	dR_{IN}/dT		0.38		%/°C			
Input DC Common-Mode Rejection Ratio	$CMRR_{IN}$		72		dB			21
Output Resistance	R_O		11		Ω			5
Output Resistance Temperature Coefficient	dR_O/dT		0.6		%/°C			
Output Low Voltage	V_{OL}		1.18		V	$\|V_{IN+}\|$ = 500 mV	14	22
Output High Voltage	V_{OH}		3.61		V	I_{OUT+} = 0 A, I_{OUT-} = 0 A		
Output Common-Mode Voltage	V_{OCM}	2.20	2.39	2.60	V	-40°C < T_A < 85°C 4.5 V < V_{DD1} < 5.5 V	14	
Input Supply Current	I_{DD1}		10.7	15.5	mA		17	23
Output Supply Current	I_{DD2}		11.6	14.5	mA	V_{IN+} = 200 mV, -40°C < T_A < 85°C 4.5 V < V_{DD2} < 5.5 V	18	24
Output Short-Circuit Current	$\|I_{OSC}\|$		9.3		mA	V_{OUT} = 0 V or V_{DD2}		25

AC Electrical Specifications

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Rising Edge Isolation Mode Rejection	IMR_R	10	25		kV/µs	V_{IM} = 1 kV	19, 20	26
Falling Edge Isolation Mode Rejection	IMR_F	10	15		kV/µs			
Isolation Mode Rejection Ratio at 60 Hz	IMRR		>140		dB		19	27
Propagation Delay to 10%	t_{PD10}		2.0	3.3	µs	-40°C < T_A < 85°C	21, 22	
Propagation Delay to 50%	t_{PD50}		3.4	5.6	µs			
Propagation Delay to 90%	t_{PD90}		6.3	9.9	µs			
Rise/Fall Time (10%-90%)	$t_{R/F}$		4.3	6.6	µs			
Bandwidth (-3 dB)	f_{-3dB}	50	85		kHz		23, 24	
Bandwidth (-45°)	$f_{-45°}$		35		kHz			
RMS Input-Referred Noise	V_N		300		µV rms	Bandwidth = 100 kHz	25, 26	28
Power Supply Rejection	PSR		5		mV_{p-p}			29

Package Characteristics

All specifications and figures are at the nominal operating condition of V_{IN+} = 0 V, V_{IN-} = 0 V, T_A = 25°C, V_{DD1} = 5.0 V, and V_{DD2} = 5.0 V, unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage*	V_{ISO}	3750			V rms	t = 1 min., RH ≤ 50%		30, 31
Input-Output Resistance	R_{I-O}	10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 Vdc		30
		10^{11}				T_A = 100°C, V_{I-O} = 500 Vdc		
Input-Output Capacitance	C_{I-O}		0.7		pF	f = 1 MHz		30
Input IC Junction-to-Case Thermal Resistance	θ_{jci}		96		°C/W			32
Output IC Junction-to-Case Thermal Resistance	θ_{jco}		114		°C/W			

*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the VDE 0884 Insulation Characteristics Table (if applicable), your equipment level safety specification, or HP Application Note 1074, "Optocoupler Input-Output Endurance Voltage."

ภาคผนวก ช

เครื่องแปลงผันแอนะลอกเป็นดิจิตอลเบอร์ ADC0820

National Semiconductor

April 1998

ADC0820
8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 µs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

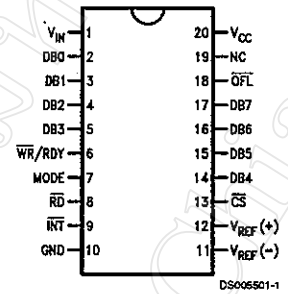
- Resolution: 8 Bits
- Conversion Time: 2.5 µs Max (RD Mode); 1.5 µs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/µs converted without external sample-and-hold to 8 bits
- Low Power: 75 mW Max
- Total Unadjusted Error: ± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

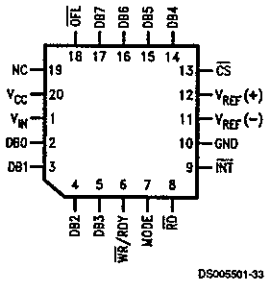
Connection and Functional Diagrams

Dual-In-Line, Small Outline and SSOP Packages



Top View

Molded Chip Carrier Package



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Connection and Functional Diagrams (Continued)

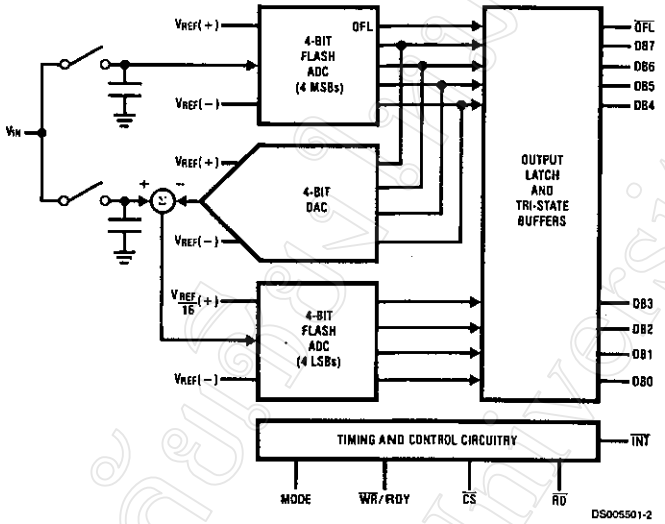


FIGURE 1.

See Ordering Information

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	10V
Logic Control Inputs	−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output	−0.2V to V_{CC} +0.2V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Input Current at Any Pin (Note 5)	1 mA
Package Input Current (Note 5)	4 mA
ESD Susceptability (Note 9)	1200V
Lead Temp. (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Notes 1, 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820CCJ	$-40°C \le T_A \le +85°C$
ADC0820CIWM	$-40°C \le T_A \le +85°C$
ADC0820BCN, ADC0820CCN	$0°C \le T_A \le 70°C$
ADC0820BCV, ADC0820CCV	$0°C \le T_A \le 70°C$
ADC0820BCWM, ADC0820CCWM	$0°C \le T_A \le 70°C$
ADC0820CCMSA	$0°C \le T_A \le 70°C$
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7=0), V_{CC}=5V, $V_{REF}(+)$=5V,and $V_{REF}(-)$=GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A=T_J$=25°C.

Parameter	Conditions	ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			8			8	8	Bits
Total Unadjusted Error (Note 3)	ADC0820BCN, BCWM		±1			±½	±½	LSB
	ADC0820CCJ							LSB
	ADC0820CCN, CCWM, CIWM,					±1	±1	LSB
	ADC0820CCMSA					±1	±1	LSB
Minimum Reference Resistance		2.3	1.00		2.3	1.2		kΩ
Maximum Reference Resistance		2.3	6		2.3	5.3	6	kΩ
Maximum $V_{REF}(+)$ Input Voltage			V_{CC}			V_{CC}	V_{CC}	V
Minimum $V_{REF}(-)$ Input Voltage			GND			GND	GND	V
Minimum $V_{REF}(+)$ Input Voltage			$V_{REF}(-)$			$V_{REF}(-)$	$V_{REF}(-)$	V
Maximum $V_{REF}(-)$ Input Voltage			$V_{REF}(+)$			$V_{REF}(+)$	$V_{REF}(+)$	V
Maximum V_{IN} Input Voltage			V_{CC}+0.1			V_{CC}+0.1	V_{CC}+0.1	V
Minimum V_{IN} Input Voltage			GND−0.1			GND−0.1	GND−0.1	V
Maximum Analog Input Leakage Current	$\overline{CS}$ =V_{CC}							
	V_{IN}=V_{CC}		3			0.3	3	µA
	V_{IN}=GND		−3			−0.3	−3	µA
Power Supply Sensitivity	V_{CC}=5V±5%	±1/16	±¼		±1/16	±¼	±¼	LSB

DC Electrical Characteristics

The following specifications apply for V_{CC}=5V, unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX}**; all other limits $T_A=T_J$=25°C.

Parameter	Conditions		ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
$V_{IN(1)}$, Logical "1" Input Voltage	V_{CC}=5.25V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		2.0			2.0	2.0	V
		Mode		3.5			3.5	3.5	V
$V_{IN(0)}$, Logical "0" Input Voltage	V_{CC}=4.75V	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		0.8			0.8	0.8	V
		Mode		1.5			1.5	1.5	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)}$=5V; $\overline{CS}$, $\overline{RD}$		0.005	1		0.005		1	µA
	$V_{IN(1)}$=5V; $\overline{WR}$		0.1	3		0.1	0.3	3	µA
	$V_{IN(1)}$=5V; Mode		50	200		50	170	200	µA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)}$=0V; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	−1		−0.005		−1	µA
$V_{OUT(1)}$, Logical "1" Output Voltage	V_{CC}=4.75V, I_{OUT}=−360 µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			2.4			2.8	2.4	V
	V_{CC}=4.75V, I_{OUT}=−10 µA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			4.5			4.6	4.5	V
$V_{OUT(0)}$, Logical "0" Output Voltage	V_{CC}=4.75V, I_{OUT}=1.6 mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.4			0.34	0.4	V
I_{OUT}, TRI-STATE Output Current	V_{OUT}=5V; DB0–DB7, RDY		0.1	3		0.1	0.3	3	µA
	V_{OUT}=0V; DB0–DB7, RDY		−0.1	−3		−0.1	−0.3	−3	µA
I_{SOURCE}, Output Source Current	V_{OUT}=0V; DB0–DB7, $\overline{OFL}$		−12	−6		−12	−7.2	−6	mA
	$\overline{INT}$		−9	−4.0		−9	−5.3	−4.0	mA
I_{SINK}, Output Sink Current	V_{OUT}=5V; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	7		14	8.4	7	mA
I_{CC}, Supply Current	$\overline{CS}$ =$\overline{WR}$ =$\overline{RD}$ =0		7.5	15		7.5	13	15	mA

AC Electrical Characteristics

The following specifications apply for V_{CC}=5V, $t_r=t_f$=20 ns, $V_{REF}(+)$=5V, $V_{REF}(-)$=0V and T_A=25°C unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *Figure 2*	1.6		2.5	µs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *Figure 2*	t_{CRD}+20		t_{CRD}+50	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, t_{RD}=600 ns; *Figures 3, 4*			1.52	µs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *Figures 3, 4*		600		ns
	Max	(Note 4) See Graph	50			µs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *Figures 3, 4* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, t_{RD}<t_i; *Figure 3* C_L=15 pF	190		280	ns
		C_L=100 pF	210		320	ns

AC Electrical Characteristics (Continued)

The following specifications apply for V_{CC}=5V, t_r=t_f=20 ns, $V_{REF}(+)$=5V, $V_{REF}(-)$=0V and T_A=25°C unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)	Pin 7 = V_{CC}, t_{RD}>t_l; *Figure 4*				
	C_L=15 pF	70		120	ns
	C_L=100 pF	90		150	ns
t_{ACC3}, Access Time (Delay from Rising Edge of RDY to Output Valid)	R_{PULLUP} = 1k and C_L = 15 pF	30			ns
t_l, Internal Comparison Time	Pin 7=V_{CC}; *Figures 4, 5* C_L=50 pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	R_L=1k, C_L=10 pF	100		200	ns
$t_{\overline{INTL}}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, C_L= 50 pF				
	t_{RD}>t_l; *Figure 4*			t_l	ns
	t_{RD}<t_l; *Figure 3*	t_{RD}+200		t_{RD}+290	ns
$t_{\overline{INTH}}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*Figures 2, 3, 4* C_L=50 pFc	125		225	ns
$t_{\overline{INTHWR}}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*Figure 5*, C_L=50 pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*Figure 2*, C_L=50 pF, Pin 7 =0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*Figure 5*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7=V_{CC}, t_{RD}<t_l *Figure 3*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*Figures 2, 3, 4, 5* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/μs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RD} graphs.

Note 5: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < V^- or V_{IN} > V^+) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

ภาคผนวก ซ

การ์ด ISA

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ISA CARD อเนกประสงค์

จากการทำโปรเจคของนักศึกษาที่ผ่านๆ มา มักมีความจำเป็นต้องใช้การ Interface PC เพื่อรับส่ง ข้อมูลเข้าออก ระหว่าง PC กับ อุปกรณ์ภายนอกต่าง ๆ ซึ่งเมื่อทำโปรเจคหนึ่งก็มักจะต้องสร้าง ISA card Interface เพื่อใช้ในการทำ Project ทำให้บั่นทอนเวลาในการทำโปรเจคในส่วนที่ต้องการจริง ๆ เป็นอย่างมาก จึงเกิดแนวความคิดที่จะทำ ISA card อเนกประสงค์ ให้สามารถนำไปประยุกต์ใช้งานได้หลากหลาย โดยใช้ต้นทุนที่ต่ำเพื่อให้สามารถนำไปประยุกต์ใช้งานได้ง่ายและมีประสิทธิภาพ

ลักษณะการทำงาน

1. เป็น ISA card อเนกประสงค์โดยใช้หลักการ Mother-Daughter Board โดยจะแบ่งการทำงานเป็นสองส่วนคือส่วนที่เป็นส่วนหลัก (Mother Board) ทำหน้าที่ในส่วนของการเป็น Address Decode ซึ่งเป็นส่วนพื้นฐานในการทำงานเพื่อรองรับการเชื่อมต่อของ Daughter board และส่วนการ์ดย่อย (Daughter Board) คือส่วนที่เพิ่มเติม เพื่อการใช้งานใช้เฉพาะทาง ผู้ใช้สามารถสร้างให้เหมาะสมกับงานที่ต้องการได้ง่าย

2. เป็น ISA card ที่สามารถเลือก Address ทำงานได้ 8 ช่วงค่าโดยใช้ dip switch เป็นตัวเลือกเพื่อไม่ให้ค่า Address ซ้ำกับอุปกรณ์ตัวอื่นที่ติดตั้งไปแล้ว โดยจะมีสามารถเลือกขอบเขตของ Address ได้ตั้งแต่ 200h – 3FFh

3. ในแต่ละช่วงค่าของ Base Address สามารถแบ่งเป็น Address ย่อยเพื่อติดต่อกับอุปกรณ์อื่น อีกได้ถึง 64 อุปกรณ์

การทำงาน

Address Decode

การทำงานด้าน Address decode จะอยู่ในส่วนของ Mother Board ซึ่งจะใช้สัญญาณ Address 10 เส้น ในการทำงาน โดยมีการทำงานดังนี้

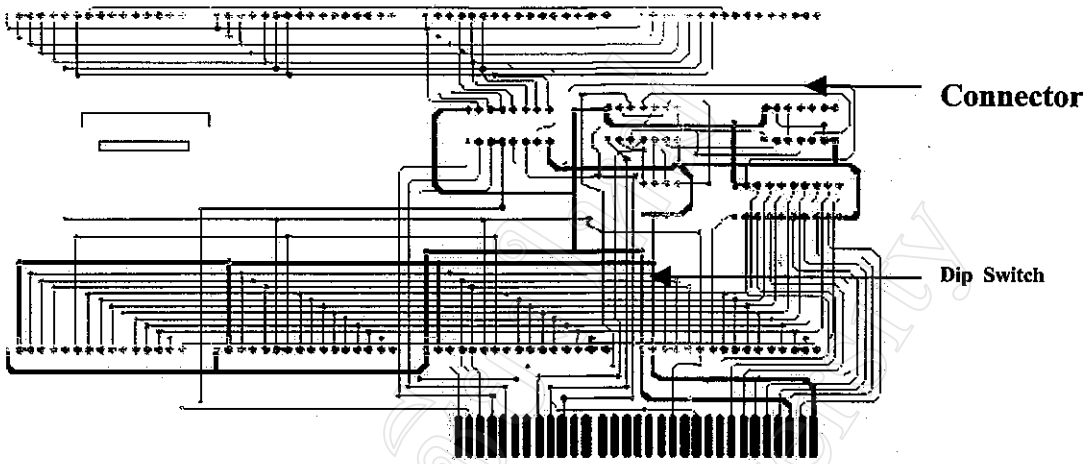
A9 เป็น Address ที่ระบุการทำงานว่าเป็น IO หรือไม่ ถ้าเป็นต้อง set เป็น 1

A6-A8 เป็น Address ที่ระบุ Base Address สามารถเลือกได้โดยใช้ DIP switch

A3-A5 เป็น Address ที่จะนำเข้า IC74LS138 เพื่อเป็น Demultiplex ในการ Enable การทำงานของ Daughter Board เพื่อเลือกการทำงานว่าจะใช้งาน Daughter Board ตัวใด (Address ใด)

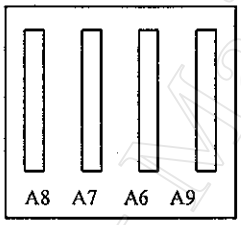
A0-A2 เป็น Address ที่จะส่งขึ้น Daughter Board เพื่อเป็น Address ในการเลือกอุปกรณ์ บน Daughter Board และถ้าใช้ IC 74138 บน Daughter Board อีกจะทำให้สามารถติดตั้งอุปกรณ์บน Daughter Board ได้ถึง 8 ตัว

ฉะนั้น ความสามารถของการ์ด Pdp ISA สูงสุด จึงสามารถรองรับการทำงานของอุปกรณ์ได้ทั้งสิ้น 64 อุปกรณ์ ต่อ Address base หนึ่งค่า โดย สามารถเลือก Address base ได้ 8 ช่วงค่า



รูปที่ 1 แสดงลักษณะของลายวงจร Card ISA PDP โดยใช้ Protel

จากรูปที่ 1 จะเป็นการแสดงลักษณะของ ISA card อย่างคร่าว ๆ ซึ่งจะมี connector เป็น pin 16 ตัวเมียสองตัวในการเชื่อมต่อกับ Daughter Board ซึ่งจะได้อธิบายรายละเอียดต่อไป และ มี Dip switch 4 channel เพื่อเป็น ตัว Set Base Address (A9-A6) ซึ่งมีลักษณะดังนี้



รูปที่ 2 แสดงลักษณะของ Dip switch และ Address

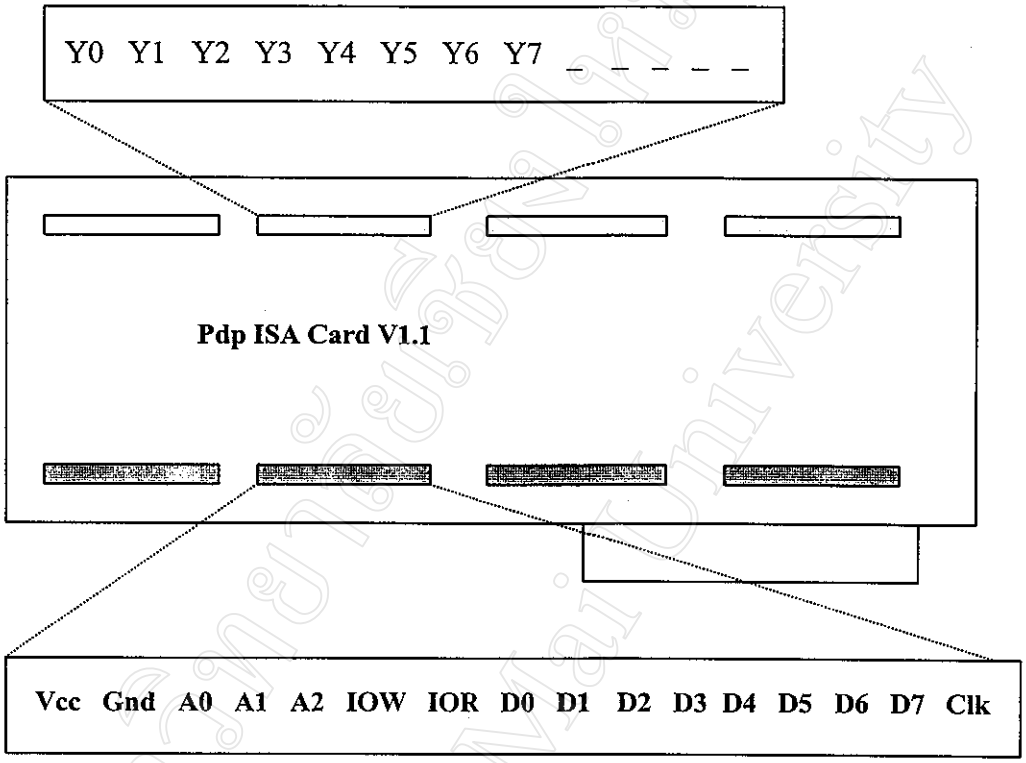
การกำหนด Address ส่วน Base Address นั้น จะใช้ Dip Switch ในการเลือกค่าที่ต้องการของสัญญาณ Address A6-A9 โดยการ set จะมีลักษณะดังนี้

- ถ้า Dip Switch ON แสดงว่าต้องการให้สัญญาณ Address เส้นนั้นเป็น 0 Logic LOW
- ถ้า Dip Switch OFF แสดงว่าต้องการให้สัญญาณ Address เส้นนั้นเป็น 1 Logic HIGH

ลักษณะการเรียง Address จะเป็นดังรูปที่ 2 คือ A8 A7 A6 และ A9 ตามลำดับ (โดยส่วนของ A9 ได้กำหนดไว้ว่าต้องเป็น 1 เสมอ คือ OFF Switch ตลอด)

ตัวอย่างเช่นต้อง การ Base Address เป็น 200H ก็ต้อง Set Dip Sw ตามลำดับดังนี้ On On On Off (0 0 0 1) เป็นต้น

สัญญาณบน Pdp ISA Card



รูปที่ 3 แสดงรูปลักษณะขาสัญญาณบน Pdp ISA Card

ลักษณะขาสัญญาณที่ Mother Board ส่งไปให้ Daughter Board มีลักษณะดังรูปที่ 3 โดย Daughter Board จะใช้ Connector สอง ตัวในการเชื่อมต่อกับ Mother Board โดยส่วนล่างจะเป็นสัญญาณควบคุม Address Data ต่าง ๆ ส่วนด้านบนจะเป็นสัญญาณ Address Active เพื่อ เลือกการทำงานว่าจะติดต่อกับ Daughter Board ตัวใดประกอบไปด้วย Y0-Y7 โดยมีรายละเอียดดังนี้

VCC GND

จะเป็น Vcc และ Gnd ที่ต่อเชื่อมกับไฟของระบบโดยตรง โดย Vcc จะมีค่า 5 Volt

A0 – A2

จะเป็นสัญญาณ Address ของระบบเพื่อส่งขึ้นไปยัง Daughter Board เพื่อเลือก Active การทำงานของอุปกรณ์บน Daughter Board

IOW

สัญญาณ I/o Write เพื่อบอกสถานะการใช้ Bus ว่าต้องการเขียนค่าลงอุปกรณ์ภายนอกหรือไม่ โดยสัญญาณนี้ จะ Active Low

IOR

สัญญาณ I/o Read เป็นสัญญาณ Active Low อีกเช่นกัน เพื่อบอกสถานะการใช้ Bus ว่าต้องการอ่านค่าจากอุปกรณ์ภายนอกหรือไม่

D0-D7

เป็นสัญญาณจาก Data Bus เป็นข้อมูลขนาด 8 bit ซึ่งได้ผ่านอุปกรณ์ Tri State มาแล้วเพื่อป้องกันการเกิดการรบกวนของข้อมูลภายนอกกับข้อมูลภายในระบบ

CLK

เป็น Clock ของระบบซึ่งต่อขึ้นมาโดยตรงจากขา B20 ซึ่งเป็น clock ที่สร้างขึ้นโดยการหารสัญญาณ OSC ด้วย 3 (ปกติ OSC มีความถี่ 14.31818 MHz) ทำให้ได้ความถี่ประมาณ 4.77 MHz มี Duty Cycle ของสัญญาณจะมีค่าประมาณ 1/3 คือ ใน 1 คาบจะช่วงที่เป็นลอจิก 1 เท่ากับ 1/3 ของคาบเวลาทั้งหมด

Y0 – Y7

สัญญาณ Y0-Y7 เป็นสัญญาณ Active การทำงานของ Daughter Board แบบ Active Low ซึ่งสัญญาณนี้ได้มาจากการ Demultiplex ของ Address A3-A5 ตัวอย่างเช่น ถ้าเรา Set Base Address ไว้ที่ 200H และต้องการติดต่อกับ Daughter Board ที่ใช้ Y1 Active ก็จะมี address เป็น

1 0 0 0 0 0 1 0 0 0 สัญญาณ A9 – A0

หรือก็คือ 208H นั่นเอง โดยในด้านของ Daughter Board ก็ถูกสร้างมาให้สนับสนุนการทำงานในการเลือกว่าจะใช้สัญญาณ Yใด ในการ Active อีกเช่นกัน

การใช้งาน

การติดตั้ง Address

เนื่องจากตัวการ์ดเป็นลักษณะ Mother – Daughter Board จึงต้อง Set Address ทั้งส่วนหลักและส่วนย่อย โดยส่วนที่การ์ดหลักจะตั้งค่า Address โดยใช้ dip Switch (สีฟ้า บน mother board) ส่วนการตั้งค่า Address ของ Daughter board จะใช้ jumper ตรงส่วนบนของ daughter board แต่ละตัว โดยมีรายละเอียดดังนี้

1. รายละเอียด Address

จะใช้ Address จากระบบ (คอมพิวเตอร์ทั้งหมด 10 เส้น A0 – A9) ประกอบกับการตรวจสอบสัญญาณส่วนอื่นๆ ทำให้สามารถเลือกการทำงานดังที่ต้องการได้ดังนี้

- A9 – A6 เป็นการเลือก Address หลัก (ตามรูปที่ 2)

  (//// ควรตั้งให้ A9 เป็น 1 โดยการ off switch ขวามือเสมอ ////)

- A3 – A5 จะใช้ในการเลือก Daughter board โดยการกำหนดที่ jumper ของ daughter board โดยเป็นลักษณะดังนี้

A3	A4	A5	jumper ที่ใส่
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

(/// ใช้ jumper ตัวเดียวเท่านั้น ในการเลือก Daughter board

และ อย่าตั้งให้ Address ของ Daughter board แต่ละตัวตรงกัน /////)

ฉะนั้นจะเห็นว่าสามารถต่อ Daughter Board เพิ่มได้ถึง 8 ตัว แต่ขนาดของการ์ดมีจำกัดจึงมีช่องต่อเพียง 4 ช่องเท่านั้น

- A0 – A2

จะเป็นการเลือก อุปกรณ์บน Daughter ว่าจะใช้ IC ตัวใด โดยใช้ลักษณะเดียวกับ daughter board กล่าวคือ

A2	A1	A0	เลือกใช้ไอซีตัวที่
0	0	0	0
0	0	1	1
0	1	0	2
1	1	1	7

โดยนับลำดับของ IC จากบนลงล่าง

ดังเช่น ถ้าตั้งค่า dip switch เป็น on off off on ตามลำดับและ set jumper เป็นตัวที่ 1 (ลำดับที่ 2) และใช้ IC เป็นตัวแรก จะได้ค่า Address ดังนี้

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	0	1	0	0	0
Dip Switch				**Daughter Board**			**IC ตัวแรก**		

แปลงค่า Address เป็นฐาน 16 ได้เป็น 0x308

2. วิธีการเขียนโปรแกรม

เช่นการรับค่าจาก อุปกรณ์

```
#include<dos.h>
#include<stdio.h>
main()
{
        unsigned char data;
        data = inportb(0x308);   // รับค่าเข้ามาจาก port 0x308
        printf("%x",data);       // แสดงค่าในเลขฐาน 16
}
```

หรือเมื่อต้องการส่งค่า ออกไปยังอุปกรณ์ก็ใช้คำสั่ง

```
outportb(port,value);  // ส่งค่า value ออกที่ port
```

3. ลักษณะการ์ด

<u>การ์ด DO-32 v1.1</u>

จะเป็นการ์ด Daughter Board ในการส่งค่า Digital ได้ขนาด 32 bits (8 bits x 4 Channel) สัญญาณไฟฟ้าจะเป็น TTL โดยใช้ IC Flipflop เบอร์ 74LS374

การ์ด DI-48 V1.1

จะเป็นการ Daughter Board ในการรับค่า digital โดยจะค่าได้ทั้งหมด 48 bits (8 biits x 6 channel) สัญญาณไฟฟ้าเป็น TTL โดยใช้ IC 3-state เบอร์ 74LS245

โดยจะเรียงลำดับ Address ของ IC จากตัวบนถึงตัวล่าง ตัวบนจะเป็นตัวที่ 0 และไล่มาตามลำดับ ซึ่งบนตัวการ์ดจะมีสัญญาณไฟ 5 Volt และ Gnd เพื่อใช้ในการต่อเชื่อมกับอุปกรณ์ส่วนอื่น ๆ

ข้อควรระวัง

1. ห้าม short circuit ระหว่าง Gnd และ Vcc เพราะเป็นระบบไฟหลักของเครื่อง PC โดยตรง
2. ควรสังเกตวงจรที่จะนำไปต่อร่วมให้ดี ด้านแรงดันไฟฟ้าและกระแส
3. ควรต่อวงจรในลักษณะ common ground

(*////// เนื่องจากราคาการ์ด มีราคาถูกมาก จึงไม่ขอรับผิดชอบในการเสียหายที่เกิดขึ้น จากการทำงานของผู้ใช้งาน)

ประวัติผู้เขียน

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