Development of a CMOS Frequency to Voltage Converter

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Abstract. *This article proposes a high performance frequency-to-voltage converter (FVC). The proposed circuit has a simple structure which consists of just only one current source, one Logic Controller Block (LCB), two capacitors and four MOS transistors to generate different phase shifts in time domain using the switched capacitor control technique. To validate the feasibility of the proposed circuit and its theoretical operation, the circuit has been simulated by using the PSpice simulation program. The proposed circuit provides the output voltage dependent on the input signal frequency which can operate in the wide range of frequencies varying from 2.5 to 125 MHz, as well as, providing the stable output voltage levels by the number of N of approximately 8 cycles of input signals with high accuracy of 0.4 %. The power consumption of the circuit is relatively low at about 0.25 mW at 5 V supply voltage.*

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1. Introduction

The frequency-to-voltage converter (FVC) has many applications in communication, instrumentation systems, motor speed control, isolated data transmission and etc. [1]. The FVC is the one part of electronic circuits that has important and widely used with the reasons such as high-speed operation, good linearity, wide frequency range, and low output ac ripples [2-4].

From literature studies, the technique and concept of FVC circuit design can be divided into 2 methods. The first method is based on low-pass filtering of the fixed duration pulses at a rate set by the input frequency [5-8]. The second method is based on counting the number of narrow pulses over a fixed period of time [2]. As above mentioned regarding the FVC design methods, they are both based on the complex circuits, high power consumption and unsuitable for modem integrated applications [5-8].

Therefore, in this paper, we purposed a high performance of CMOS frequency to voltage converter. The proposed circuit consists of one current source, one Logic Controller Block (LCB), two capacitors and four MOS transistors. These devices help to generate different phase shifts in time domain by using the switched capacitor technique for control frequency-to-voltage converter and thus provide high accuracy voltage output while consume lower power than the previous design methods. In addition, the proposed circuit can operate also at a wide frequency variation range and fast response time. To confirm the validity of the proposed circuit, the circuit has been simulated by using the Pspice simulation program.

2. Circuit Configuration and Operation of Frequency-to-Voltage Converter (FVC)

The proposed FVC circuit consists of a current source I_C, a Logic Controller Block (LCB), two capacitors C_1 and C_2 and four MOS transistors (M_{n1}, M_{n2}, M_{n3} and M_{p1}), which is defined to operate as switches, it's called switched capacitor and LCB as shown in Fig. 1 (a). The input signal of LCB generated the signals Φ_1 and Φ_2 to control the MOS transistors M_{n1} and M_{n2} as shown in Fig. 1 (b). The time period of the signals Φ_1 and Φ_2 are the same values which is in the form of the pulse signals (~2 nS) and both Φ_1 and Φ_2 signals have the same frequency, while the Φ_1 and Φ_2 signals provided different phases as shown in Fig. 1(c). The M_{p1} and M_{n3} are controlled directly from input signal V_{in}. The MOS transistors M_{n1} and M_{n2} are controlled with Φ_1 and Φ_2 signals to control the switched capacitors, which generated from input signal during half time period of T as shown in Fig. 1 (c).

The Φ_1 and Φ_2 signals are generated from the LCB as shown in Fig. 1(b) consists of two AND gates and five inverters. The main function of the inverters I_1-I_5 are designed for time delay of τ_1 and τ_2 with different phase.

The input of AND gate (and$_1$) connected with node of V_{x1} and input of inverter I_3 to generate the output signal Φ_1. The Φ_2 signal is generated by AND gate (and$_2$), inverter I_4 and I_5. Both of output signals Φ_1 and Φ_2 have the same frequency as the input V_{in}.

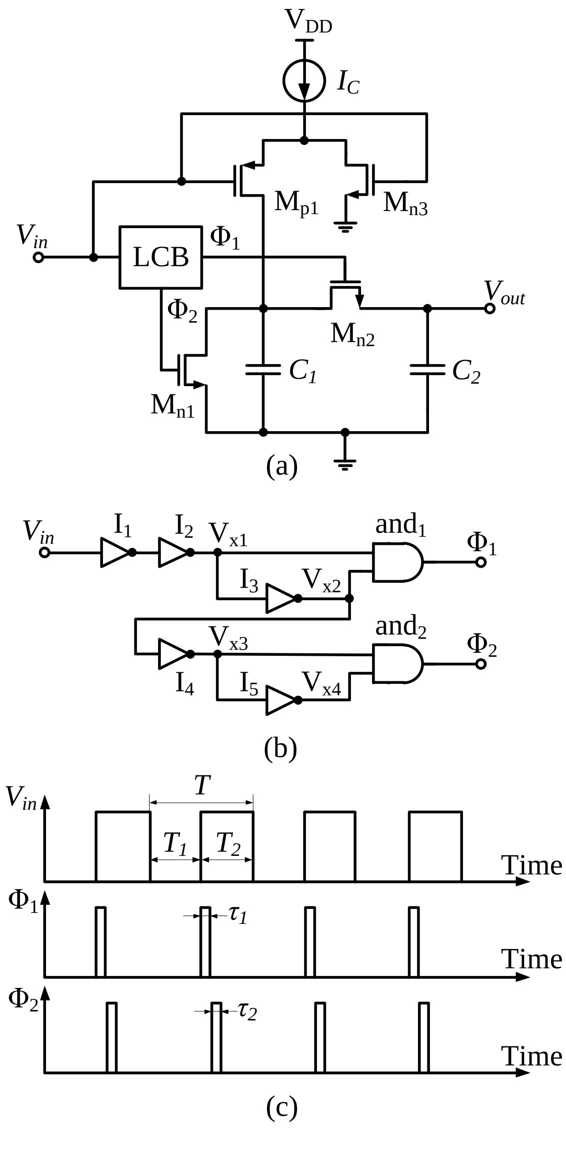

Fig. 1: circuit configuration and operation of the proposed frequency to voltage circuit: (a) The frequency-to-voltage converter; (b) logic controller block and (c) V_{in} signal, Φ_1 and Φ_2.

At the time of T_1 is a low level, the M_{p1} will be turned on while M_{n3}, M_{n1} and M_{n2} will be turned off by controlling from the LCB with the Φ_1 and Φ_2 signals. In this case, capacitor C_1 will be charged with the current I_C as shown in the Fig. 2 (a). The M_{n3} is responsible for reducing the voltage error that may occur during the switching of the M_{p1}. To charge of capacitor C_1 depends on the time period T_1 when the input signal changes to a high level, the capacitor C_1 will stop charging. Then, Φ_1 signals from the LCB raise up to a high level in a short period of time τ_1 in order to M_{n2} is turned on. At the same time, M_{n1} and M_{p1} are turned off. After the M_{n2} turned on and capacitor C_1 is completely charged and then the capacitor C_1 will be transferred the current to capacitor C_2 until the voltage across C_2 equal to C_1 as shown in Fig. 2 (b). When the Φ_1 signal returns to low level again and the Φ_2 signal goes to a high level in a short time period of T_2, and M_{n1} will be turned on for discharging the capacitor C_1 as shown in Fig. 2 (c).

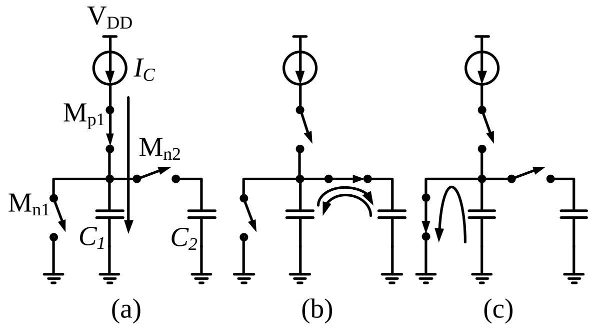

Fig. 2: (a) Capacitors C_1 will be charged with the current I_C; (b) charge distribution of C_1 and C_2; and (c) discharge the capacitor C_1.

If the frequency of the input signal is stable. For the reasons mentioned above, the operation process will be repeated. The voltage across C_2 is output voltage which is generated from charging of capacitor C_1 with directly proportional to the time period of T_1 and is given by:

$$V_{out} = \frac{I_C}{C_1} T_1 \tag{1}$$

If the input signal is a symmetrical square wave with 50 % of the duty cycle, the equation (1) can be expressed directly in terms of f by.

$$V_{out} = \frac{I_C}{C_1}\left(\frac{T}{2}\right) = \frac{I_C}{C_1}\left(\frac{1}{2f}\right) \tag{2}$$

From Equation (2), the output voltage of the proposed circuit which is directly proportional to the time T of the input signal and the time of T can be changed to the frequency f. When the input frequency is changed. As a consequence, the output voltage is also changed. The operating range of proposed FVC from equation (2) shown that the output voltage depends on the charging of capacitor C_1 and frequency f or ($1/T$) in time domain of the input signals. The output voltage levels are defined between the ground to the V_{DD}. Therefore, the relations of the current I_C, C_1, $f_{\min}$ and $f_{\max}$ are illustrated in equations (3) and (4).

$$f_{\min} = \frac{I_C}{2C_1}\left(\frac{1}{V_{\max}}\right) \quad (3)$$

and

$$f_{\max} = \frac{I_C}{2C_1}\left(\frac{1}{V_{\min}}\right) \quad (4)$$

From equation (3) and (4), it can be seen that the frequency range of the proposed circuit can increase or decrease depending on the I_C current and capacitor value C_1, the operating frequency of the proposed circuit cannot be lower or higher than the minimum and maximum frequencies ($f_{\min}$ *and* $f_{\max}$). Because of the maximum frequency ($f_{\max}$) is limited by the time period of τ_1 and τ_2 which have phase difference.

To calculate the maximum absolute frequency is given by:

$$f_{a\max} = \frac{1}{2(\tau_1 + \tau_2)} \quad (5)$$

The response time of the proposed circuit is the time that corresponds to the time required for charging C_2 to achieve the final charge as shown in the Fig. 2 (c). The final charge of C_1 acquired at the end T_1. If the frequency of the input signal is constant and the capacitor C_1 and C_2 are equal, the first interval V_{out} is equal to half of V_{C1} (this is the result of new charge distribution between C_1 and C_2). Similarly, the second phase V_{out} will increase half of the difference between V_{C1} and V_{out} that displayed as equation (6) [5].

$$V_{out} = \frac{1}{2^1}V_{C1} + \frac{1}{2^2}V_{C1} + \frac{1}{2^3}V_{C1} + ... + \frac{1}{2^N}V_{C1} \quad (6)$$

Where N is the number of input signals and can be given by:

$$V_{out} = V_{C1}\left(1 - \frac{1}{2^N}\right) \quad (7)$$

From the equation (7), the error ΔV_{out} value which has the difference between V_{C1} and V_{out} can be shown as:

$$\Delta V_{out} = V_{C1}\frac{1}{2^N} \quad (8)$$

From equation (8), to reduce the error of ΔV_{out}, the value of N should be more than 8 cycles.

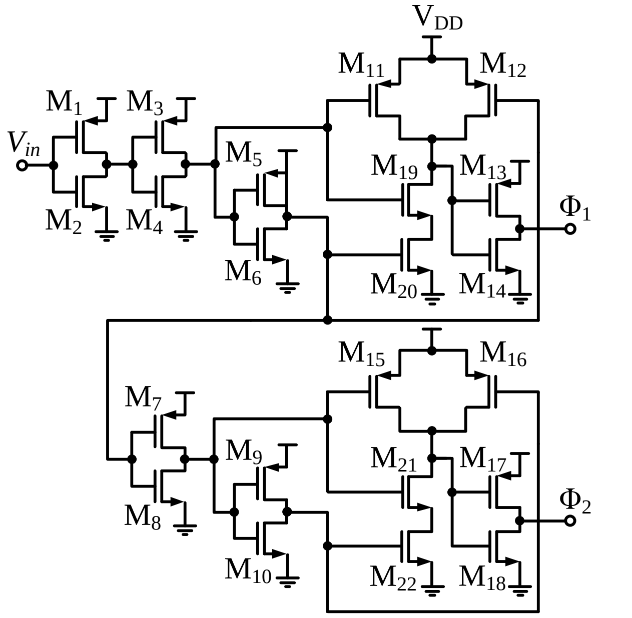

Fig. 3: Internal construction of LCB circuit.

3. Simulation results

To confirm the validity of the proposed circuit in this paper, the Pspice program was used in cooperating with the 0 .3 5 µm parameter, TSMC model, CMOS technology, the supply voltage at 5 V, current I_C is defined to 5 0 µA. The aspect ratio of MOS transistors (M_{n1} and M_{n2}) are defined to be equal to W= 10 µm/ L= 0.7 µm and M_{p1} and M_{n3} are equal to W= 10 µm /L = 1.4 µm, the value of capacitors $C_1 = C_2 =$ 2 pF. The aspect ratio of the MOS transistors that are used in the LCB circuit as shown in Fig. 3 composed of the MOS transistors M_1-M_{18} (W= 10 µm / L = 1.4 µm) and M_{19}-M_{22} (W= 40 µm / L= 1.4 µm).

From Fig. 4, the input signal V_{in} is the square wave with duty cycle 50 %. The proposed circuit is tested the operating frequency at 10 MHz, LCB generate phase shift with pulse width τ_1 and τ_2 of Φ_1 and Φ_2 signals are equal 2 nS as shown in Fig. 5, provides output voltage (V_{out}) 1.25 V at 800 nS as shown in Fig. 6, which corresponds to the response time of the converter as shown in Fig. 6.

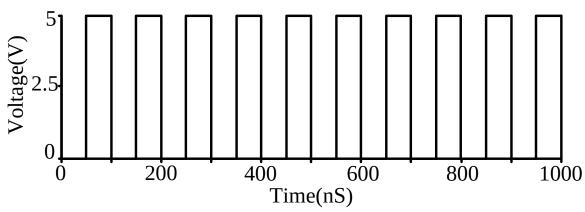

Fig. 4: Input signal is a square waveform of 10 MHz.

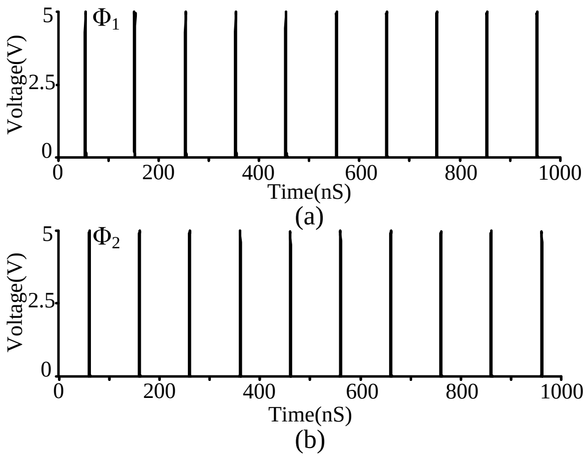

Fig. 5: Φ_1 and Φ_2 signals in time domain.

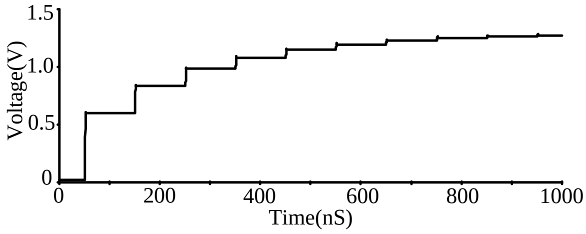

Fig. 6: The output voltage of proposed FVC.

After this period, the proposed circuit provides stable output voltage (V_{out}) without increasing of the ac ripple, so the proposed circuit doesn't need to use the low pass filter before sending the V_{out} signal the next circuit for signal processing.

4. Conclusions

This paper presents the development of a CMOS frequency to voltage converter which consists of a one LCB, two capacitors and four MOS transistors using switched capacitor technique for controlling the frequency-to-voltage converter. The proposed circuit is designed by a simple structure, it can be operated at wide frequency range from 2.5 MHz to 125 MHz and provided the stable output voltage levels by the number of *N* of about 8 cycles of input signals, which has accuracy at 0.4 %, the power consumption of about 0.25 mW at 5 V supply voltage.

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References

[1] Gupta, K., Bhardwaj, M. and Singh, Prof. B. P. (2012), Design and Analysis of CMOS Frequency to Voltage Converter using 0.35μm technology, *Applied International Journal of Scientific & Engineering Research*, Volume 3, Issue 5, May-2012 ISSN 2229-5518.

[2] anlop, S., Yongyut, C. and Suree B. (1991), An analog Sinusoidal Frequency- to-Voltage Converter, *Applied IEEE Transactions on Instrumentation and Measurement*, vol.40, no.6, Dec 1991.

[3] Bui, H.T. and Savaria, Y. (2008), Design of a high-speed differential frequency-to-voltage converter and its application in a 5-GHz frequency-locked loop, *Applied IEEE Transactions Circuits and Syst.*, vol. 55, pp. 766-774, 2008.

[4] Singh, M. and Sahu, P.P. (2013), A wideband linear sinusoidal frequency to voltage converter with fast response time, paper presented in *International Conference on Design and Manufacturing*, IConDM 2013.

[5] Djemouai, A., Sawan , M. and Slamani, M.(1998), High performance integrated CMOS frequency-to-voltage converter, paper presented in *the Tenth International Conference on Microelectronics*, 14-16 Dec. 1998.

[6] Djemouai, A., Sawan, M. and Slamani, M.(1999), High performance integrated CMOS frequency-to-voltage converter, paper presented in *IEEE International Conference on Electronics, Circuits and Systems*, 5-8 Sept.1999.

[7] Djemouai, A., Sawan, M. A. and Slamani, M.(2001), New frequency - locked loop based on CMOS frequency-to- voltage converter: Design and implementation, *Applied IEEE Trans. Circuits Syst. II Analog Digit. Signal Process*,vol.48, pp. 441-449, 2001.

[8] Mohd, F. and Yasin, K.F. (2009), Signal processing circuitry for CMOS-based SAW gas sensors with low power and area, *Applied International Atomic Energy Agency (IAEA)*,vol. 42, Issue.30, 2009.

Biographies

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