ภาคผนวกที่ 1

Reflection Grating

Edmund Scientific

INFORMATION AND INSTRUCTIONS

INSTRUMENT QUALITY PLANE REFLECTION GRATINGS
Nos. 41,013–41,048

	Grooves per inch	15,240 (600/mm)	15,240 (600/mm)	30,480 (1200/mm)	30,480 (1200/mm)
	Blaze wave length	4,000A	5,000A	2,400A	4,000A
Size	Groove lgth.	Ruled Width	Stock No.	Stock No.	Stock No.	Stock No.
½" x 1"	½"	1"	41,021	41,030	41,039	41,048
1" x 1"	1"	1"	41,019	41,028	41,037	41,046
2" x 2"	2"	2"	41,016	41,025	41,034	41,043
4" x 4"	4"	4"	41,013	41,022	41,031	41,040

Examination of the replica's surface may reveal small imperfections which will have little if any effect upon the spectrum. The grating should not be touched with your fingers, and if inadvertently the grating becomes soiled, DO NOT ATTEMPT to clean the ruled surface with lens tissue, or cotton swabs. In most cases dust and oil can be removed by flushing the ruled surface with laboratory grade ether and drying quickly with a jet of clean air.

These high-quality replicas were produced from precision-made, imported masters. The masters were made on an interferometrically-controlled ruling engine, which is the most modern and accurate method.

Basically, a replica grating consists of a series of closely-spaced lines impressed on the surface by the master. Because of the phenomena of diffraction and interference, these lines cause a dispersion of light according to wavelength. The result is a series of bright bands or spectra, each of which contains all visible wavelengths of the light source. These bands lie perpendicular to the grating lines.

Because of the regular distribution of the spectral bands and wavelengths in each band, replica gratings are extremely useful in spectrographic studies, such as determining the wavelengths of unknown color bands, analyzing the spectral characteristics of an unfamiliar light source and photographing spectra.

Fig. 1
Typical Light Paths

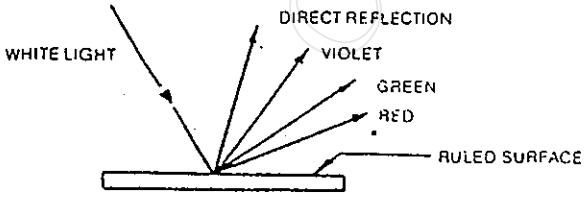
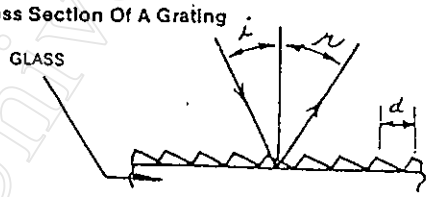


Figure 1 illustrates the dispersion effect of grating.

Fig. 2 Cross Section Of A Grating



If we could examine a grating in cross section we would see something like Figure 2. The normal is the line perpendicular to the face of the grating. All angles are measured from this line. "i" is the angle the incoming light makes with this line, "r" the angle of the reflected light. "d" is the distance between one ruled groove and the next. The dispersing action of the grating is determined by the following formula:

$$n\lambda = d(\sin i \pm \sin r)$$

where:

n = Order (explained below)

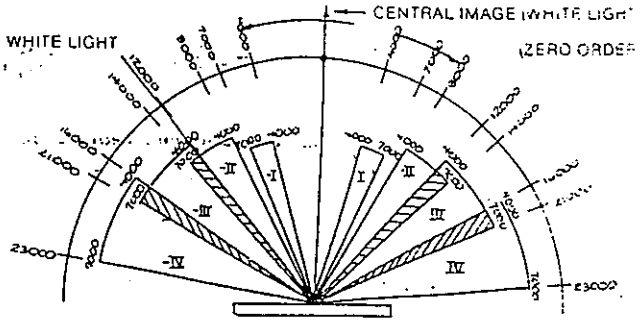
λ = Wavelength of light, measured in Angstroms units $1\ A = 10^{-10}$ meters $= 39.34 \times 10^{-9}$ inches

d = Spacing, as explained above, also in Angstroms

i = Angle of incidence

r = Angle of reflection and the minus sign is used where i and r are on opposite sides of the grating normal.

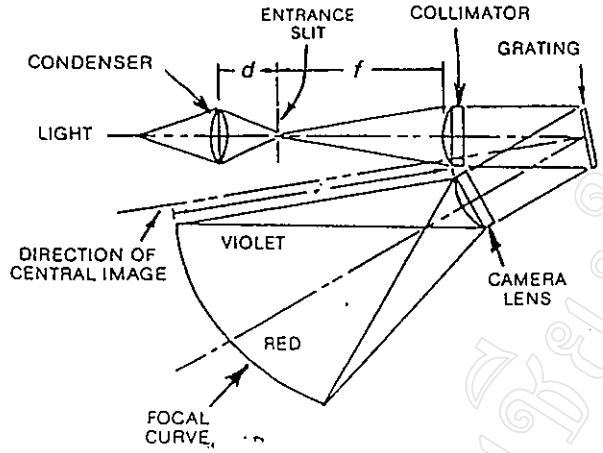
Fig. 3



711201-1
Rev. 8/81 500C

sensitivity also. Any source of light may be used in conjunction with a spectrograph; some of the more common ones are tungsten filament, metallic and carbon arcs, Mercury, Neon, Argon, etc. glow tubes, flames with various salts introduced into them, & the sun. Following are sketches of 2 common mountings and comments concerning their use.

Fig. 6

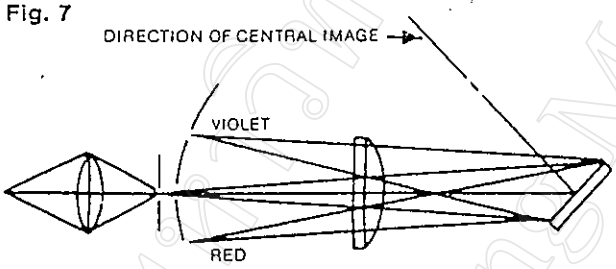


(1) Plane gratings:

The condenser of diameter "b" focuses the light on the slit. The collimator, and camera lens of focal length "f" and diameter "D", may be simple lenses or preferably achromats. "D" should be equal to the size of grating. See figure 6.

"b" should be at least $\frac{D}{f} \times a$.

Fig. 7



(2) Littrow

This is similar to (1) but uses. only one larger lens. The beam from the slit goes through a hole in the focal curve. Referred to as the Littrow Arrangement, see Figure 7.

It is strongly suggested that the interested experimenter consult the following references, as they give many more details than can be shown here:

1. Practical Spectroscopy, Harrison, Ford and Loofbourow. Prentice-Hall, New York, 1948. Good general spectrographic reference.
2. Experimental Spectroscopy, Sawyer, Prentice-Hall. Englewood Cliffs, New Jersey, 1951. Good treatment of mathematical design.
3. Experimental Physics, Strong, Prentice-Hall, Englewood Cliffs, New Jersey, 1938. Especially valuable for the general experimenter.

Advantages of reflection grating over transmission:
1. Less light loss by absorption.
2. Reflection grating can be blazed to put most of light at a given angle.
3. "Folded" layout can be used to reduce space.
4. Will transmit U.V.

Advantages of reflection grating over prism:
1. More speed per dollar.
2. More resolution per dollar.
3. Higher dispersion with a single grating (no need to use several as in prism systems) by using high orders and small grating spacings.

ภาคผนวกที่ 2

CCD Linear Image Sensor ILX511

SONY

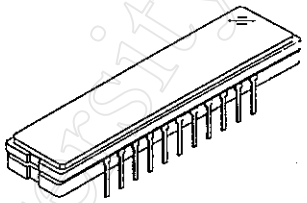
ILX511

2048-pixel CCD Linear Image Sensor (B/W)

Description

The ILX511 is a rectangular reduction type CCD linear image sensor designed for bar code POS hand scanner and optical measuring equipment use. A built-in timing generator and clock-drivers ensure single 5 V power supply for easy use.

22 pin DIP (Plastic)



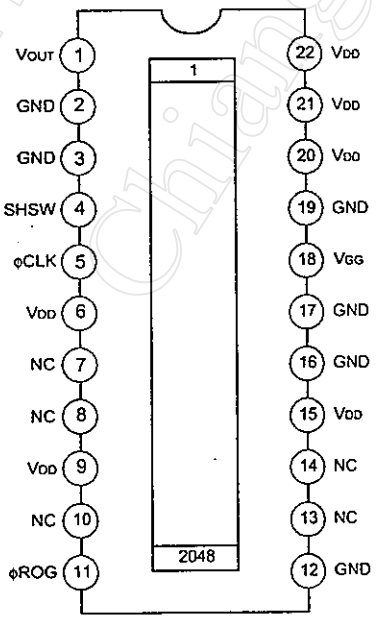
Features

- Number of effective pixels: 2048 pixels
- Pixel size: 14 µm × 200 µm (14 µm pitch)
- Single 5 V power supply
- Ultra-high sensitivity
- Built-in timing generator and clock-drivers
- Built-in sample-and-hold circuit
- Maximum clock frequency: 2MHz

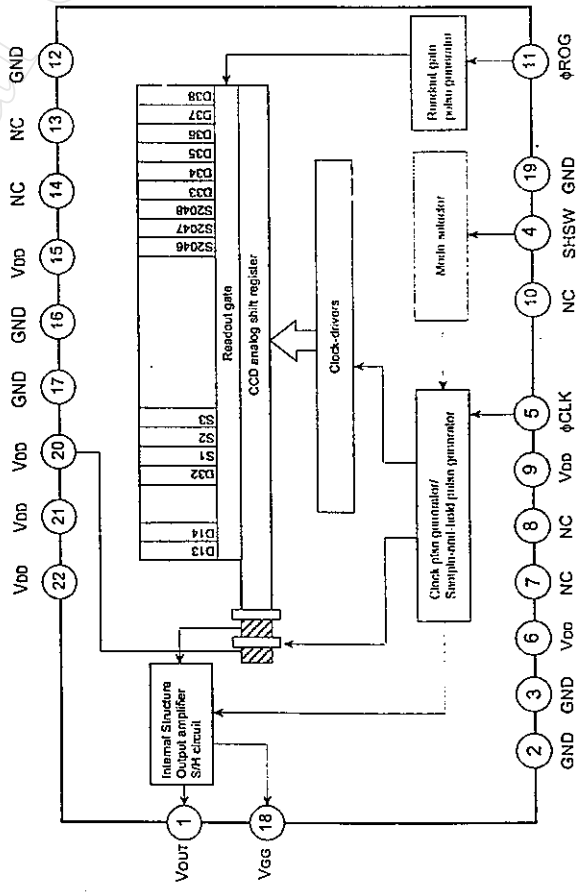
Absolute Maximum Ratings

• Supply voltage	V_{DD}	6	V
• Operating temperature		–10 to +60	°C
• Storage temperature		–30 to +80	°C

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin No.	Symbol	Description
1	V_{OUT}	Signal output
2	GND	GND
3	GND	GND
4	SHSW	Switch (with S/H or without S/H)
5	ϕCLK	Clock pulse input
6	V_{DD}	5V power supply
7	NC	NC
8	NC	NC
9	V_{DD}	5V power supply
10	NC	NC
11	ϕROG	Readout gate pulse input
12	GND	GND
13	NC	NC
14	NC	NC
15	V_{DD}	5V power supply
16	GND	GND
17	GND	GND
18	V_{GG}	Output circuit gate bias
19	GND	GND
20	V_{DD}	5V power supply
21	V_{DD}	5V power supply
22	V_{DD}	5V power supply

Mode Description

Mode in Use	Pin 4 (SHSW)
With S/H	GND
Without S/H	V_{DD}

Recommended Voltage

Item	Min.	Typ.	Max.	Unit
V_{DD}	4.5	5.0	5.5	V

Input Clock Voltage Condition (Note)

Item	Min.	Typ.	Max.	Unit
V_{IH}	4.5	5.0	5.5	V
V_{IL}	0	—	0.5	V

Note) This is applied to the all pulses applied externally. (ϕCLK, ϕROG)

Item	Symbol	Min.	Typ.	Max.	Unit
Input capacity of ϕCLK pin	$C_{\phi CLK}$	—	10	—	pF

Electro-optical Characteristics

(Ta = 25 °C, V_{DD} = 5 V, Clock frequency: 1 MHz, Light source = 3200 K, IR cut filter: CM-500S (t = 1.0 mm), Without S/H mode)

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Sensitivity 1	R1	150	200	250	V/(lx • s)	Note 1
Sensitivity 2	R2	—	1800	—	V/(lx • s)	Note 2
Sensitivity nonuniformity	PRNU	—	5.0	10.0	%	Note 3
Saturation output voltage	V_{SAT}	0.6	0.8	—	V	—
Dark voltage average	V_{DRK}	—	3.0	6.0	mV	Note 4
Dark signal nonuniformity	DSNU	—	6.0	12.0	mV	Note 4
Image lag	IL	—	1	—	%	Note 5
Dynamic range	DR	—	267	—	—	Note 6
Saturation exposure	SE	—	0.004	—	lx • s	Note 7
5 V current consumption	I_{VDD}	—	5.0	10.0	mA	—
Total transfer efficiency	TTE	92.0	98.0	—	%	—
Output impedance	Zo	—	250	—	Ω	—
Offset level	Vos	—	2.8	—	V	Note 8

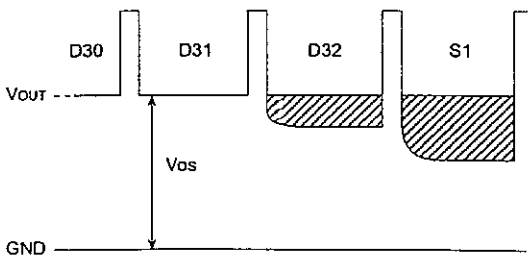
Note)

1. For the sensitivity test light is applied with a uniform intensity of illumination.
2. Light source: LED λ = 660nm
3. PRNU is defined as indicated below. Ray incidence conditions are the same as for Note 1.

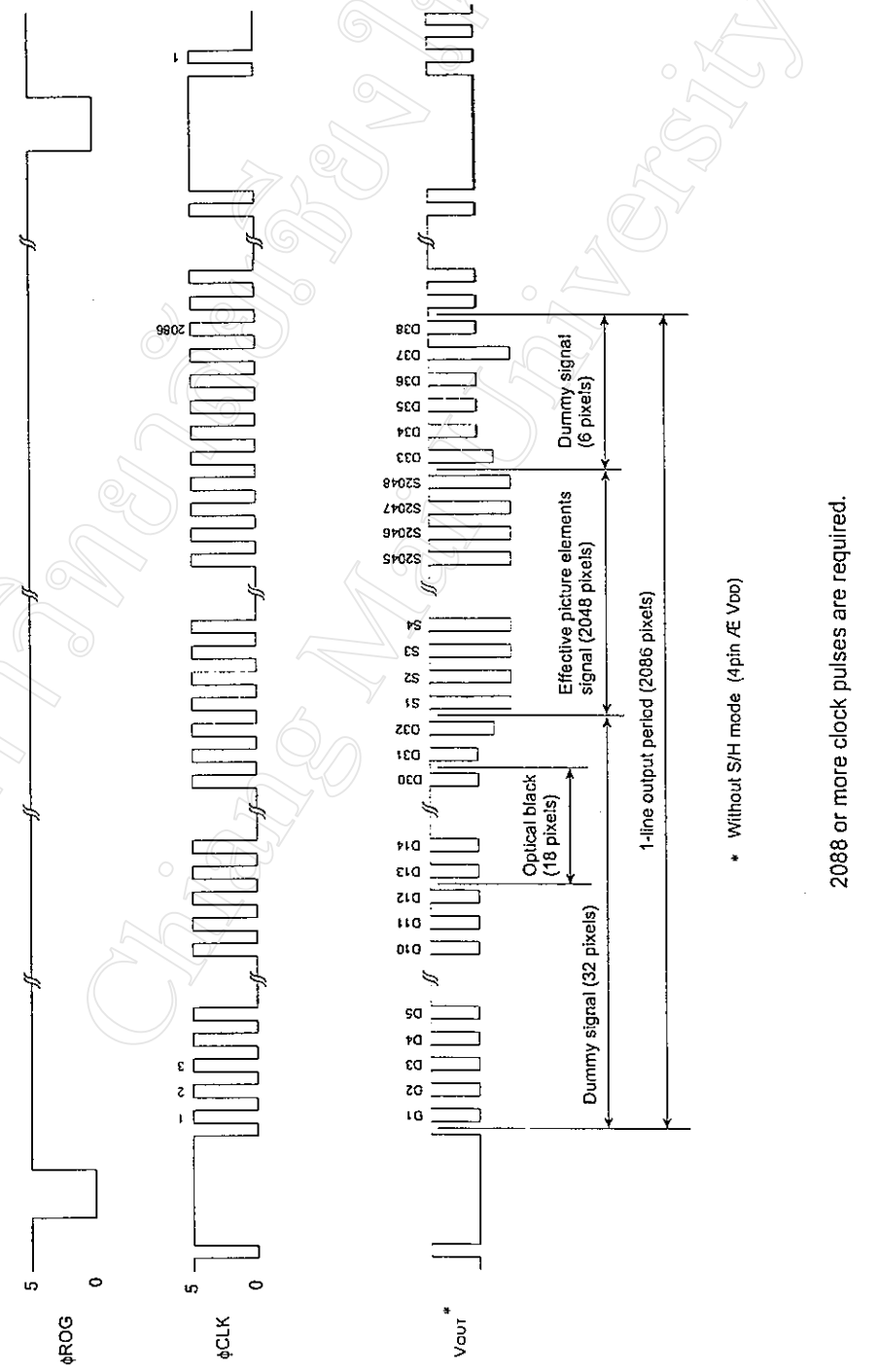
$$PRNU = \frac{(V_{MAX}-V_{MIN})/2}{V_{AVE}} \times 100\ (\%)$$

The maximum output of all the valid pixels is set to V_{MAX}, the minimum output to V_{MIN} and the average output to V_{AVE}.

4. Integration time is 10ms.
5. Typical value is used for clock pulse and readout pulse. V_{OUT} = 500 mV.
6. DR = V_{SAT}/V_{DRK}. When optical integration time is shorter, the dynamic range sets wider because dark voltage is in proportion to optical integration time.
7. SE = V_{SAT}/R1
8. Vos is defined as indicated below.



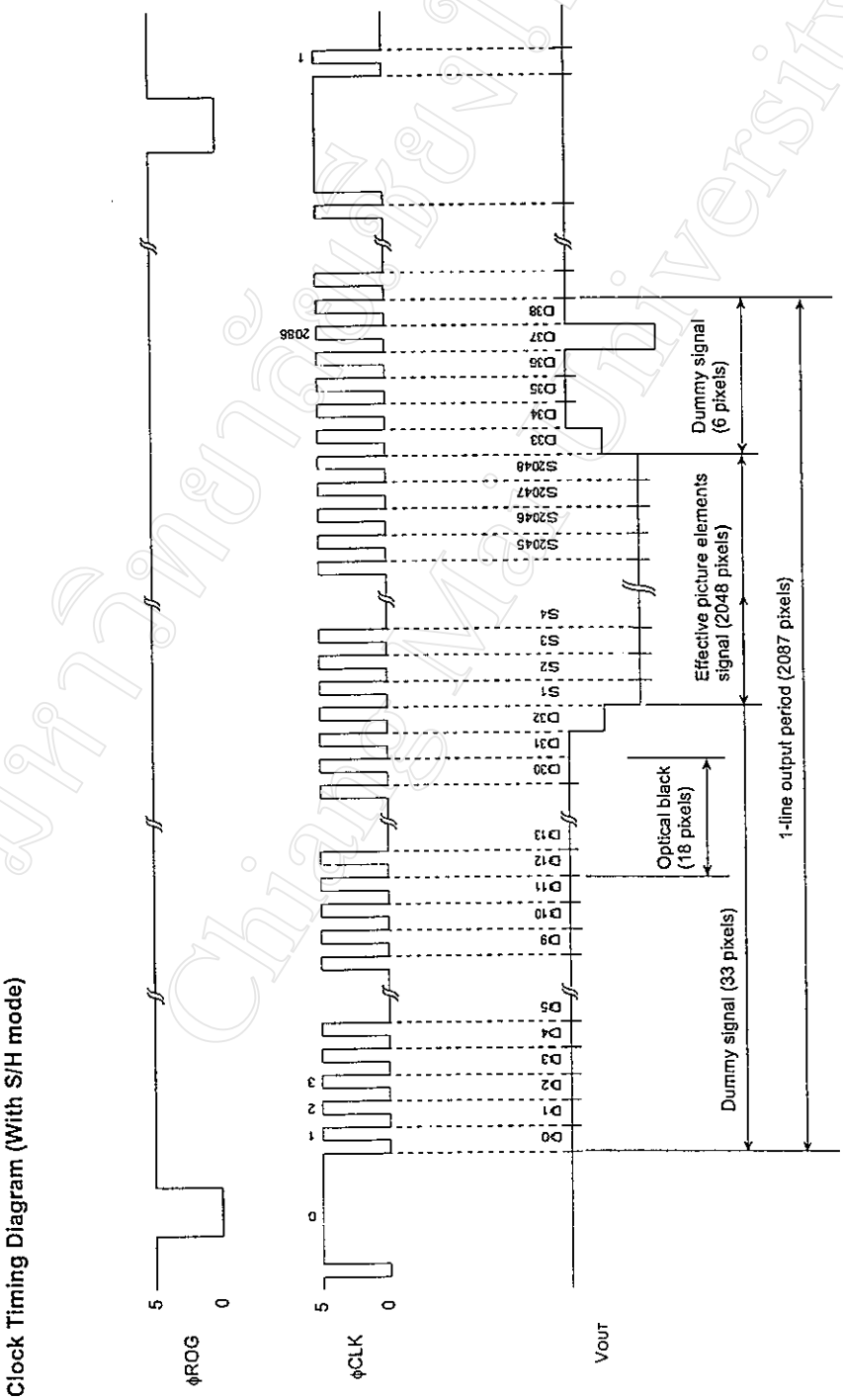
Clock Timing Diagram (Without S/H mode)



* Without S/H mode (4pin ÆVDD)

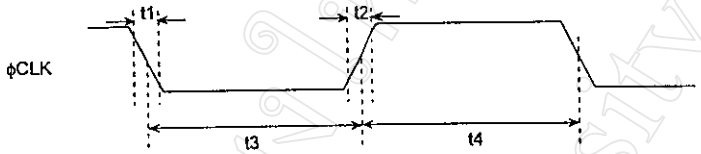
2088 or more clock pulses are required.

Clock Timing Diagram (With S/H mode)



2088 or more clock pulses are required.

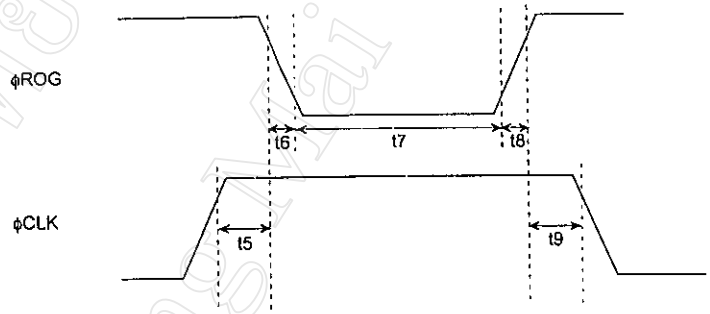
φCLK Timing (For all modes)



Item	Symbol	Min.	Typ.	Max.	Unit
φCLK pulse rise/fall time	t1, t2	0	10	100	ns
φCLK pulse duty (Note 1)	—	40	50	60	%

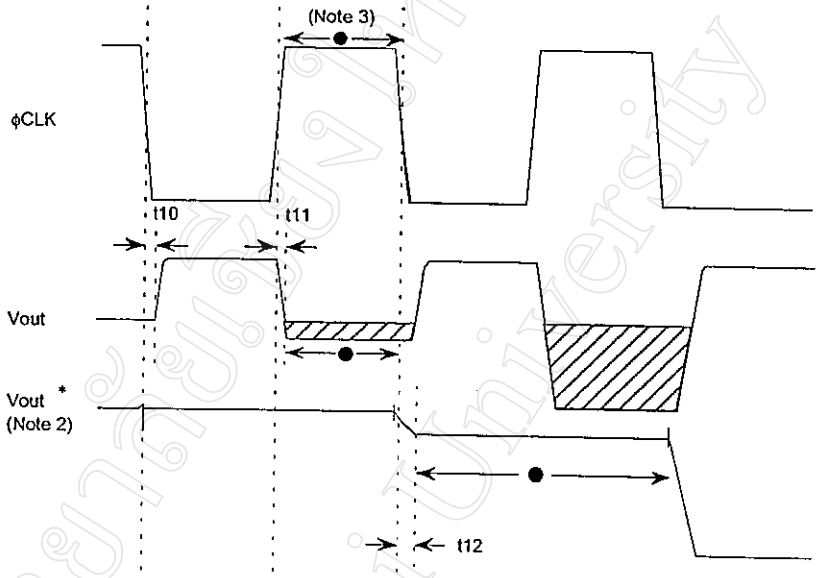
Note 1) 100 × t4 / (t3 + t4)

φROG, φCLK Timing



Item	Symbol	Min.	Typ.	Max.	Unit
φROG, φCLK pulse timing 1	t5	0	3000	—	ns
φROG, φCLK pulse timing 2	t9	1000	3000	—	
φROG pulse rise/fall time	t6, t8	0	10	—	
φROG pulse period	t7	3000	5000	—	

φCLK, VOUT Timing (Note 1)



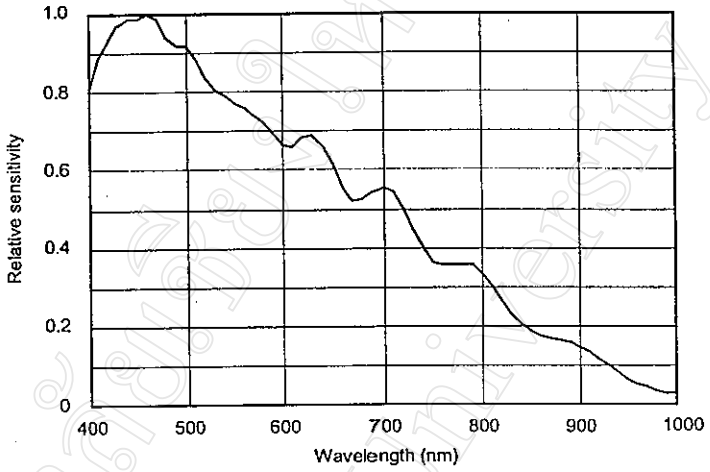
Item	Symbol	Min.	Typ.	Max.	Unit
φCLK-VOUT 1	t10	40	115	280	ns
φCLK-VOUT 2	t11	55	120	205	
φCLK-VOUT* (with S/H)	t12	10	165	240	

Note 1) fck = 1MHz, φCLK pulse duty = 50 %, φCLK pulse rise/fall time = 10 ns

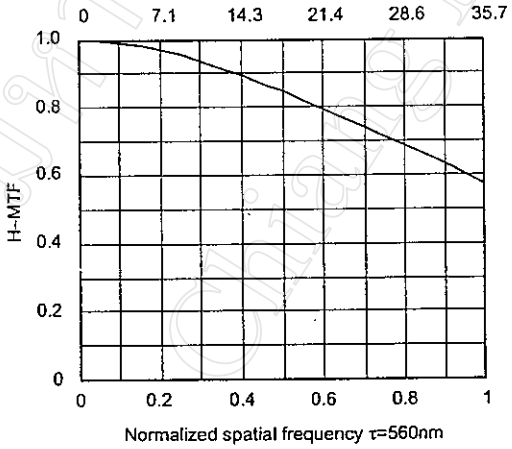
Note 2) Output waveform when internal S/H is in use.

Note 3) ● indicates the correspondence of clock pulse and data period.

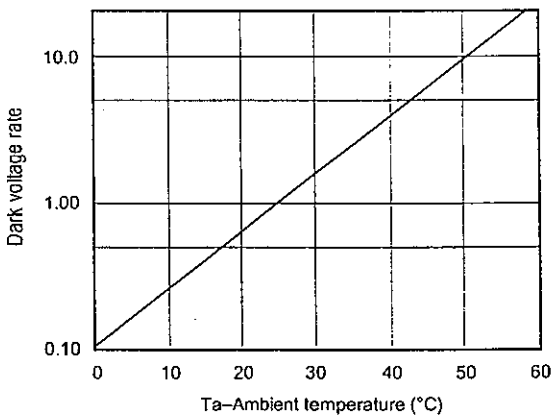
Spectral sensitivity (Typ.) (Ta = 25°C)



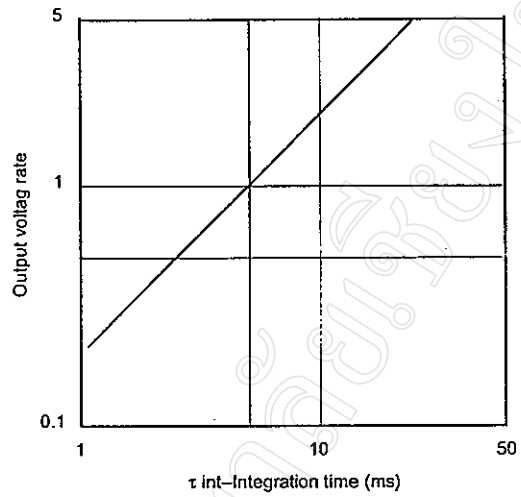
MTF of main scanning direction (Typ.)



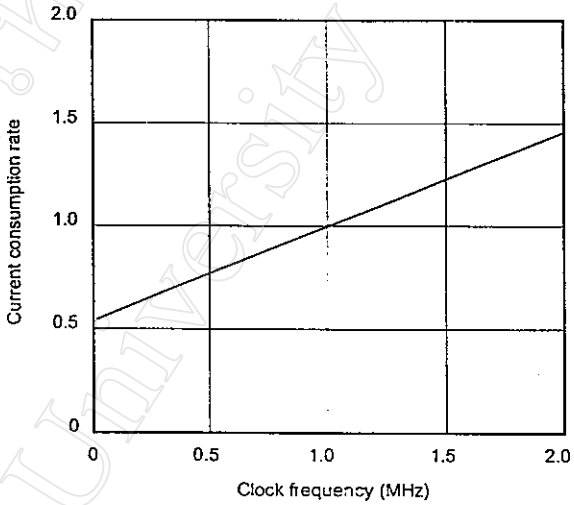
Dark voltage rate vs. Ambient temperature (Typ.)



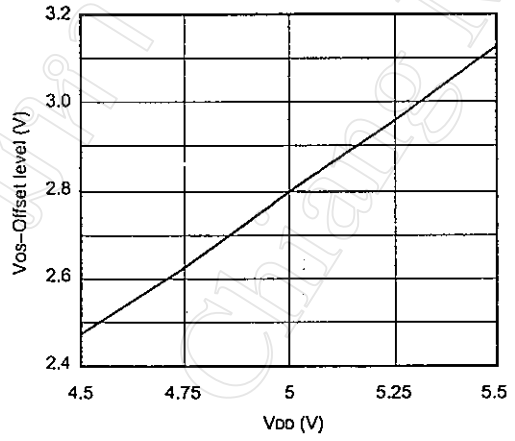
Output voltage rate vs. Integration time (Typ.)



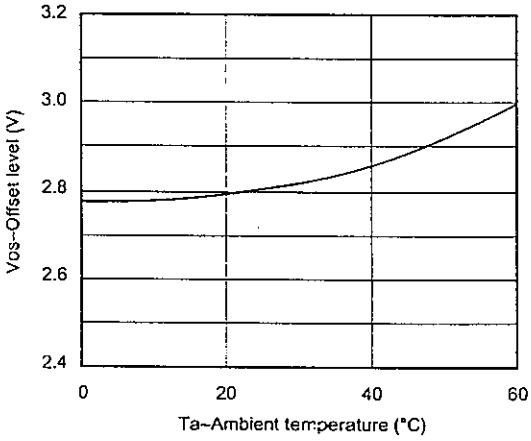
Current consumption rate vs. Clock frequency (Typ.)



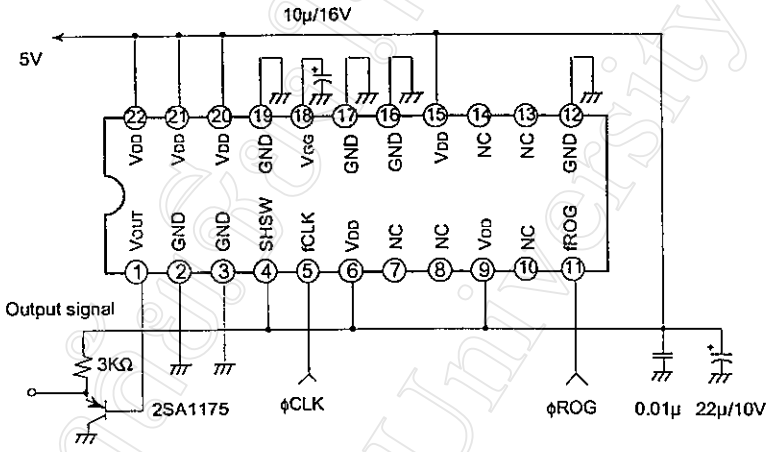
Offset level vs. VDD (Typ.)



Offset level vs. Ambient temperature (Typ.)



Application Circuit (Without S/H mode (Note))



Note) This circuit diagram is the case when internal S/H is not used.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Notes on Handling

1) Static charge prevention

CCD image sensors are easily damaged by static discharge. Before handling, be sure to take the following protective measures.

a) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.

b) When handling directly use an earth band.

c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.

d) Ionized air is recommended for discharge when handling CCD image sensors.

e) For the shipment of mounted substrates use cartons treated for the prevention of static charges.

2) Notes on handling CCD Cer-DIP package

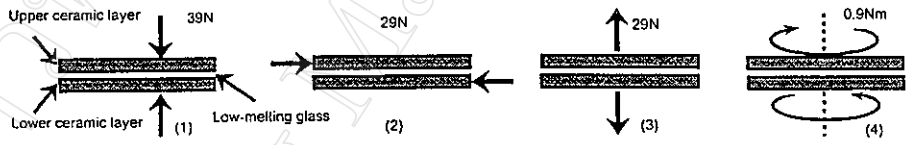
The following points should be observed when handling and installing this package.

a) (1) Compressive strength: 39N/surface
(Do not apply any load more than 0.7 mm inside the outer perimeter of the glass portion.)

(2) Shearing strength: 29N/surface

(3) Tensile strength: 29N/surface

(4) Torsional strength: 0.9Nm



b) In addition, if a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the ceramic portion. Therefore, for installation, either use an elastic load, such as a spring plate, or an adhesive.

c) Be aware that any of the following can cause the glass to crack because the upper and lower ceramic layers are shielded by low-melting glass.

(1) Applying repetitive bending stress to the external leads.

(2) Applying heat to the external leads for an extended period of time with a soldering iron.

(3) Rapid cooling or heating.

(4) Applying a load or impact to a limited portion of the low-melting glass with a small-tipped tool such as tweezers.

(5) Prying the upper or lower ceramic layers away at a support point of the low-melting glass.

Note that the preceding notes should also be observed when removing a component from a board after it has already been soldered.

3) Soldering

a) Make sure the package temperature does not exceed 80 °C.

b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.

c) To dismount image sensors, do not use a solder suction equipment. When using an electric desoldering tool, ground the controller. For the control system, use a zero cross type.

4) Dust and dirt protection
   a) Operate in clean environments.
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blower. (For dirt stuck through static electricity, ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

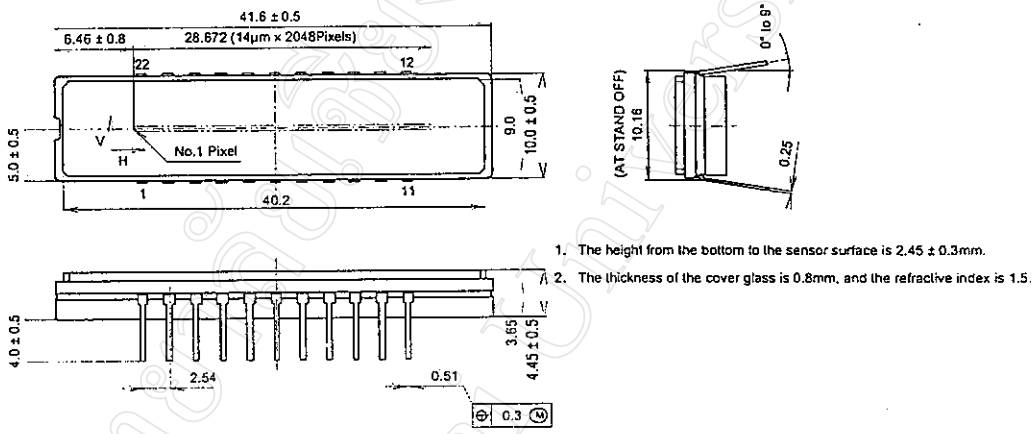
6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

7) Make sure the input pulse should not be -1 V or below.

8) Normal output signal is not obtained immediately after device switch on. Use the output signal added 22500 pulses or above to ϕ CLK clock pulse.

Package Outline Unit : mm

22pin DIP (400mil)



1. The height from the bottom to the sensor surface is 2.45 ± 0.3mm.
2. The thickness of the cover glass is 0.8mm, and the refractive index is 1.5.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Cer-DIP
LEAD TREATMENT	TIN PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g

ภาคผนวกที่ 3

Analog to Digital Converter ADC0820

National Semiconductor

February 1995

ADC0820 8-Bit High Speed μP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 μs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/μs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

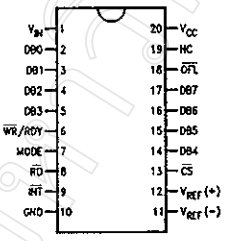
- Resolution 8 Bits
- Conversion Time 2.5 μs Max (RD Mode)
  1.5 μs Max (WR-RD Mode)
- Input signals with slew rate of 100 mV/μs converted without external sample-and-hold to 8 bits
- Low Power 75 mW Max
- Total Unadjusted Error ± ½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched TRI-STATE® output
- Logic inputs and outputs meet both MOS and T²L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

Connection and Functional Diagrams

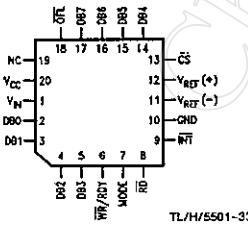
Dual-In-Line, Small Outline and SSOP Packages



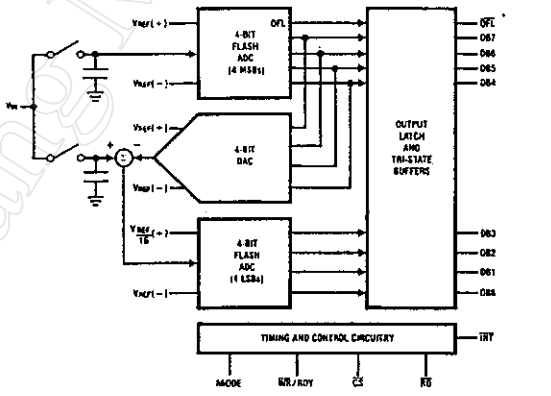
TL/H/5501–1

Top View

Molded Chip Carrier Package



TL/H/5501–33



TL/H/5501–2

FIGURE 1

See Ordering Information

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	10V
Logic Control Inputs	−0.2V to V_{CC} +0.2V
Voltage at Other Inputs and Output	−0.2V to V_{CC} +0.2V
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
Input Current at Any Pin (Note 5)	1 mA
Package Input Current (Note 5)	4 mA
ESD Susceptability (Note 9)	1200V
Lead Temp. (Soldering, 10 sec.)	
Dual-In-Line Package (plastic)	260°C
Dual-In-Line Package (ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0820CCJ	−40°C ≤ T_A ≤ +85°C
ADC0820CIWM	−40°C ≤ T_A ≤ +85°C
ADC0820BCN, ADC0820CCN	0°C ≤ T_A ≤ 70°C
ADC0820BCV, ADC0820CCV	0°C ≤ T_A ≤ 70°C
ADC0820BCWM, ADC0820CCWM	0°C ≤ T_A ≤ 70°C
ADC0820CCMSA	0°C ≤ T_A ≤ 70°C
V_{CC} Range	4.5V to 8V

Converter Characteristics

The following specifications apply for RD mode (pin 7 = 0), V_{CC} = 5V, $V_{REF}(+)$ = 5V, and $V_{REF}(-)$ = GND unless otherwise specified. **Boldface limits apply from T_{MIN} to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Parameter	Conditions	ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
		Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
Resolution			8			8	8	Bits
Total Unadjusted Error (Note 3)	ADC0820BCN, BCWM ADC0820CCJ ADC0820CCN, CCWM, CIWM, ADC0820CCMSA		±1			±½ ±1 ±1	±½ LSB ±1 ±1	LSB LSB LSB LSB
Minimum Reference Resistance		2.3	1.00		2.3	1.2		kΩ
Maximum Reference Resistance		2.3	6		2.3	5.3	6	kΩ
Maximum $V_{REF}(+)$ Input Voltage			V_{CC}			V_{CC}	V_{CC}	V
Minimum $V_{REF}(-)$ Input Voltage			GND			GND	GND	V
Minimum $V_{REF}(+)$ Input Voltage			$V_{REF}(-)$			$V_{REF}(-)$	$V_{REF}(-)$	V
Maximum $V_{REF}(-)$ Input Voltage			$V_{REF}(+)$			$V_{REF}(+)$	$V_{REF}(+)$	V
Maximum V_{IN} Input Voltage			V_{CC} + 0.1			V_{CC} + 0.1	V_{CC} + 0.1	V
Minimum V_{IN} Input Voltage			GND − 0.1			GND − 0.1	GND − 0.1	V
Maximum Analog Input Leakage Current	$\overline{CS} = V_{CC}$ $V_{IN} = V_{CC}$ V_{IN} = GND		3 −3			0.3 −0.3	3 −3	µA µA
Power Supply Sensitivity	V_{CC} = 5V ± 5%	±1/16	±¼		±1/16	±¼	±¼	LSB

DC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, unless otherwise specified. Boldface limits apply from T_{MIN} to T_{MAX}; all other limits $T_A=T_J=25°C$.

Parameter	Conditions		ADC0820CCJ			ADC0820BCN, ADC0820CCN ADC0820BCV, ADC0820CCV ADC0820BCWM, ADC0820CCWM ADC0820CCMSA, ADC0820CIWM			Limit Units
			Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	
$V_{IN(1)}$, Logical "1" Input Voltage	$V_{CC}=5.25V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		2.0			2.0	2.0	V
		Mode		3.5			3.5	3.5	V
$V_{IN(0)}$, Logical "0" Input Voltage	$V_{CC}=4.75V$	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$		0.8			0.8	0.8	V
		Mode		1.5			1.5	1.5	V
$I_{IN(1)}$, Logical "1" Input Current	$V_{IN(1)}=5V$; $\overline{CS}$, $\overline{RD}$		0.005	1		0.005		1	μA
	$V_{IN(1)}=5V$; $\overline{WR}$		0.1	3		0.1	0.3	3	μA
	$V_{IN(1)}=5V$; Mode		50	200		50	170	200	μA
$I_{IN(0)}$, Logical "0" Input Current	$V_{IN(0)}=0V$; $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, Mode		−0.005	−1		−0.005		−1	μA
$V_{OUT(1)}$, Logical "1" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=-360$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			2.4			2.8	2.4	V
	$V_{CC}=4.75V$, $I_{OUT}=-10$ μA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$			4.5			4.6	4.5	V
$V_{OUT(0)}$, Logical "0" Output Voltage	$V_{CC}=4.75V$, $I_{OUT}=1.6$ mA; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY			0.4			0.34	0.4	V
I_{OUT}, TRI-STATE Output Current	$V_{OUT}=5V$; DB0–DB7, RDY		0.1	3		0.1	0.3	3	μA
	$V_{OUT}=0V$; DB0–DB7, RDY		−0.1	−3		−0.1	−0.3	−3	μA
I_{SOURCE}, Output Source Current	$V_{OUT}=0V$; DB0–DB7, $\overline{OFL}$		−12	−6		−12	−7.2	−6	mA
	$\overline{INT}$		−9	−4.0		−9	−5.3	−4.0	mA
I_{SINK}, Output Sink Current	$V_{OUT}=5V$; DB0–DB7, $\overline{OFL}$, $\overline{INT}$, RDY		14	7		14	8.4	7	mA
I_{CC}, Supply Current	$\overline{CS}=\overline{WR}=\overline{RD}=0$		7.5	15		7.5	13	15	mA

AC Electrical Characteristics

The following specifications apply for $V_{CC}=5V$, $t_r=t_f=20$ ns, $V_{REF}(+)=5V$, $V_{REF}(-)=0V$ and $T_A=25°C$ unless otherwise specified.

Parameter		Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_{CRD}, Conversion Time for RD Mode		Pin 7 = 0, *(Figure 2)*	1.6		2.5	μs
t_{ACC0}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = 0, *(Figure 2)*	$t_{CRD}+20$		$t_{CRD}+50$	ns
t_{CWR-RD}, Conversion Time for WR-RD Mode		Pin 7 = V_{CC}; t_{WR} = 600 ns, $t_{RD}=600$ ns; *(Figures 3a and 3b)*			1.52	μs
t_{WR}, Write Time	Min	Pin 7 = V_{CC}; *(Figures 3a and 3b)*		600		ns
	Max	(Note 4) See Graph	50			μs
t_{RD}, Read Time	Min	Pin 7 = V_{CC}; *(Figures 3a and 3b)* (Note 4) See Graph		600		ns
t_{ACC1}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}<t_l$; *(Figure 3a)* $C_L=15$ pF	190		280	ns
		$C_L=100$ pF	210		320	ns
t_{ACC2}, Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Valid)		Pin 7 = V_{CC}, $t_{RD}>t_l$; *(Figure 3b)* $C_L=15$ pF	70		120	ns
		$C_L=100$ pF	90		150	ns
t_{ACC3}, Access Time (Delay from Rising Edge of RDY to Output Valid)		R_{PULLUP} = 1k and C_L = 15 pF	30			ns

AC Electrical Characteristics (Continued) The following specifications apply for $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $V_{REF}(+) = 5V$, $V_{REF}(-) = 0V$ and $T_A = 25°C$ unless otherwise specified.

Parameter	Conditions	Typ (Note 6)	Tested Limit (Note 7)	Design Limit (Note 8)	Units
t_I, Internal Comparison Time	Pin 7 = V_{CC}; *(Figures 3b and 4)* $C_L = 50$ pF	800		1300	ns
t_{1H}, t_{0H}, TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$R_L = 1k$, $C_L = 10$ pF	100		200	ns
$t_{\overline{INT}L}$, Delay from Rising Edge of $\overline{WR}$ to Falling Edge of $\overline{INT}$	Pin 7 = V_{CC}, $C_L = 50$ pF $t_{RD} > t_I$; *(Figure 3b)* $t_{RD} < t_I$; *(Figure 3a)*	 $t_{RD} + 200$		 t_I $t_{RD} + 290$	 ns ns
$t_{\overline{INT}H}$, Delay from Rising Edge of $\overline{RD}$ to Rising Edge of $\overline{INT}$	*(Figures 2, 3a and 3b)* $C_L = 50$ pF	125		225	ns
$t_{\overline{INT}HWR}$, Delay from Rising Edge of $\overline{WR}$ to Rising Edge of $\overline{INT}$	*(Figure 4)*, $C_L = 50$ pF	175		270	ns
t_{RDY}, Delay from $\overline{CS}$ to RDY	*(Figure 2)*, $C_L = 50$ pF, Pin 7 = 0	50		100	ns
t_{ID}, Delay from $\overline{INT}$ to Output Valid	*(Figure 4)*	20		50	ns
t_{RI}, Delay from $\overline{RD}$ to $\overline{INT}$	Pin 7 = V_{CC}, $t_{RD} < t_I$ *(Figure 3a)*	200		290	ns
t_P, Delay from End of Conversion to Next Conversion	*(Figures 2, 3a, 3b and 4)* (Note 4) See Graph			500	ns
Slew Rate, Tracking		0.1			V/μs
C_{VIN}, Analog Input Capacitance		45			pF
C_{OUT}, Logic Output Capacitance		5			pF
C_{IN}, Logic Input Capacitance		5			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: All voltages are measured with respect to the GND pin, unless otherwise specified.

Note 3: Total unadjusted error includes offset, full-scale, and linearity errors.

Note 4: Accuracy may degrade if t_{WR} or t_{RD} is shorter than the minimum value specified. See Accuracy vs t_{WR} and Accuracy vs t_{RD} graphs.

Note 5: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 1 mA or less. The 4 mA package input current limits the number of pins that can exceed the power supply boundaries with a 1 mA current limit to four.

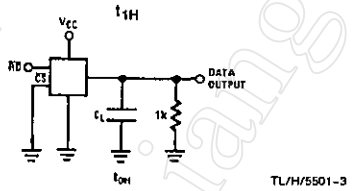
Note 6: Typicals are at 25°C and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

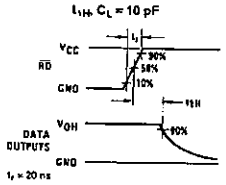
Note 8: Design limits are guaranteed but not 100% tested. These limits are not used to calculate outgoing quality levels.

Note 9: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

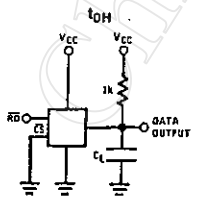
TRI-STATE Test Circuits and Waveforms



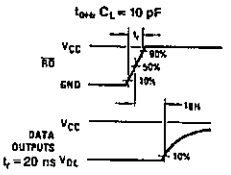
TL/H/5501–3



TL/H/5501–4

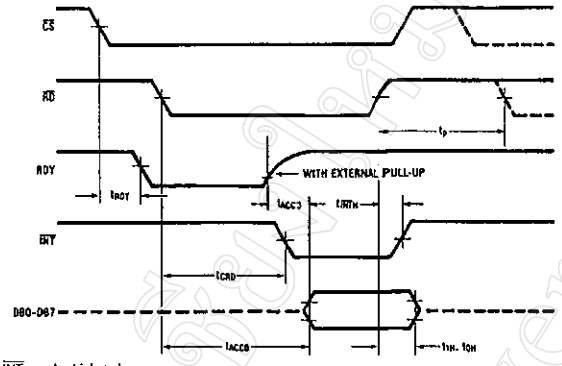


TL/H/5501–5



TL/H/5501–6

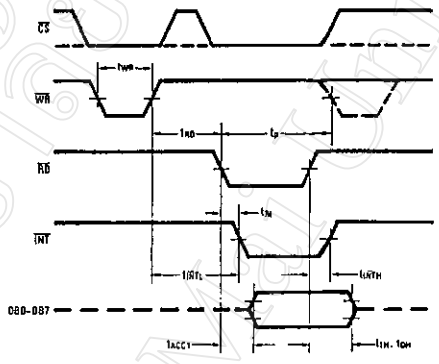
Timing Diagrams



Note: On power-up the state of $\overline{INT}$ can be high or low.

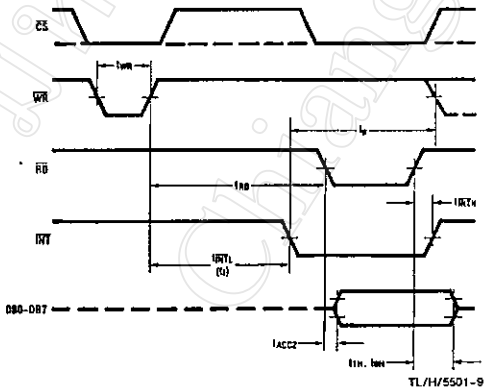
TL/H/5501-7

FIGURE 2. RD Mode (Pin 7 is Low)



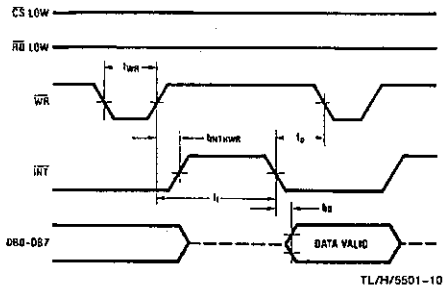
TL/H/5501-8

FIGURE 3a. WR-RD Mode (Pin 7 is High and $t_{RD} < t_I$)



TL/H/5501-9

FIGURE 3b. WR-RD Mode (Pin 7 is High and $t_{RD} > t_I$)

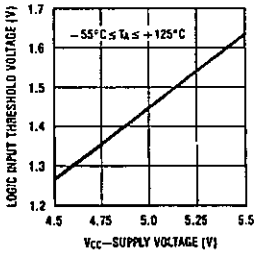


TL/H/5501-10

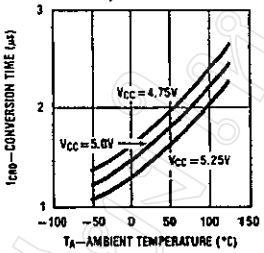
FIGURE 4. WR-RD Mode (Pin 7 is High)
Stand-Alone Operation

Typical Performance Characteristics

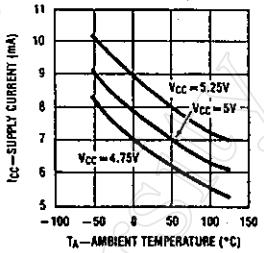
Logic Input Threshold Voltage vs Supply Voltage



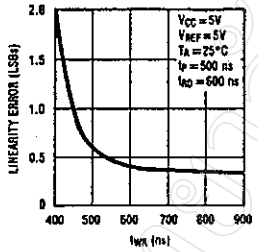
Conversion Time (RD Mode) vs Temperature



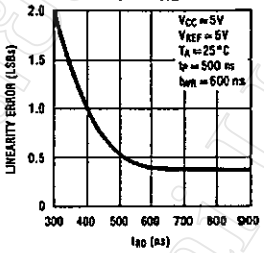
Power Supply Current vs Temperature (not including reference ladder)



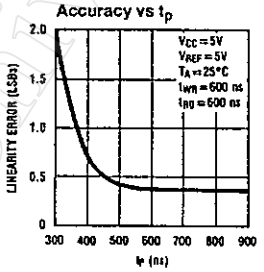
Accuracy vs t_{WR}



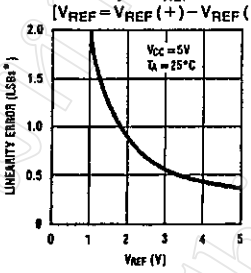
Accuracy vs t_{RD}



Accuracy vs t_P

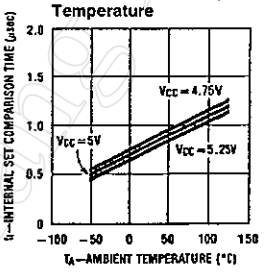


Accuracy vs V_{REF}
[$V_{REF} = V_{REF}(+) - V_{REF}(-)$]

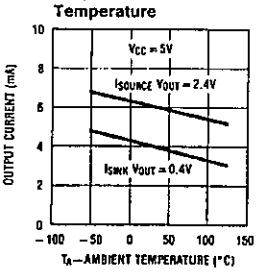


*1 LSB = $\frac{V_{REF}}{256}$

t_I, Internal Time Delay vs Temperature



Output Current vs Temperature



TL/H/5501–11

Description of Pin Functions

Pin	Name	Function
1	V_{IN}	Analog input; range $=GND \le V_{IN} \le V_{CC}$
2	DB0	TRI-STATE data output—bit 0 (LSB)
3	DB1	TRI-STATE data output—bit 1
4	DB2	TRI-STATE data output—bit 2
5	DB3	TRI-STATE data output—bit 3
6	$\overline{WR}$/RDY	**WR-RD Mode** **$\overline{WR}$:** With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. Approximately 800 ns (the preset internal time out, t_i) after the $\overline{WR}$ rising edge, the result of the conversion will be strobed into the output latch, provided that $\overline{RD}$ does not occur prior to this time out (see *Figures 3a* and *3b*). **RD Mode** **RDY:** This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$; RDY will go TRI-STATE when the result of the conversion is strobed into the output latch. It is used to simplify the interface to a microprocessor system (see *Figure 2*).
7	Mode	**Mode:** Mode selection input—it is internally tied to GND through a 50 μA current source. **RD Mode:** When mode is low **WR-RD Mode:** When mode is high
8	$\overline{RD}$	**WR-RD Mode** With $\overline{CS}$ low, the TRI-STATE data outputs (DB0-DB7) will be activated when $\overline{RD}$ goes low (see *Figure 4*). $\overline{RD}$ can also be used to increase the speed of the converter by reading data prior to the preset internal time out (t_i, ~800 ns). If this is done, the data result transferred to output latch is latched after the falling edge of the $\overline{RD}$ (see *Figures 3a* and *3b*). **RD Mode** With $\overline{CS}$ low, the conversion will start with $\overline{RD}$ going low, also $\overline{RD}$ will enable the TRI-STATE data outputs at the completion of the conversion. RDY going TRI-STATE and $\overline{INT}$ going low indicates the completion of the conversion (see *Figure 2*).
9	$\overline{INT}$	**WR-RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ will go low, ~800 ns (the preset internal time out, t_i) after the rising edge of $\overline{WR}$ (see *Figure 3b*); or $\overline{INT}$ will go low after the falling edge of $\overline{RD}$, if $\overline{RD}$ goes low prior to the 800 ns time out (see *Figure 3a*). $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figures 3a* and *3b*). **RD Mode** $\overline{INT}$ going low indicates that the conversion is completed and the data result is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$ or $\overline{CS}$ (see *Figure 2*).
10	GND	Ground
11	$V_{REF}(-)$	The bottom of resistor ladder, voltage range: $GND \le V_{REF}(-) \le V_{REF}(+)$ (Note 5)
12	$V_{REF}(+)$	The top of resistor ladder, voltage range: $V_{REF}(-) \le V_{REF}(+) \le V_{CC}$ (Note 5)
13	$\overline{CS}$	$\overline{CS}$ must be low in order for the $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	TRI-STATE data output—bit 4
15	DB5	TRI-STATE data output—bit 5
16	DB6	TRI-STATE data output—bit 6
17	DB7	TRI-STATE data output—bit 7 (MSB)
18	$\overline{OFL}$	Overflow output—If the analog input is higher than the $V_{REF}(+)$, $\overline{OFL}$ will be low at the end of conversion. It can be used to cascade 2 or more devices to have more resolution (9, 10-bit). This output is always active and does not go into TRI-STATE as DB0–DB7 do.
19	NC	No connection
20	V_{CC}	Power supply voltage

1.0 Functional Description

1.1 GENERAL OPERATION

The ADC0820 uses two 4-bit flash A/D converters to make an 8-bit measurement (*Figure 1*). Each flash ADC is made up of 15 comparators which compare the unknown input to a reference ladder to get a 4-bit result. To take a full 8-bit reading, one flash conversion is done to provide the 4 most significant data bits (via the MS flash ADC). Driven by the 4 MSBs, an internal DAC recreates an analog approximation of the input voltage. This analog signal is then subtracted from the input, and the difference voltage is converted by a second 4-bit flash ADC (the LS ADC), providing the 4 least significant bits of the output data word.

The internal DAC is actually a subsection of the MS flash converter. This is accomplished by using the same resistor ladder for the A/D as well as for generating the DAC signal. The DAC output is actually the tap on the resistor ladder which most closely approximates the analog input. In addition, the "sampled-data" comparators used in the ADC0820 provide the ability to compare the magnitudes of several analog signals simultaneously, without using input summing amplifiers. This is especially useful in the LS flash ADC, where the signal to be converted is an analog difference.

1.0 Functional Description (Continued)

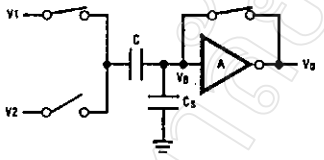
1.2 THE SAMPLED-DATA COMPARATOR

Each comparator in the ADC0820 consists of a CMOS inverter with a capacitively coupled input (*Figure 5*). Analog switches connect the two comparator inputs to the input capacitor (C) and also connect the inverter's input and output. This device in effect now has one differential input pair. A comparison requires two cycles, one for zeroing the comparator, and another for making the comparison.

In the first cycle, one input switch and the inverter's feedback switch (*Figure 5a*) are closed. In this interval, C is charged to the connected input (V1) less the inverter's bias voltage (V_B, approximately 1.2V). In the second cycle (*Figure 5b*), these two switches are opened and the other (V2) input's switch is closed. The input capacitor now subtracts its stored voltage from the second input and the difference is amplified by the inverter's open loop gain. The inverter's input (V_B') becomes

$$V_B - (V1 - V2)\frac{C}{C + C_S}$$

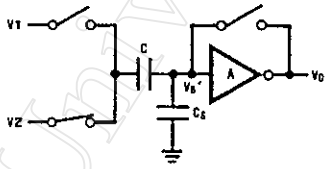
and the output will go high or low depending on the sign of $V_B' - V_B$.



TL/H/5501–12

- $V_O = V_B$
- V on C = $V1 - V_B$
- C_S = stray input node capacitor
- V_B = inverter input bias voltage

FIGURE 5a. Zeroing Phase



TL/H/5501–13

- $V_B' - V_B = (V2 - V1)\frac{C}{C + C_S}$
- $V_O' = \frac{-A}{C + C_S}[CV2 - CV1]$
- V_O' is dependent on V2 − V1

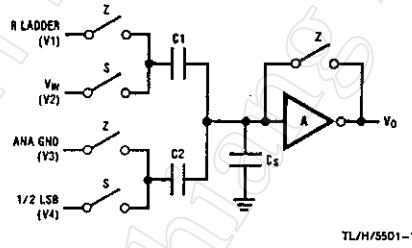
FIGURE 5b. Compare Phase

FIGURE 5. Sampled-Data Comparator

The actual circuitry used in the ADC0820 is a simple but important expansion of the basic comparator described above. By adding a second capacitor and another set of switches to the input (*Figure 6*), the scheme can be expanded to make dual differential comparisons. In this circuit, the feedback switch and one input switch on each capacitor (Z switches) are closed in the zeroing cycle. A comparison is then made by connecting the second input on each capacitor and opening all of the other switches (S switches). The change in voltage at the inverter's input, as a result of the change in charge on each input capacitor, will now depend on both input signal differences.

1.3 ARCHITECTURE

In the ADC0820, one bank of 15 comparators is used in each 4-bit flash A/D converter (*Figure 7*). The MS (most significant) flash ADC also has one additional comparator to detect input overrange. These two sets of comparators operate alternately, with one group in its zeroing cycle while the other is comparing.



TL/H/5501–14

$$V_O = \frac{-A}{C1 + C2 + C_S}\{C1(V2 - V1) + C2(V4 - V3)\}$$

$$= \frac{-A}{C1 + C2 + C_S}[\Delta Q_{C1} + \Delta Q_{C2}]$$

FIGURE 6. ADC0820 Comparator (from MS Flash ADC)

Detailed Block Diagram

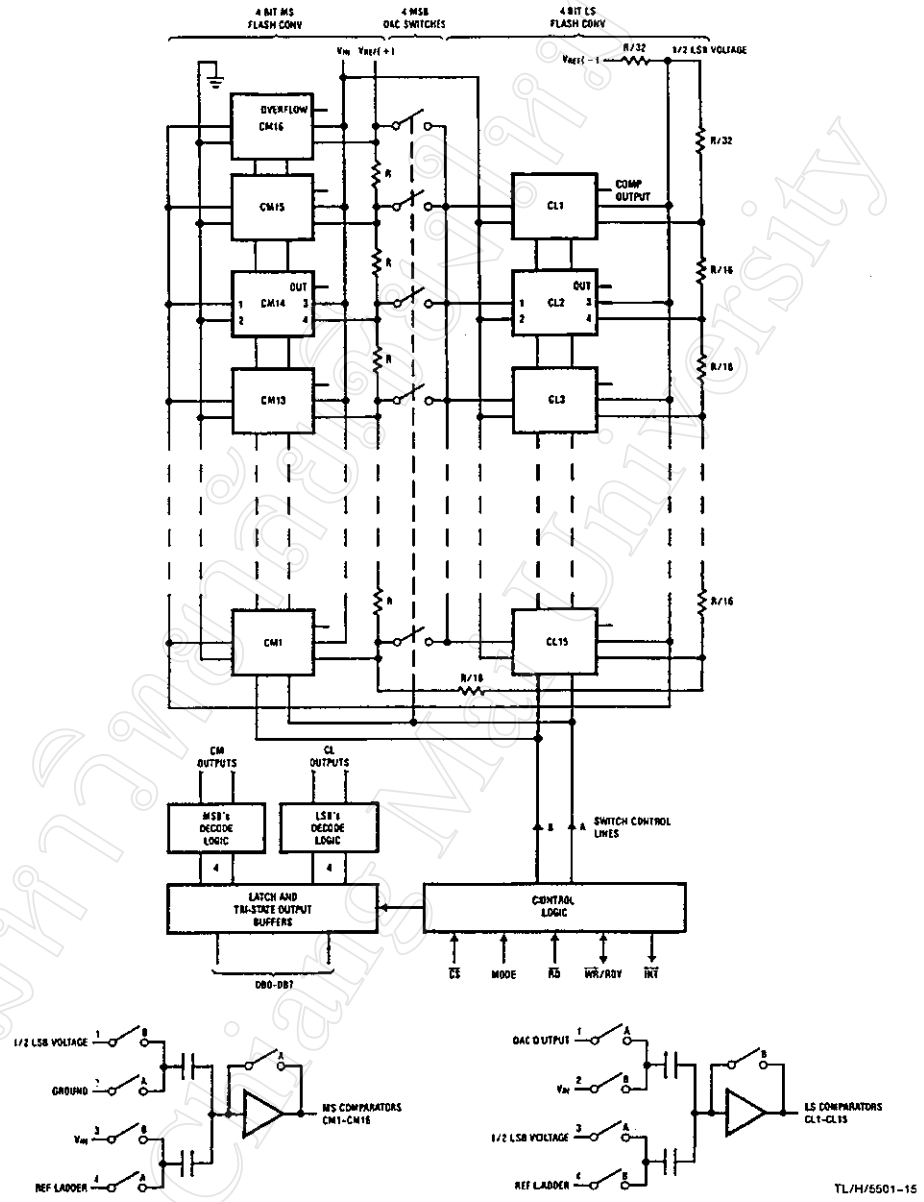


FIGURE 7

1.0 Functional Description (Continued)

When a typical conversion is started, the $\overline{WR}$ line is brought low. At this instant the MS comparators go from zeroing to comparison mode (*Figure B*). When $\overline{WR}$ is returned high after at least 600 ns, the output from the first set of comparators (the first flash) is decoded and latched. At this point the two 4-bit converters change modes and the LS (least significant) flash ADC enters its compare cycle. No less than 600 ns later, the $\overline{RD}$ line may be pulled low to latch the lower 4 data bits and finish the 8-bit conversion. When $\overline{RD}$ goes low, the flash A/Ds change state once again in preparation for the next conversion.

Figure B also outlines how the converter's interface timing relates to its analog input (V_{IN}). In WR-RD mode, V_{IN} is measured while $\overline{WR}$ is low. In RD mode, sampling occurs during the first 800 ns of $\overline{RD}$. Because of the input connections to the ADC0820's LS and MS comparators, the converter has the ability to sample V_{IN} at one instant (Section 2.4), despite the fact that two separate 4-bit conversions are being done. More specifically, when $\overline{WR}$ is low the MS flash is in compare mode (connected to V_{IN}), and the LS flash is in zero mode (also connected to V_{IN}). Therefore both flash ADCs sample V_{IN} at the same time.

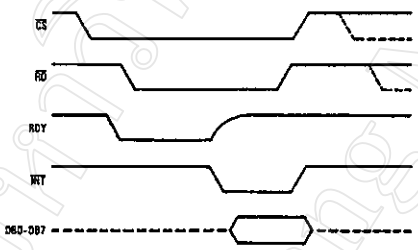
1.4 DIGITAL INTERFACE

The ADC0820 has two basic interface modes which are selected by strapping the MODE pin high or low.

RD Mode

With the MODE pin grounded, the converter is set to Read mode. In this configuration, a complete conversion is done by pulling $\overline{RD}$ low until output data appears. An $\overline{INT}$ line is provided which goes low at the end of the conversion as well as a RDY output which can be used to signal a processor that the converter is busy or can also serve as a system Transfer Acknowledge signal.

RD Mode (Pin 7 Is Low)

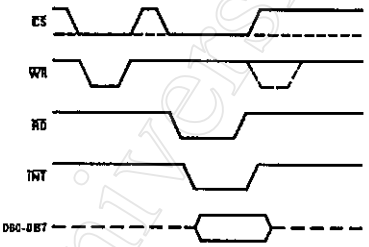


TL/H/5501–16

When in RD mode, the comparator phases are internally triggered. At the falling edge of $\overline{RD}$, the MS flash converter goes from zero to compare mode and the LS ADC's comparators enter their zero cycle. After 800 ns, data from the MS flash is latched and the LS flash ADC enters compare mode. Following another 800 ns, the lower 4 bits are recovered.

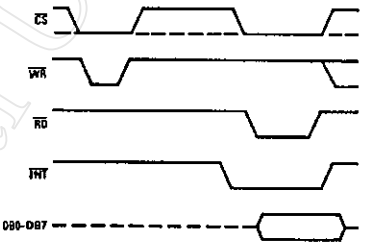
WR then RD Mode

With the MODE pin tied high, the A/D will be set up for the WR-RD mode. Here, a conversion is started with the $\overline{WR}$ input; however, there are two options for reading the output data which relate to interface timing. If an interrupt driven scheme is desired, the user can wait for $\overline{INT}$ to go low before reading the conversion result (*Figure B*). $\overline{INT}$ will typically go low 800 ns after $\overline{WR}$'s rising edge. However, if a shorter conversion time is desired, the processor need not wait for $\overline{INT}$ and can exercise a read after only 600 ns (*Figure A*). If this is done, $\overline{INT}$ will immediately go low and data will appear at the outputs.



TL/H/5501–17

FIGURE A. WR-RD Mode (Pin 7 Is High and $t_{RD} < t_i$)



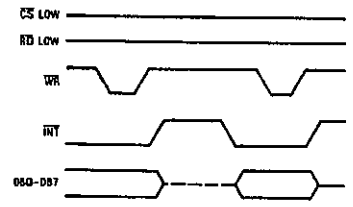
TL/H/5501–18

FIGURE B. WR-RD Mode (Pin 7 Is High and $t_{RD} > t_i$)

Stand-Alone

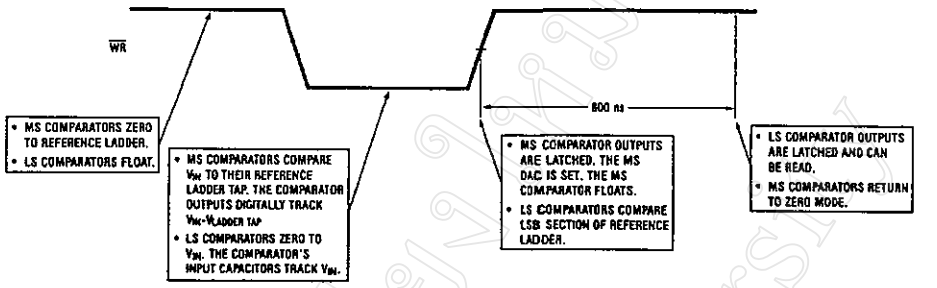
For stand-alone operation in WR-RD mode, $\overline{CS}$ and $\overline{RD}$ can be tied low and a conversion can be started with $\overline{WR}$. Data will be valid approximately 800 ns following $\overline{WR}$'s rising edge.

WR-RD Mode (Pin 7 Is High) Stand-Alone Operation



TL/H/5501–19

1.0 Functional Description (Continued)



TL/H/5501–20

Note: MS means most significant
LS means least significant

FIGURE 8. Operating Sequence (WR-RD Mode)

OTHER INTERFACE CONSIDERATIONS

In order to maintain conversion accuracy, $\overline{WR}$ has a maximum width spec of 50 μs. When the MS flash ADC's sampled-data comparators (Section 1.2) are in comparison mode ($\overline{WR}$ is low), the input capacitors (C, *Figure 6*) must hold their charge. Switch leakage and inverter bias current can cause errors if the comparator is left in this phase for too long.

Since the MS flash ADC enters its zeroing phase at the end of a conversion (Section 1.3), a new conversion cannot be started until this phase is complete. The minimum spec for this time (t_P, *Figures 2, 3a, 3b,* and *4*) is 500 ns.

2.0 Analog Considerations

2.1 REFERENCE AND INPUT

The two V_{REF} inputs of the ADC0820 are fully differential and define the zero to full-scale input range of the A to D converter. This allows the designer to easily vary the span of the analog input since this range will be equivalent to the voltage difference between $V_{IN}(+)$ and $V_{IN}(-)$. By reducing V_{REF}($V_{REF} = V_{REF}(+) - V_{REF}(-)$) to less than 5V, the sensitivity of the converter can be increased (i.e., if $V_{REF} = 2V$ then 1 LSB = 7.8 mV). The input/reference arrangement also facilitates ratiometric operation and in many cases the chip power supply can be used for transducer power as well as the V_{REF} source.

This reference flexibility lets the input span not only be varied but also offset from zero. The voltage at $V_{REF}(-)$ sets the input level which produces a digital output of all zeroes. Though V_{IN} is not itself differential, the reference design affords nearly differential-input capability for most measurement applications. *Figure 9* shows some of the configurations that are possible.

2.2 INPUT CURRENT

Due to the unique conversion techniques employed by the ADC0820, the analog input behaves somewhat differently than in conventional devices. The A/D's sampled-data comparators take varying amounts of input current depending on which cycle the conversion is in.

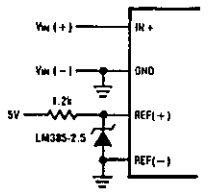
The equivalent input circuit of the ADC0820 is shown in *Figure 10a*. When a conversion starts ($\overline{WR}$ low, WR-RD mode), all input switches close, connecting V_{IN} to thirty-one 1 pF capacitors. Although the two 4-bit flash circuits are not both in their compare cycle at the same time, V_{IN} still sees all input capacitors at once. This is because the MS flash converter is connected to the input during its compare interval and the LS flash is connected to the input during its zeroing phase (Section 1.3). In other words, the LS ADC uses V_{IN} as its zero-phase input.

The input capacitors must charge to the input voltage through the on resistance of the analog switches (about 5 kΩ to 10 kΩ). In addition, about 12 pF of input stray capacitance must also be charged. For large source resistances, the analog input can be modeled as an RC network as shown in *Figure 10b*. As R_S increases, it will take longer for the input capacitance to charge.

In RD mode, the input switches are closed for approximately 800 ns at the start of the conversion. In WR-RD mode, the time that the switches are closed to allow this charging is the time that $\overline{WR}$ is low. Since other factors force this time to be at least 600 ns, input time constants of 100 ns can be accommodated without special consideration. Typical total input capacitance values of 45 pF allow R_S to be 1.5 kΩ without lengthening $\overline{WR}$ to give V_{IN} more time to settle.

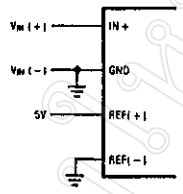
2.0 Analog Considerations (Continued)

External Reference 2.5V Full-Scale



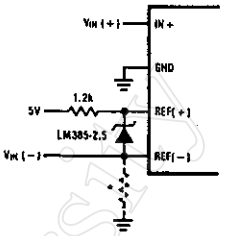
TL/H/5501–21

Power Supply as Reference



TL/H/5501–22

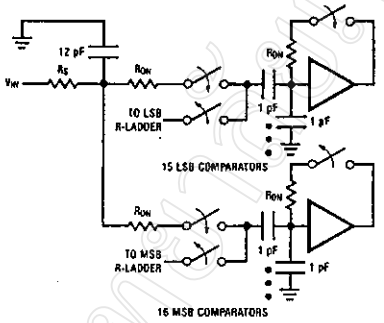
Input Not Referred to GND



* Current path must still exist from $V_{IN}(-)$ to ground

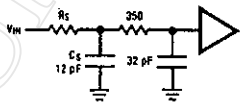
TL/H/5501–23

FIGURE 9. Analog Input Options



TL/H/5501–24

FIGURE 10a



TL/H/5501–25

FIGURE 10b

2.3 INPUT FILTERING

It should be made clear that transients in the analog input signal, caused by charging current flowing into V_{IN}, will not degrade the A/D's performance in most cases. In effect the ADC0820 does not "look" at the input when these transients occur. The comparators' outputs are not latched while $\overline{WR}$ is low, so at least 600 ns will be provided to charge the ADC's input capacitance. It is therefore not necessary to filter out these transients by putting an external cap on the V_{IN} terminal.

2.4 INHERENT SAMPLE-HOLD

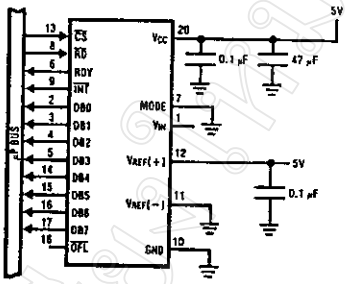
Another benefit of the ADC0820's input mechanism is its ability to measure a variety of high speed signals without the help of an external sample-and-hold. In a conventional SAR type converter, regardless of its speed, the input must remain at least ½ LSB stable throughout the conversion process if full accuracy is to be maintained. Consequently, for many high speed signals, this signal must be externally sampled, and held stationary during the conversion.

Sampled-data comparators, by nature of their input switching, already accomplish this function to a large degree (Section 1.2). Although the conversion time for the ADC0820 is 1.5 μs, the time through which V_{IN} must be 1/2 LSB stable is much smaller. Since the MS flash ADC uses V_{IN} as its "compare" input and the LS ADC uses V_{IN} as its "zero" input, the ADC0820 only "samples" V_{IN} when $\overline{WR}$ is low (Sections 1.3 and 2.2). Even though the two flashes are not done simultaneously, the analog signal is measured at one instant. The value of V_{IN} approximately 100 ns after the rising edge of $\overline{WR}$ (100 ns due to internal logic prop delay) will be the measured value.

Input signals with slew rates typically below 100 mV/μs can be converted without error. However, because of the input time constants, and charge injection through the opened comparator input switches, faster signals may cause errors. Still, the ADC0820's loss in accuracy for a given increase in signal slope is far less than what would be witnessed in a conventional successive approximation device. An SAR type converter with a conversion time as fast as 1 μs would still not be able to measure a 5V 1 kHz sine wave without the aid of an external sample-and-hold. The ADC0820, with no such help, can typically measure 5V, 7 kHz waveforms.

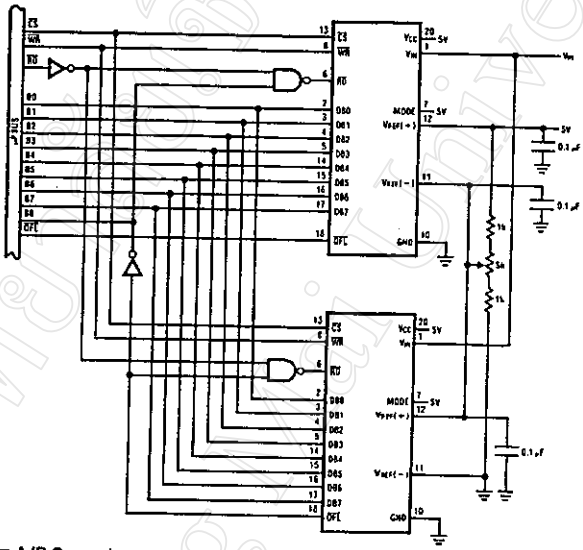
3.0 Typical Applications

8-Bit Resolution Configuration



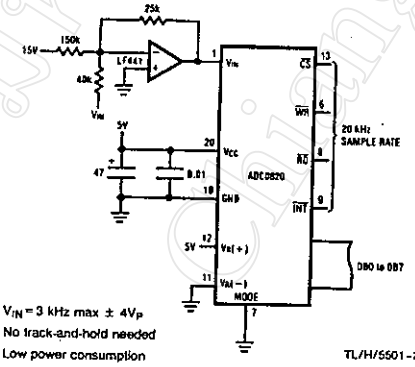
TL/H/5501-26

9-Bit Resolution Configuration



TL/H/5501-27

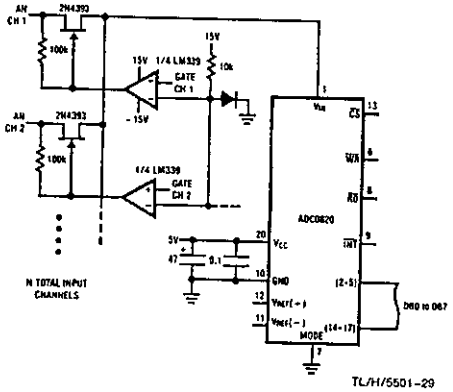
Telecom A/D Converter



- V_{IN} = 3 kHz max ± 4V_P
- No track-and-hold needed
- Low power consumption

TL/H/5501-28

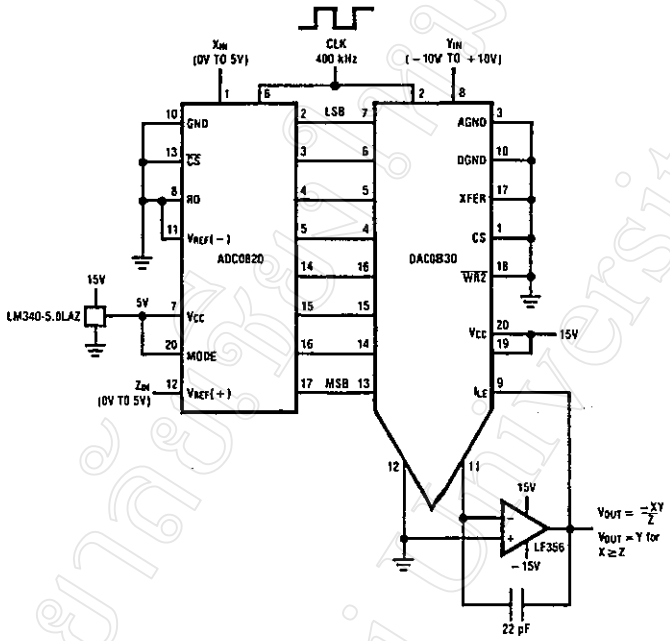
Multiple Input Channels



TL/H/5501-29

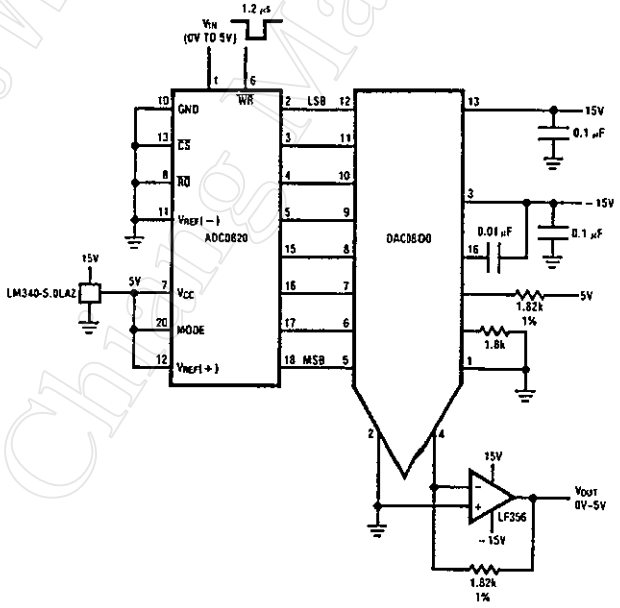
3.0 Typical Applications (Continued)

8-Bit 2-Quadrant Analog Multiplier



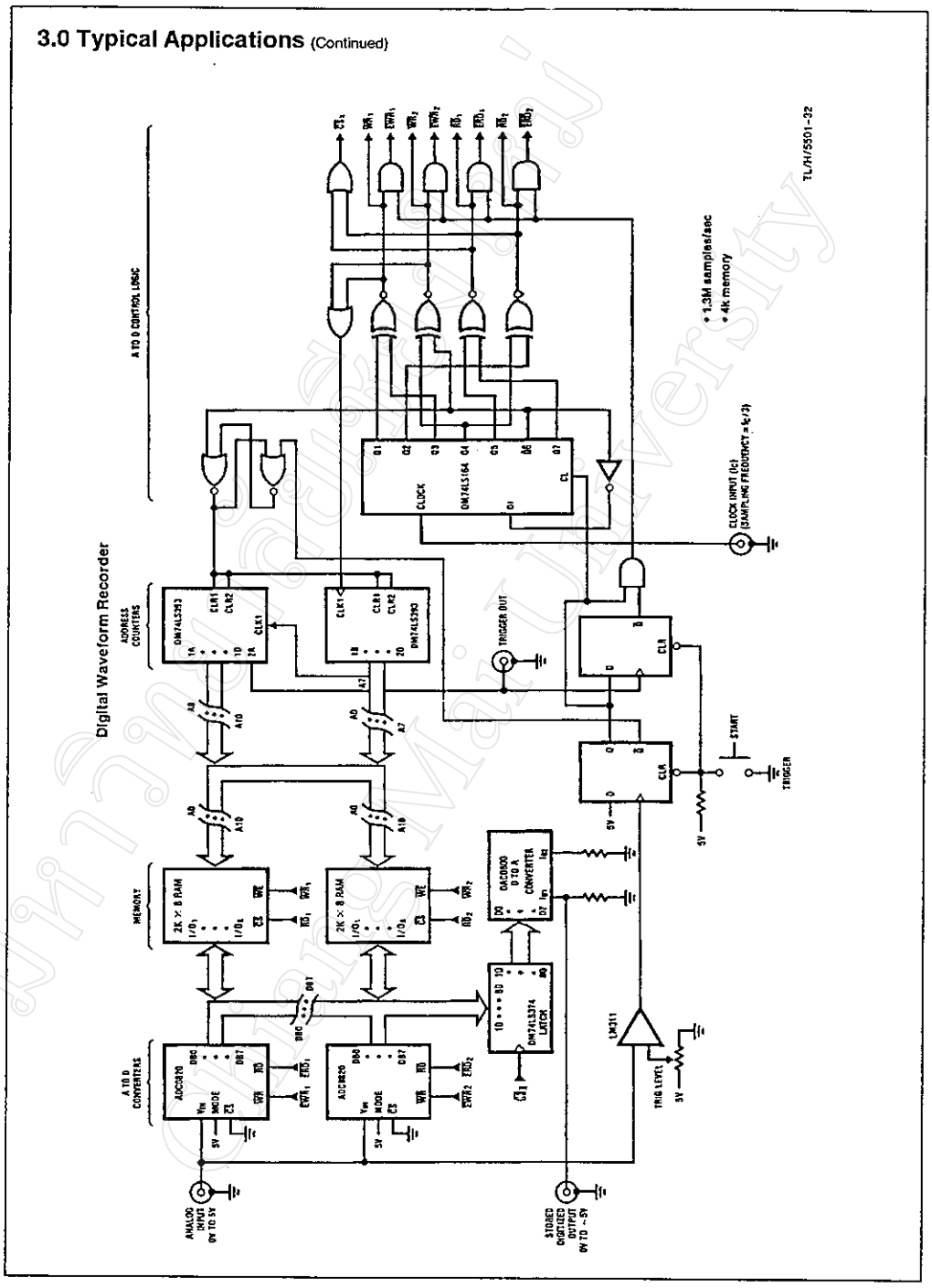
TL/H/5501–30

Fast Infinite Sample-and-Hold



TL/H/5501–31

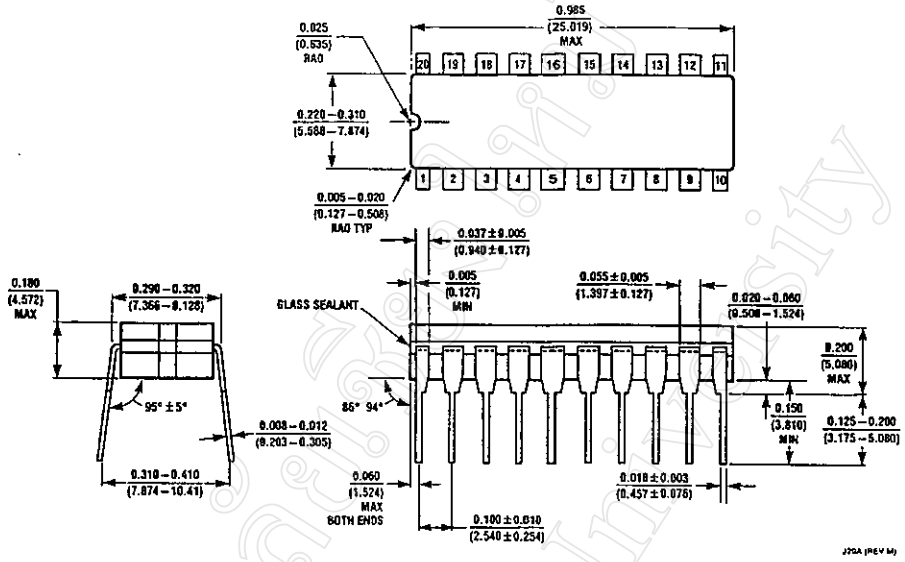
3.0 Typical Applications (Continued)



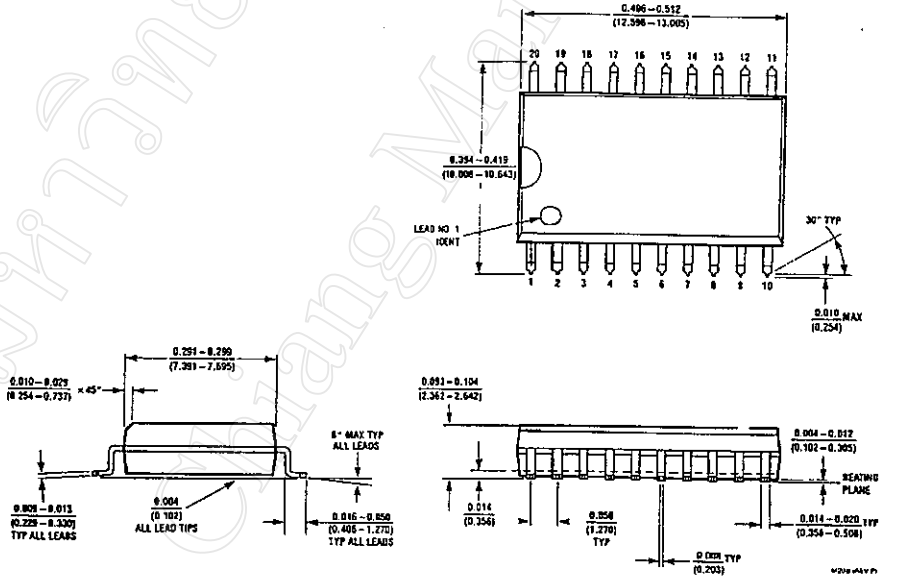
Ordering Information

Part Number	Total Unadjusted Error	Package	Temperature Range
ADC0820BCV	±½ LSB	V20A—Molded Chip Carrier	0°C to +70°C
ADC0820BCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820BCN		N20A—Molded DIP	0°C to +70°C
ADC0820CCJ	±1 LSB	J20A—Cerdip	−40°C to +85°C
ADC0820CCMSA		MSA20— Shrink Small Outline Package	0°C to +70°C
ADC0820CCV		V20A—Molded Chip Carrier	0°C to +70°C
ADC0820CCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820CIWM		M20B—Wide Body Small Outline	−40°C to +85°C
ADC0820CCN		N20A—Molded DIP	0°C to +70°C

Physical Dimensions inches (millimeters)

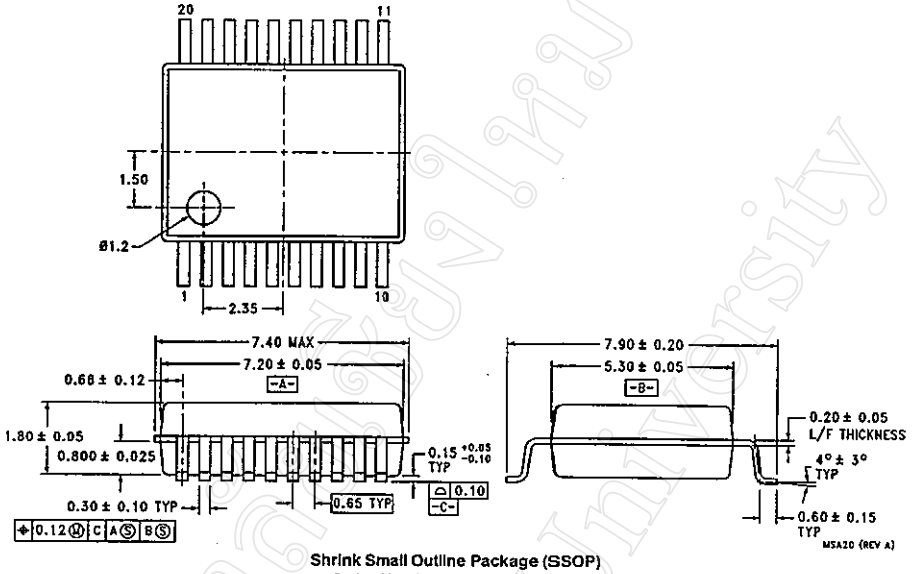


Hermetic Dual-In-Line Package (J)
Order Number ADC0820CCJ
NS Package Number J20A

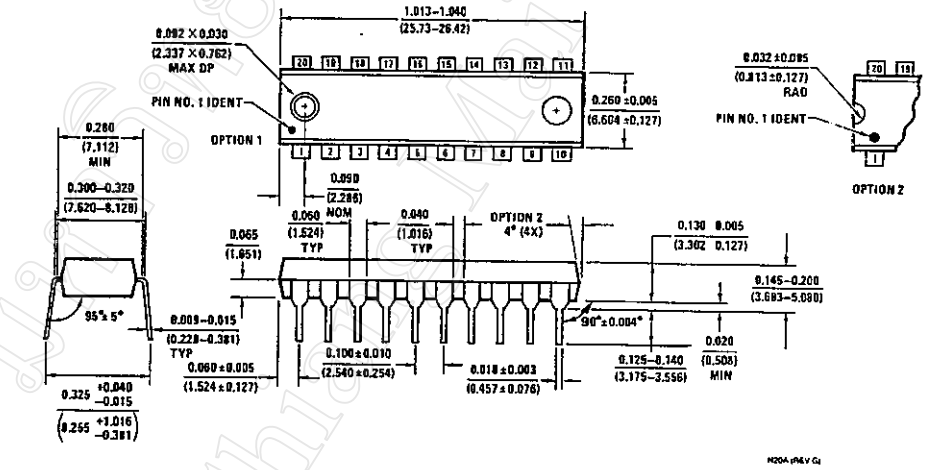


SO Package (M)
Order Number ADC0820BCWM, ADC0820CCWM or ADC0820CIWM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

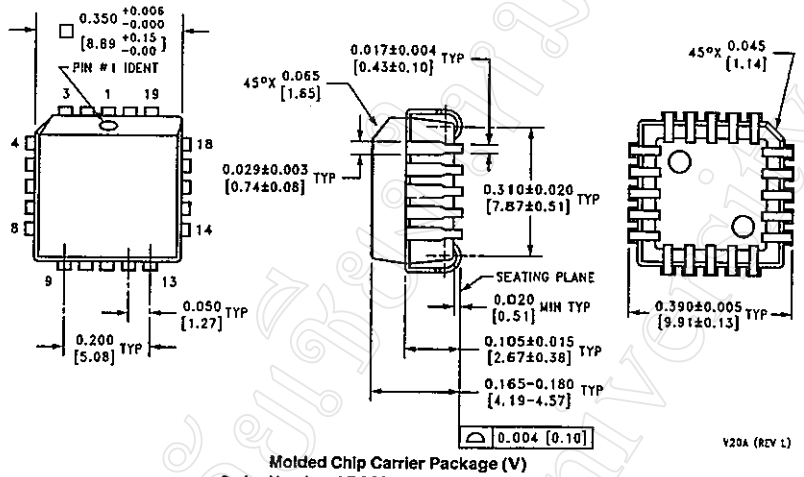


Shrink Small Outline Package (SSOP)
Order Number ADC0820CCMSA
NS Package Number MSA20



Molded Dual-In-Line Package (N)
Order Number ADC0820BCN or ADC0820CCN
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



Molded Chip Carrier Package (V)
Order Number ADC0820BCV or ADC0820CCV
NS Package Number V20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

ภาคผนวกที่ 4

8255 Programmable Interface Adepter

HARRIS Semiconductor

82C55A

CMOS Programmable Peripheral Interface

June 1998

Features

- Pin Compatible with NMOS 8255A
- 24 Programmable I/O Pins
- Fully TTL Compatible
- High Speed, No "Wait State" Operation with 5MHz and 8MHz 80C86 and 80C88
- Direct Bit Set/Reset Capability
- Enhanced Control Word Read Capability
- L7 Process
- 2.5mA Drive Capability on All I/O Ports
- Low Standby Power (ICCSB) 10µA

Description

The Harris 82C55A is a high performance CMOS version of the industry standard 8255A and is manufactured using a self-aligned silicon gate CMOS process (Scaled SAJI IV). It is a general purpose programmable I/O device which may be used with many different microprocessors. There are 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. The high performance and industry standard configuration of the 82C55A make it compatible with the 80C86, 80C88 and other microprocessors.

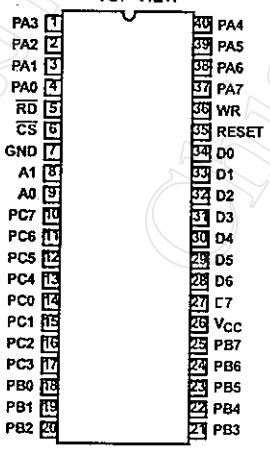
Static CMOS circuit design insures low operating power. TTL compatibility over the full military temperature range and bus hold circuitry eliminate the need for pull-up resistors. The Harris advanced SAJI process results in performance equal to or greater than existing functionally equivalent products at a fraction of the power.

Ordering Information

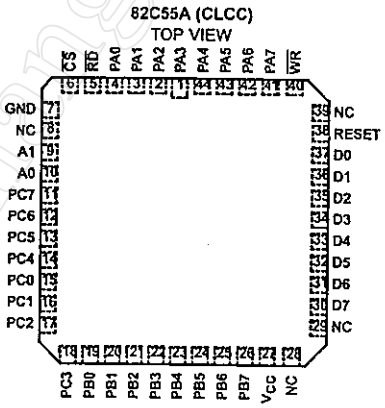
PART NUMBERS 5MHz	PART NUMBERS 8MHz	PACKAGE	TEMPERATURE RANGE	PKG. NO.
CP82C55A-5	CP82C55A	40 Ld PDIP	0°C to 70°C	E40.6
IP82C55A-5	IP82C55A		-40°C to 85°C	E40.6
CS82C55A-5	CS82C55A	44 Ld PLCC	0°C to 70°C	N44.65
IS82C55A-5	IS82C55A		-40°C to 85°C	N44.65
CD82C55A-5	CD82C55A	40 Ld CERDIP	0°C to 70°C	F40.6
ID82C55A-5	ID82C55A		-40°C to 85°C	F40.6
MD82C55A-5/B	MD82C55A/B		-55°C to 125°C	F40.6
8406601QA	8406602QA	SMD#		F40.6
MR82C55A-5/B	MR82C55A/B	44 Pad CLCC	-55°C to 125°C	J44.A
8406601XA	8406602XA	SMD#		J44.A

Pinouts

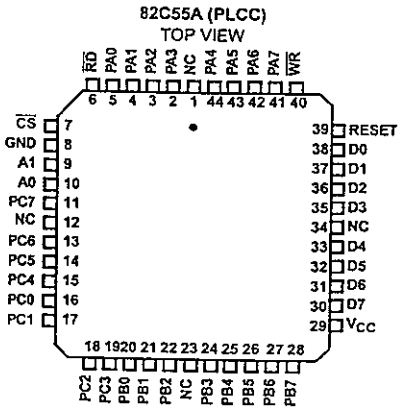
82C55A (DIP)
TOP VIEW



82C55A (CLCC)
TOP VIEW



82C55A (PLCC)
TOP VIEW



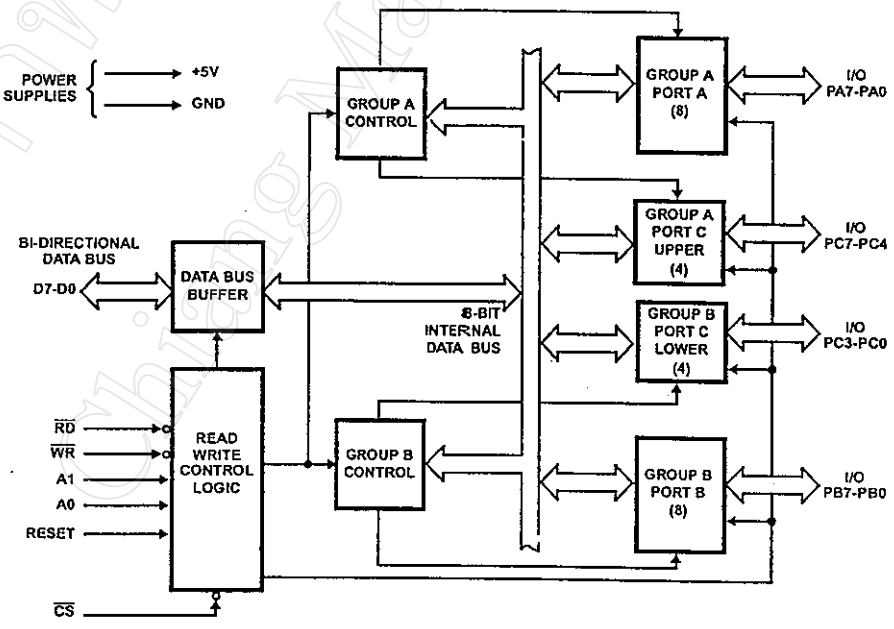
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2969.2

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	26		V_{CC}: The +5V power supply pin. A 0.1µF capacitor between pins 26 and 7 is recommended for decoupling.
GND	7		GROUND
D0-D7	27-34	I/O	DATA BUS: The Data Bus lines are bidirectional three-state pins connected to the system data bus.
RESET	35	I	RESET: A high on this input clears the control register and all ports (A, B, C) are set to the input mode with the "Bus Hold" circuitry turned on.
$\overline{CS}$	6	I	CHIP SELECT: Chip select is an active low input used to enable the 82C55A onto the Data Bus for CPU communications.
$\overline{RD}$	5	I	READ: Read is an active low input control signal used by the CPU to read status information or data via the data bus.
$\overline{WR}$	36	I	WRITE: Write is an active low input control signal used by the CPU to load control words and data into the 82C55A.
A0-A1	8, 9	I	ADDRESS: These input signals, in conjunction with the $\overline{RD}$ and $\overline{WR}$ inputs, control the selection of one of the three ports or the control word register. A0 and A1 are normally connected to the least significant bits of the Address Bus A0, A1.
PA0-PA7	1-4, 37-40	I/O	PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port.
PB0-PB7	18-25	I/O	PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port.
PC0-PC7	10-17	I/O	PORT C: 8-bit input and output port. Bus hold circuitry is present on this port.

Functional Diagram



Functional Description

Data Bus Buffer

This three-state bi-directional 8-bit buffer is used to interface the 82C55A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS) Chip Select. A "low" on this input pin enables the communcation between the 82C55A and the CPU.

(RD) Read. A "low" on this input pin enables 82C55A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 82C55A.

(WR) Write. A "low" on this input pin enables the CPU to write data or control words into the 82C55A.

(A0 and A1) Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register. They are normally connected to the least significant bits of the address bus (A0 and A1).

82C55A BASIC OPERATION

A1	A0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	Port A → Data Bus
0	1	0	1	0	Port B → Data Bus
1	0	0	1	0	Port C → Data Bus
1	1	0	1	0	Control Word → Data Bus
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	Data Bus → Port A
0	1	1	0	0	Data Bus → Port B
1	0	1	0	0	Data Bus → Port C
1	1	1	0	0	Data Bus → Control
					DISABLE FUNCTION
X	X	X	X	1	Data Bus → Three-State
X	X	1	1	0	Data Bus → Three-State

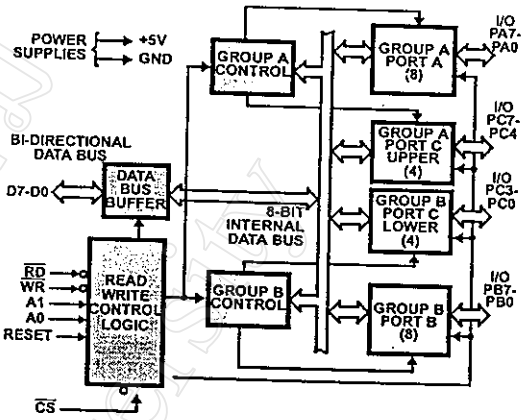


FIGURE 1. 82C55A BLOCK DIAGRAM. DATA BUS BUFFER, READ/WRITE, GROUP A & B CONTROL LOGIC FUNCTIONS

(RESET) Reset. A "high" on this input initializes the control register to 9Bh and all ports (A, B, C) are set to the input mode. "Bus hold" devices internal to the 82C55A will hold the I/O port inputs to a logic "1" state with a maximum hold current of 400µA.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 82C55A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 82C55A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the "Basic Operation" table. Figure 4 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic "1", as this implies control word mode information.

Ports A, B, and C

The 82C55A contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 82C55A.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A. See Figure 2A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer. See Figure 2B.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B. See Figure 2B.

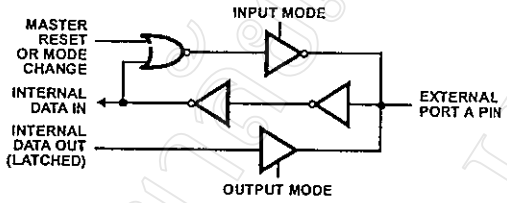


FIGURE 2A. PORT A BUS-HOLD CONFIGURATION

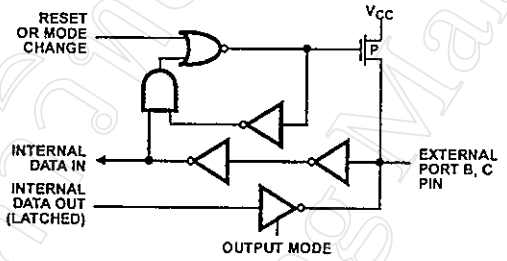


FIGURE 2B. PORT B AND C BUS-HOLD CONFIGURATION

FIGURE 2. BUS-HOLD CONFIGURATION

Operational Description

Mode Selection

There are three basic modes of operation than can be selected by the system software:

Mode 0 - Basic Input/Output
Mode 1 - Strobed Input/Output
Mode 2 - Bi-directional Bus

When the reset input goes "high", all ports will be set to the input mode with all 24 port lines held at a logic "one" level by internal bus hold devices. After the reset is removed, the 82C55A can remain in the input mode with no additional initialization required. This eliminates the need to pullup or pull-down resistors in all-CMOS designs. The control word register will contain 9Bh. During the execution of the system program, any of the other modes may be selected using a single output instruction. This allows a single 82C55A to service a variety of peripheral devices with a simple software maintenance routine. Any port programmed as an output port is initialized to all zeros when the control word is written.

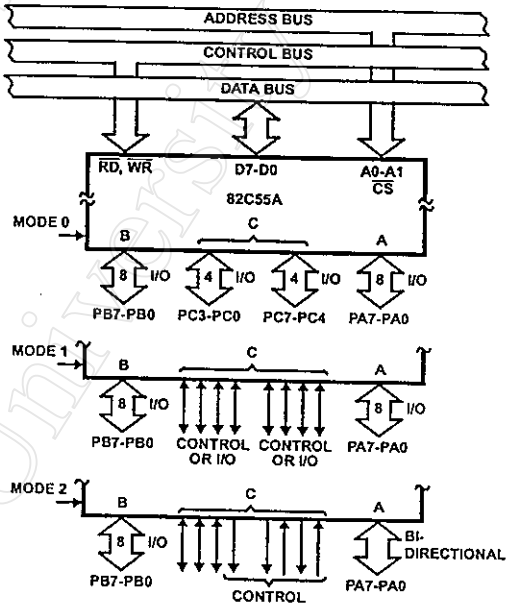


FIGURE 3. BASIC MODE DEFINITIONS AND BUS INTERFACE

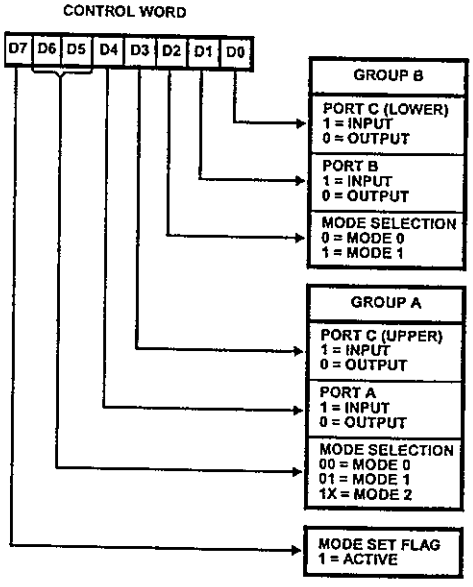


FIGURE 4. MODE DEFINITION FORMAT

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance: Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

The mode definitions and possible mode combinations may seem confusing at first, but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs. PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature (Figure 5)

Any of the eight bits of Port C can be Set or Reset using a single Output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were output ports.

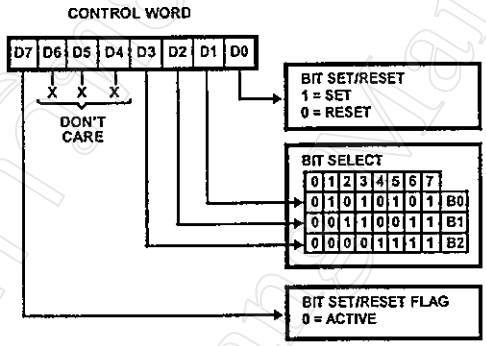


FIGURE 5. BIT SET/RESET FORMAT

Interrupt Control Functions

When the 82C55A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the programmer to enable or disable a CPU interrupt by a specific I/O device without affecting any other device in the interrupt structure.

INTE Flip-Flop Definition

(BIT-SET)-INTE is SET - Interrupt Enable

(BIT-RESET)-INTE is Reset - Interrupt Disable

NOTE: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No handshaking is required, data is simply written to or read from a specific port.

Mode 0 Basic Functional Definitions:

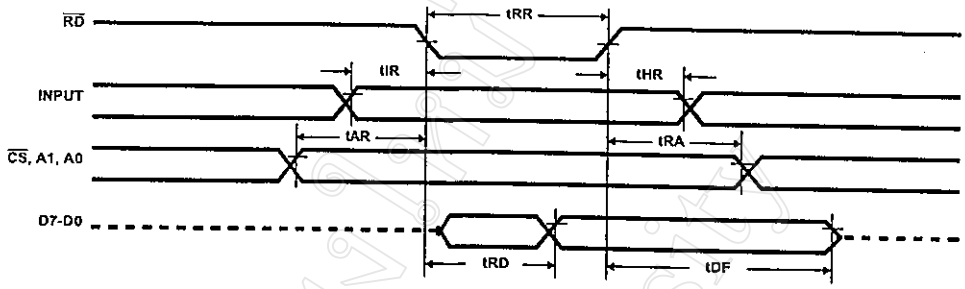
- Two 8-bit ports and two 4-bit ports
- Any Port can be input or output
- Outputs are latched
- Input are not latched
- 16 different Input/Output configurations possible

MODE 0 PORT DEFINITION

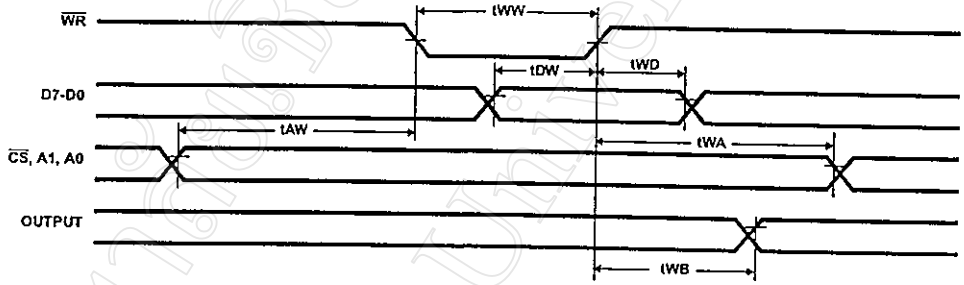
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (Upper)	#	PORT B	PORT C (Lower)
0	0	0	0	Output	Output	0	Output	Output
0	0	0	1	Output	Output	1	Output	Input
0	0	1	0	Output	Output	2	Input	Output
0	0	1	1	Output	Output	3	Input	Input
0	1	0	0	Output	Input	4	Output	Output
0	1	0	1	Output	Input	5	Output	Input
0	1	1	0	Output	Input	6	Input	Output
0	1	1	1	Output	Input	7	Input	Input
1	0	0	0	Input	Output	8	Output	Output
1	0	0	1	Input	Output	9	Output	Input
1	0	1	0	Input	Output	10	Input	Output
1	0	1	1	Input	Output	11	Input	Input
1	1	0	0	Input	Input	12	Output	Output
1	1	0	1	Input	Input	13	Output	Input
1	1	1	0	Input	Input	14	Input	Output
1	1	1	1	Input	Input	15	Input	Input

82C55A

Mode 0 (Basic Input)

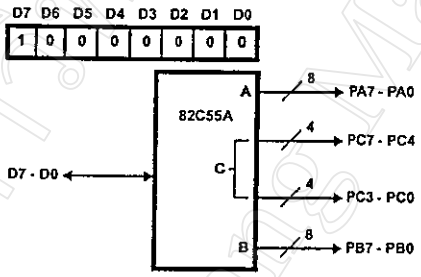


Mode 0 (Basic Output)

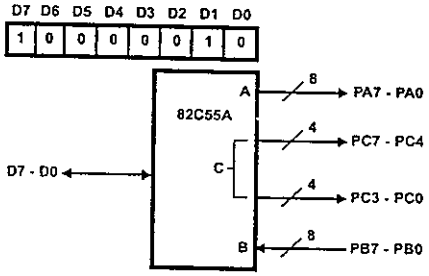


Mode 0 Configurations

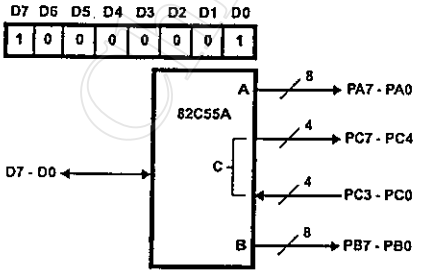
CONTROL WORD #0



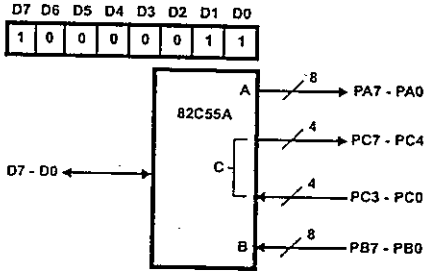
CONTROL WORD #2



CONTROL WORD #1

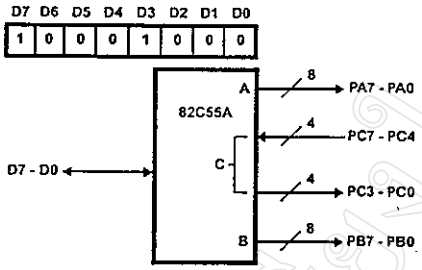


CONTROL WORD #3

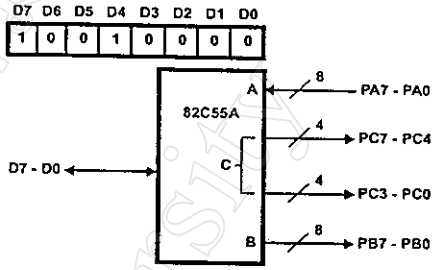


Mode 0 Configurations (Continued)

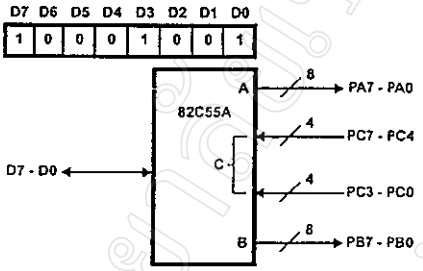
CONTROL WORD #4



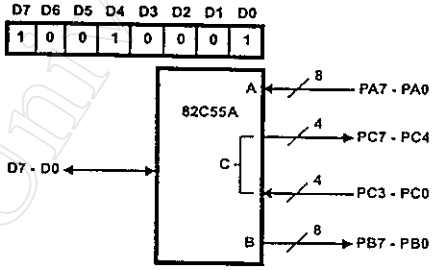
CONTROL WORD #8



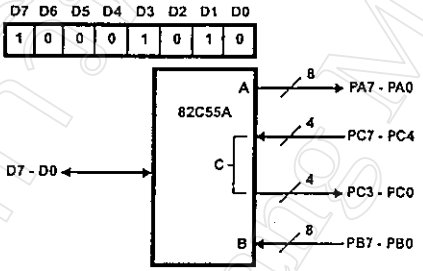
CONTROL WORD #5



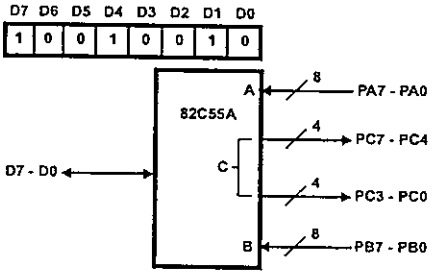
CONTROL WORD #9



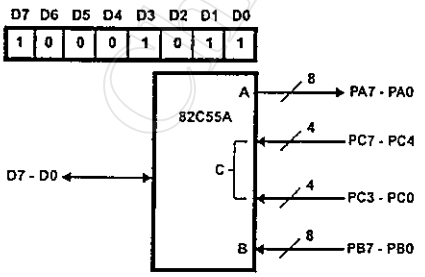
CONTROL WORD #6



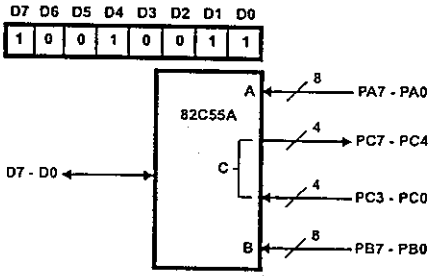
CONTROL WORD #10



CONTROL WORD #7

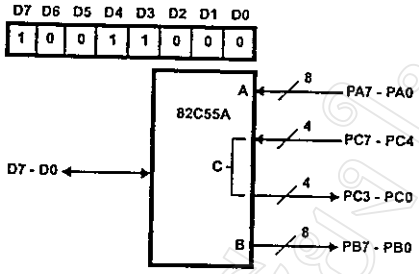


CONTROL WORD #11

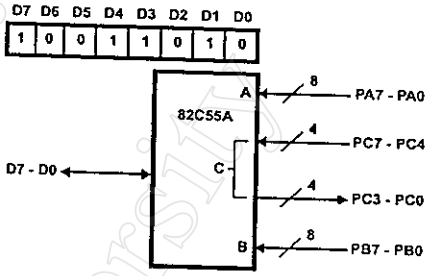


Mode 0 Configurations (Continued)

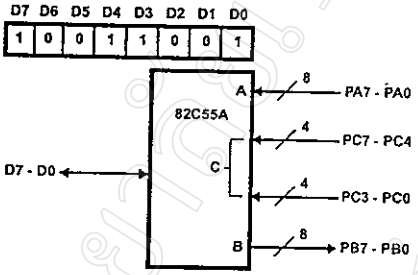
CONTROL WORD #12



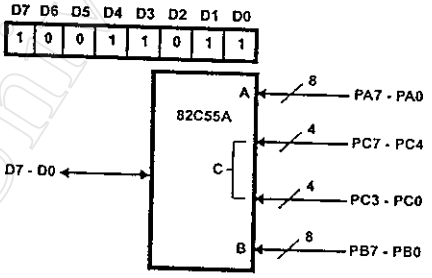
CONTROL WORD #14



CONTROL WORD #13



CONTROL WORD #15



Operating Modes

Mode 1 - (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "hand shaking" signals. In mode 1, port A and port B use the lines on port C to generate or accept these "hand shaking" signals.

Mode 1 Basic Function Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit port and one 4-bit control/data port
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit port.

Input Control Signal Definition

(Figures 6 and 7)

STB (Strobe Input)

A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch: in essence, and acknowledgment. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

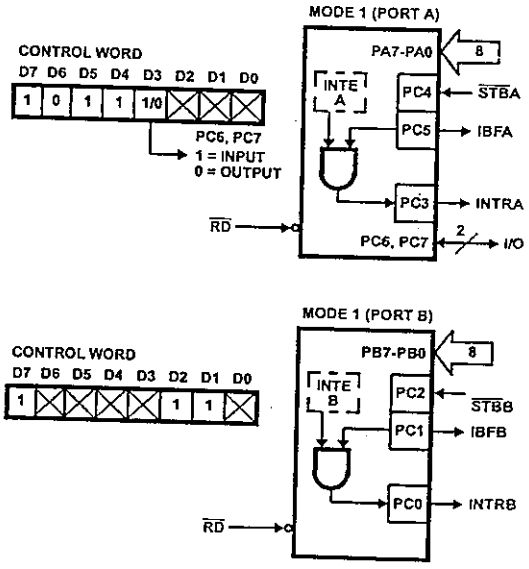


FIGURE 6. MODE 1 INPUT

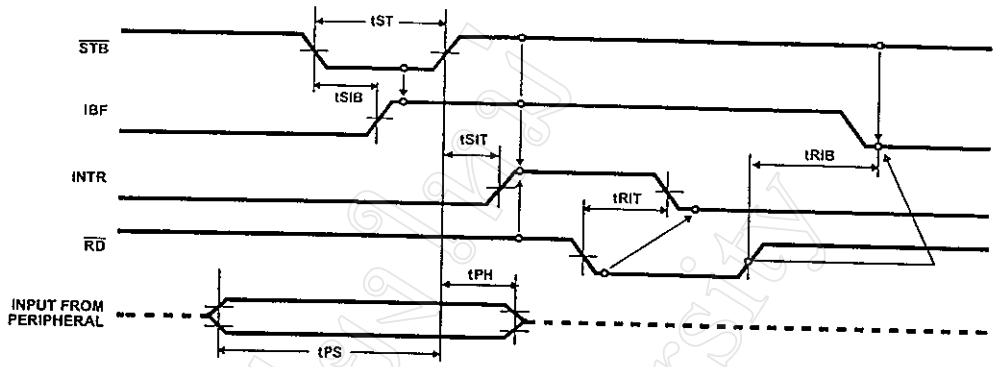


FIGURE 7. MODE 1 (STROBED INPUT)

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when and input device is requesting service. INTR is set by the condition: $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC4.

INTE B

Controlled by bit set/reset of PC2.

Output Control Signal Definition

(Figure 8 and 9)

$\overline{OBF}$ - Output Buffer Full F/F). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to be specified port. This does not mean valid data is sent out of the part at this time since $\overline{OBF}$ can go true before data is available. Data is guaranteed valid at the rising edge of $\overline{OBF}$. (See Note 1). The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ input being low.

$\overline{ACK}$ - Acknowledge Input). A "low" on this input informs the 82C55A that the data from Port A or Port B is ready to be accepted. In essence, a response from the peripheral device indicating that it is ready to accept data, (See Note 1).

INTR - (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by Bit Set/Reset of PC6.

INTE B

Controlled by Bit Set/Reset of PC2.

NOTE:

1. To strobe data into the peripheral device, the user must operate the strobe line in a hand shaking mode. The user needs to send $\overline{OBF}$ to the peripheral device, generates an $\overline{ACK}$ from the peripheral device and then latch data into the peripheral device on the rising edge of $\overline{OBF}$.

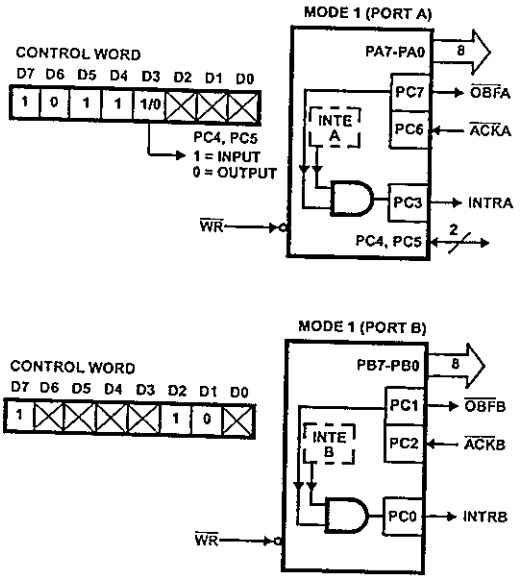


FIGURE 8. MODE 1 OUTPUT

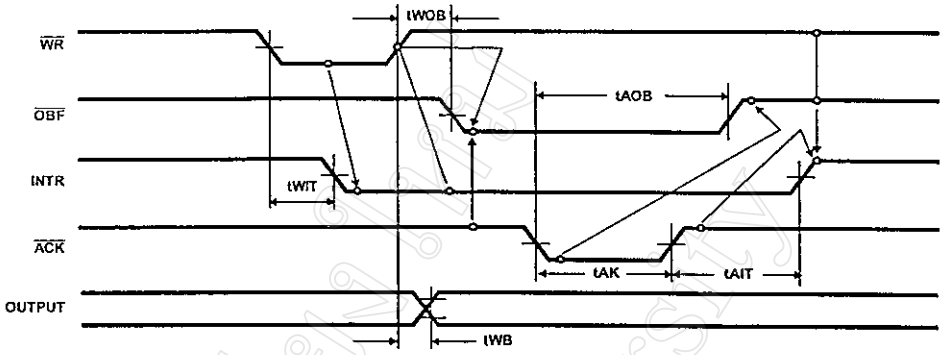
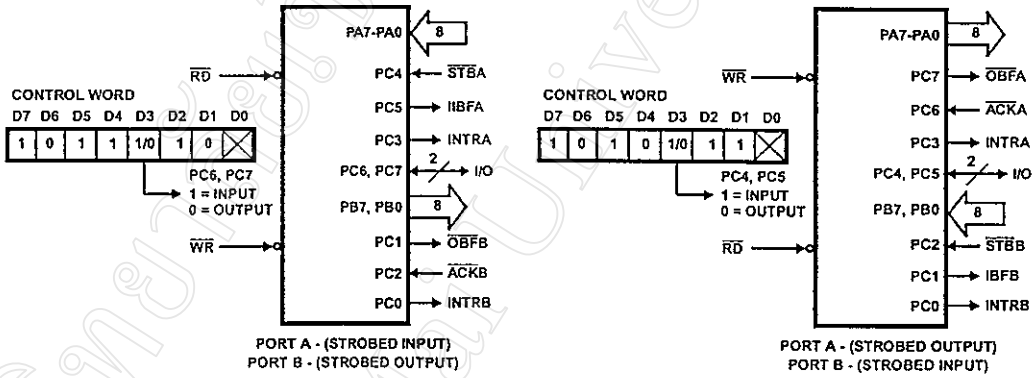


FIGURE 9. MODE 1 (STROBED OUTPUT)



Combinations of Mode 1: Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

FIGURE 10. COMBINATIONS OF MODE 1

Operating Modes

Mode 2 (Strobed Bi-Directional Bus I/O)

The functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bi-directional bus I/O). "Hand shaking" signals are provided to maintain proper bus flow discipline similar to Mode 1. Interrupt generation and enable/disable functions are also available.

Mode 2 Basic Functional Definitions:

- Used in Group A only
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C)
- Both inputs and outputs are latched
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A)

Bi-Directional Bus I/O Control Signal Definition
(Figures 11, 12, 13, 14)

INTR - (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ - (Output Buffer Full). The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ - (Acknowledge). A "low" on this input enables the three-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 - (The INTE flip-flop associated with $\overline{OBF}$). Controlled by bit set/reset of PC4.

Input Operations

$\overline{STB}$ - (Strobe Input). A "low" on this input loads data into the input latch.

IBF - (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 - (The INTE flip-flop associated with IBF). Controlled by bit set/reset of PC4.

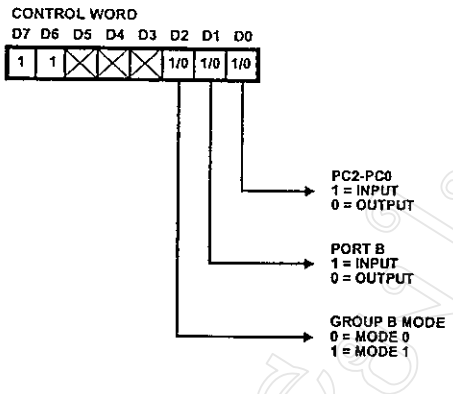


FIGURE 11. MODE CONTROL WORD

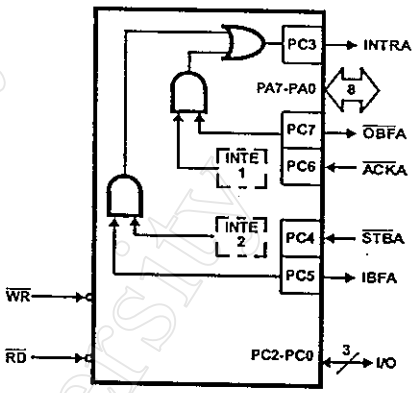
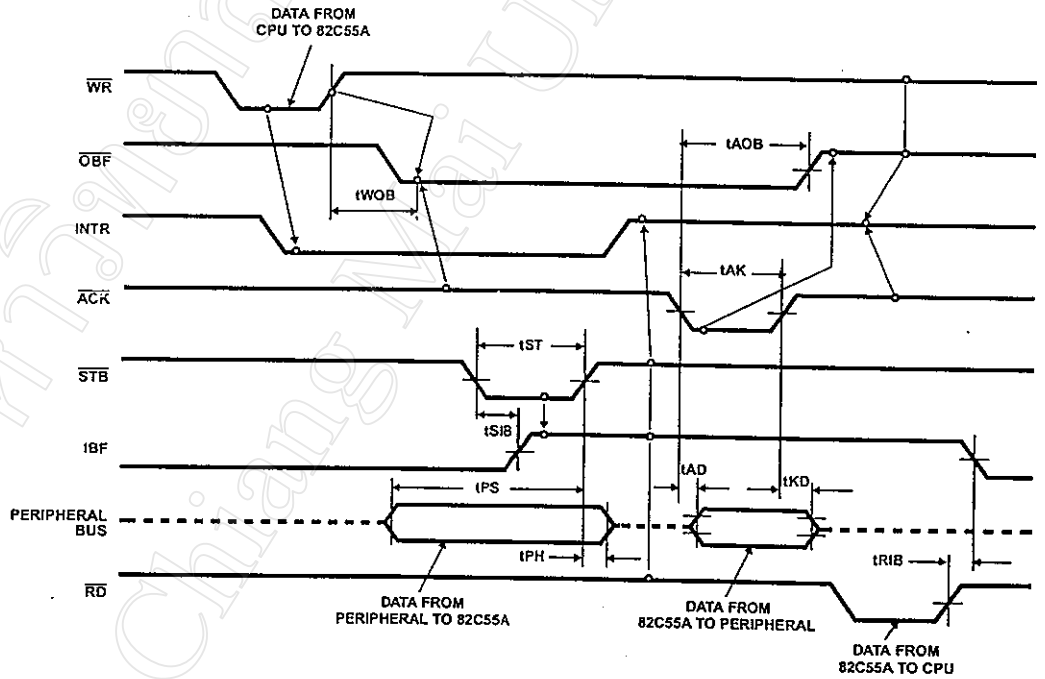


FIGURE 12. MODE 2



NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before RD is permissible. (INTR = IBF • MASK • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • MASK • $\overline{ACK}$ • $\overline{WR}$)

FIGURE 13. MODE 2 (BI-DIRECTIONAL)

ภาคผนวกที่ 5

Q-BAISC Program

```
'*************************************************************
'Program  : SPECTROPHOTOMETER(SPECTRO.BAS)
'Language : Quickbasics version 4.5
'Edit by  : RADEN PHOTHIDEE
'         Laser and Applied Optics Research Laboratory
'         PB1-346 Department of Physics Faculty of Science
'         Chiangmai University
'*************************************************************
CLS
DIM a(10000) AS INTEGER, b(10000) AS INTEGER
PA = &H308
PB = &H309
PC = &H30A
PCC = &H30B
OUT PCC, &H93
    BI = 0: BF = 0
  FOR i = 1 TO 10000
xx:
   BI = INP(PC)
    IF BI = BF THEN GOTO xx
     a(i) = INP(PA)
   BF = BI
    FOR r = 1 TO 18
   NEXT r
  NEXT i
INPUT "FILENAME :", FILENAME$
OPEN "C:\DATA" + FILENAME$ FOR OUTPUT AS #1
    FOR i = 1 TO 10000
    PRINT #1, a(i)
   NEXT i
```

```
CLOSE #1
CLS
INPUT "FILENAME FOR SMOOTH :", f$
n = 9999
OPEN f$ FOR INPUT AS 1
FOR i = 0 TO n
INPUT #1, a(i)
NEXT
CLOSE


FOR i = 1 TO n
IF a(i) < 100 THEN GOTO ZZ
NEXT
ZZ:
m = 0
FOR j = i TO n
IF a(j) < 225 THEN m = m + 1: a(m) = a(j)
IF m = 2500 THEN GOTO yy
NEXT

yy:
PRINT "Data Start st .... "; i
INPUT "FILENAME TO SAVE :", ff$
OPEN ff$ FOR OUTPUT AS 1
FOR j = 1 TO 2500
PRINT #1, a(j)
NEXT
CLOSE
```

```
INPUT "I am here..."; t

fff$ = "c:\qb\smooth\one2.txt"
OPEN fff$ FOR OUTPUT AS #2
m = 20
FOR i = 0 TO n - m
x = 0
FOR j = 1 TO m
x = x + a(i + j)
NEXT j
a(i) = x / m
NEXT i

FOR i = 1 TO 10000
PRINT #2, a(i)
NEXT
CLOSE #2
END
```

ประวัติผู้เขียน

ชื่อ	นายระเด่น โพธิ์ดี
วัน เดือน ปี เกิด	19 พฤษภาคม 2517
ประวัติการศึกษา	สำเร็จการศึกษามัธยมศึกษาตอนปลาย โรงเรียนนครสวรรค์ อ. เมือง จ. นครสวรรค์ ปีการศึกษา 2535 สำเร็จการศึกษาปริญญาวิทยาศาสตรบัณฑิต สาขาวิชาฟิสิกส์อุตสาหกรรมและอุปกรณ์การแพทย์ สถาบันเทคโนโลยีพระจอมเกล้าพระนครเหนือ ปีการศึกษา 2540