Rachanon Intharasakul 2008: Design and Implementation System for Nonbinary Encoder and Decoder with FPGA Board. Master of Engineering (Electrical Engineering), Major Field: Electrical Engineering, Department of Electrical Engineering. Thesis Advisor: Assistant Professor Usana Tuntoolavest, Ph.D. 83 pages.

Channel coding is the main method to increase reliability of data communications, especially for wireless communication systems. Almost all channel codes were designed for binary symbol for simplicity. However, some applications require the use of nonbinary symbol such as the outer codes of concatenated codes. A particular example is convolutional vector symbol decoding which was designed for large symbols. The typical size is 32 bits/symbol. In this case, the method and the system for encoding and decoding them need to be redesigned.

This thesis is focused on the design and implementation of nonbinary encoding and decoding system using integrated circuit technology by FPGA board. To test the designed systems and the interface between the FPGA board and the computer, the (3, 2, 2) nonbinary convolutional encoding with 32 bits/symbol and some functions of vector symbol decoding have been implemented. They worked exactly as designed.

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