

Tanin Duangjan 2009: Design of Low-power VLSI Digital Circuit Using Multiple Supply Voltages. Master of Engineering (Electrical Engineering), Major Field: Electrical Engineering, Department of Electrical Engineering. Thesis Advisor: Assistant Professor Chugiat Garagate, Ph.D. 106 pages.

This study proposes the multiple voltage supply technique for low-power design of VLSI system. This technique applies difference levels of voltages to each of logic gate in circuit to reduce power dissipation. C programming was used to develop the directed acyclic graph algorithm to track path in network graph model. The processes were as follows. First, to compute the delay time of each path, the algorithm starts from its primary input to primary output. The longest delay time was the critical path and the other paths being shorter than the critical path were called non-critical path. Second, the three supply voltages were applied to each logic gate in both critical and non-critical paths. For the critical path, 5.0 volts were applied to all gates. Regarding non-critical paths, 3.3 volts and 4.0 volts were applied to those paths, which the total delay time must less than the critical path. Finally, the power dissipations of logic gates in each path were computed. The results showed that, in the same circuit, the maximum delay time applying the mixed 3.3, 4.0 and 5.0 volts were equal to those applying 5.0 volts only. In addition, the total dynamic power dissipation of the mixed 3.3, 4.0 and 5.0 volts were reduced about 8.3-13.7% when compared to those of the maximum voltages.

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Thesis Advisor's signature

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