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Siseerot Ketkaew and Krisada Bisyuyabud. 2007. A Prototype For Dust Trap by Applied High Voltage DC Switching Power Supply. Proceedings of PCC Nagoya 2007, The Fourth Power Conversion Conference, Nagoya Congress Center, Nagoya, Japan.

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http://www.cpe.ku.ac.th/~yuen/204471/power/switching_regulator/#how%20it%20work

http://pdf1.alldatasheet.co.kr/datasheet-pdf/view/32418/TOSHIBA/TLP250.html

http://www.datasheetcatalog.com/datasheets_pdf/T/L/4/9/TL494CD.shtml

http://www.datasheetcatalog.com/datasheets_pdf/I/R/F/P/IRFP460.shtml

ภาคผนวก

ภาคผนวก ก

ดาต้าชีตไอซีเบอร์ TLP250

TOSHIBA Photocoupler GaAlAs Ired & Photo−IC

TLP250

Transistor Inverter

Inverter For Air Conditionor

IGBT Gate Drive

Power MOS FET Gate Drive

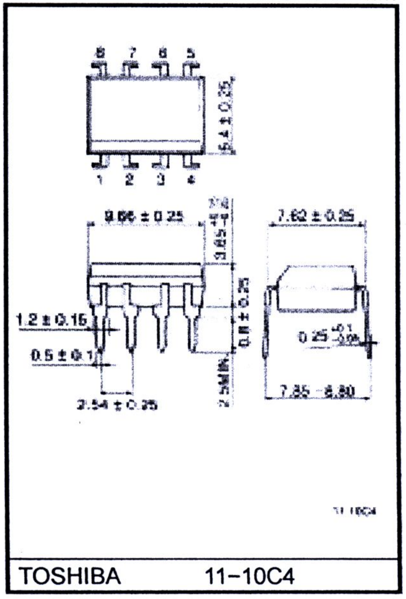
The TOSHIBA TLP250 consists of a GaAlAs light emitting diode and a integrated photodetector.
This unit is 8−lead DIP package.
TLP250 is suitable for gate driving circuit of IGBT or power MOS FET.

- Input threshold current: I_F=5mA(max.)
- Supply current (I_{CC}): 11mA(max.)
- Supply voltage (V_{CC}): 10−35V
- Output current (I_O): ±1.5A (max.)
- Switching time (t_{pLH}/t_{pHL}): 1.5μs(max.)
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file No.E67349
- Option (D4) type
  VDE approved: DIN VDE0884/06.92,certificate No.76823
  Maximum operating insulation voltage: 630V_{PK}
  Highest permissible over voltage: 4000V_{PK}

(Note) When a VDE0884 approved type is needed, please designate the "option (D4)"

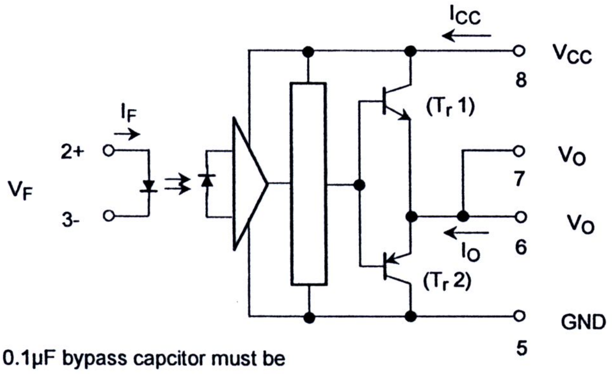
- Creepage distance: 6.4mm(min.)
  Clearance: 6.4mm(min.)

Unit in mm



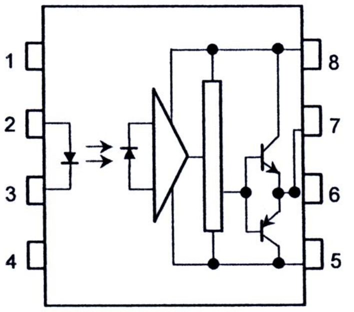
Weight: 0.54 g

Schmatic



A 0.1μF bypass capcitor must be connected between pin 8 and 5 (See Note 5).

Pin Configuration (top view)



1 : N.C.
2 : Anode
3 : Cathode
4 : N.C.
5 : GND
6 : V_O (Output)
7 : V_O
8 : V_{CC}

Truth Table

		Tr1	Tr2
Input LED	On	On	Off
	Off	Off	On

Absolute Maximum Ratings (Ta = 25°C)

	Characteristic		Symbol	Rating	Unit
LED	Forward current		I_F	20	mA
	Forward current derating (Ta ≥ 70°C)		$\Delta I_F / \Delta Ta$	−0.36	mA / °C
	Peak transient forward curent (Note 1)		I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Junction temperature		Tj	125	°C
Detector	"H"peak output current ($P_W \le 2.5\mu s, f \le 15kHz$) (Note 2)		I_{OPH}	−1.5	A
	"L"peak output current ($P_W \le 2.5\mu s, f \le 15kHz$) (Note 2)		I_{OPL}	+1.5	A
	Output voltage	(Ta ≤ 70°C)	V_O	35	V
		(Ta = 85°C)		24	
	Supply voltage	(Ta ≤ 70°C)	V_{CC}	35	V
		(Ta = 85°C)		24	
	Output voltage derating (Ta ≥ 70°C)		$\Delta V_O / \Delta Ta$	−0.73	V / °C
	Supply voltage derating (Ta ≥ 70°C)		$\Delta V_{CC} / \Delta Ta$	−0.73	V / °C
	Junction temperature		Tj	125	°C
Operating frequency (Note 3)			f	25	kHz
Operating temperature range			T_{opr}	−20~85	°C
Storage temperature range			T_{stg}	−55~125	°C
Lead soldering temperature (10 s) (Note 4)			T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%) (Note 5)			BV_S	2500	Vrms

Note 1: Pulse width $P_W \le 1\mu s$, 300pps

Note 2: Exporenential wavefom

Note 3: Exporenential wavefom, $I_{OPH} \le -1.0A(\le 2.5\mu s)$, $I_{OPL} \le +1.0A(\le 2.5\mu s)$

Note 4: It is 2 mm or more from a lead root.

Note 5: Device considerd a two terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

Note 6: A ceramic capacitor(0.1μF) should be connected from pin 8 to pin 5 to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching proparty. The total lead length between capacitor and coupler should not exceed 1cm.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.		Unit
Input current, on (Note 7)	$I_{F(ON)}$	7	8	10		mA
Input voltage, off	$V_{F(OFF)}$	0	—	0.8		V
Supply voltage	V_{CC}	15	—	30	20	V
Peak output current	I_{OPH}/I_{OPL}	—	—	±0.5		A
Operating temperature	T_{opr}	−20	25	70	85	°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

Electrical Characteristics (Ta = −20~70°C, unless otherwise specified)

Characteristic		Symbol	Test Circuit	Test Condition		Min.	Typ.*	Max.	Unit
Input forward voltage		V_F	—	I_F = 10 mA , Ta = 25°C			1.6	1.8	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	—	I_F = 10 mA		—	−2.0	—	mV / °C
Input reverse current		I_R	—	V_R = 5V, Ta = 25°C			—	10	μA
Input capacitance		C_T	—	V = 0 , f = 1MHz , Ta = 25°C		—	45	250	pF
Output current	"H" level	I_{OPH}	3	V_{CC} = 30V (*1)	I_F = 10 mA V_{8-6} = 4V	−0.5	−1.5	—	A
	"L" level	I_{OPL}	2		I_F = 0 V_{6-5} = 2.5V	0.5	2	—	
Output voltage	"H" level	V_{OH}	4	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, I_F = 5mA		11	12.8	—	V
	"L" level	V_{OL}	5	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_F = 0.8V		—	−14.2	−12.5	
Supply current	"H" level	I_{CCH}	—	V_{CC} = 30V, I_F = 10mA Ta = 25°C		—	7	—	mA
				V_{CC} = 30V, I_F = 10mA		—	—	11	
	"L" level	I_{CCL}	—	V_{CC} = 30V, I_F = 0mA Ta = 25°C		—	7.5	—	
				V_{CC} = 30V, I_F = 0mA		—	—	11	
Threshold input current	"Output L→H"	I_{FLH}	—	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_O > 0V		—	1.2	5	mA
Threshold input voltage	"Output H→L"	I_{FHL}	—	V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω, V_O < 0V		0.8	—	—	V
Supply voltage		V_{CC}	—			10	—	35	V
Capacitance (input−output)		C_S	—	V_S = 0 , f = 1MHz Ta = 25• •		—	1.0	2.0	pF
Resistance(input−output)		R_S	—	V_S = 500V , Ta = 25°C R.H.≤ 60%		1×10^{12}	10^{14}	—	Ω

* All typical values are at Ta = 25°C (*1): Duration of I_O time ≤ 50μs

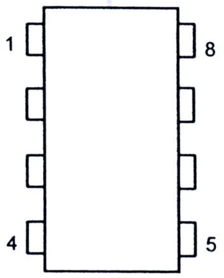
Switching Characteristics (Ta = –20~70°C , unless otherwise specified)

Characteristic		Symbol	Test Cir–cuit	Test Condition	Min.	Typ.*	Max.	Unit
Propagation delay time	L→H	t_{pLH}	6	I_F = 8mA (Note 7) V_{CC1} = +15V, V_{EE1} = −15V R_L = 200Ω	—	0.15	0.5	μs
	H→L	t_{pHL}			—	0.15	0.5	
Output rise time		t_r			—	—	—	
Output fall time		t_f			—	—	—	
Common mode transient immunity at high level output		C_{MH}	7	V_{CM} = 600V, I_F = 8mA V_{CC} = 30V, Ta = 25°C	−5000	—	—	V / μs
Common mode transient immunity at low level output		C_{ML}	7	V_{CM} = 600V, I_F = 0mA V_{CC} = 30V, Ta = 25°C	5000	—	—	V / μs

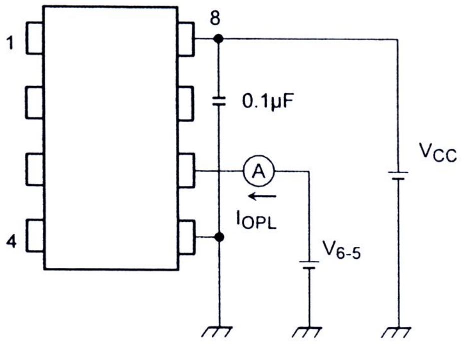
* All typical values are at Ta = 25°C

Note 7: Input signal rise time (fall time) < 0.5 μs.

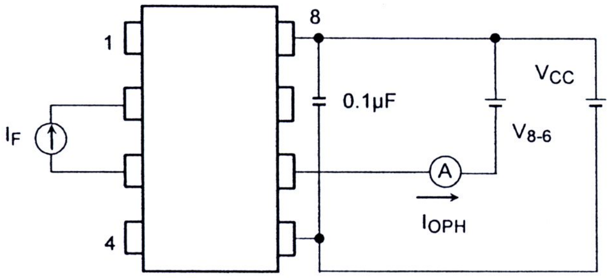
Test Circuit 1 :



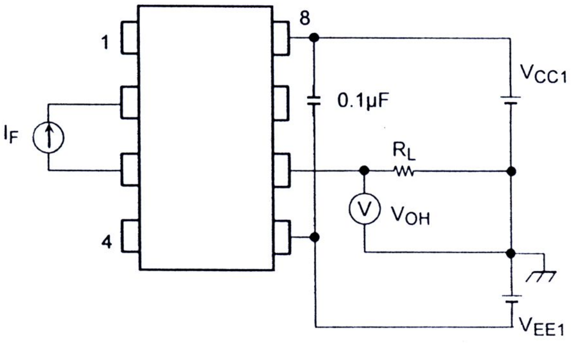
Test Circuit 2 : IOPL



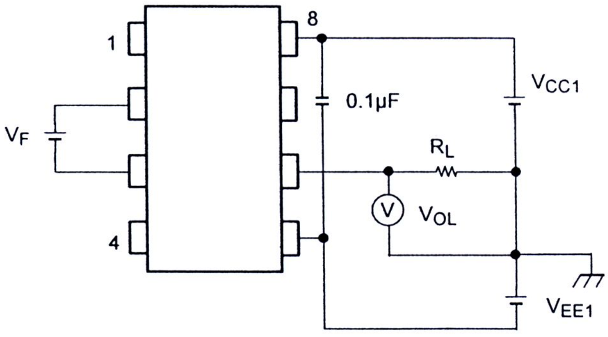
Test Circuit 3 : IOPH



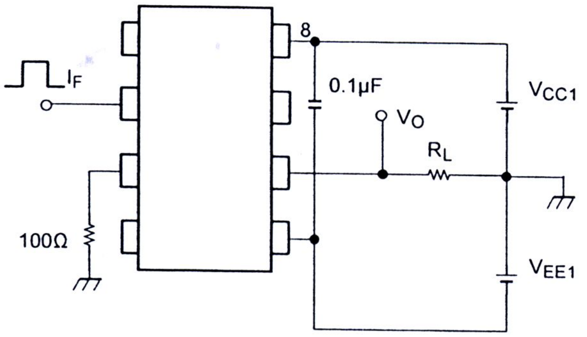
Test Circuit 4 : VOH

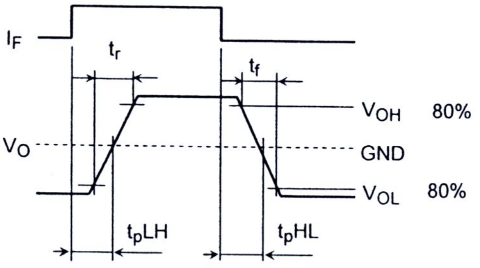


Test Circuit 5 : V_{OL}

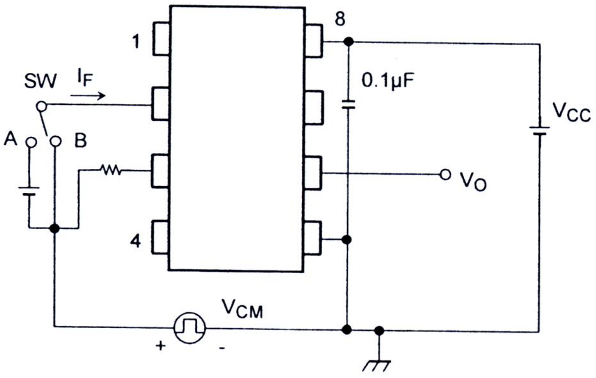


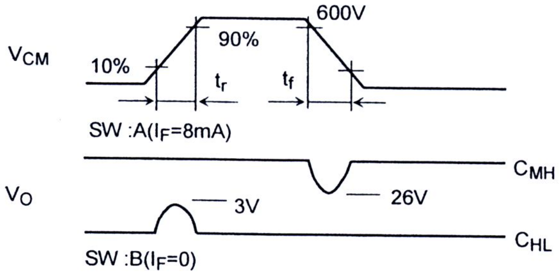
Test Circuit 6: t_{pLH}, t_{pHL}, t_r t_f





Test Circuit 7: C_{MH}, C_{ML}



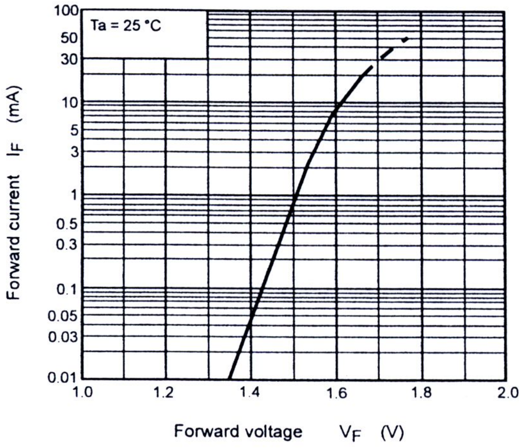


$$C_{ML} = \frac{480\ (V)}{t_{r\ (\mu s)}}$$

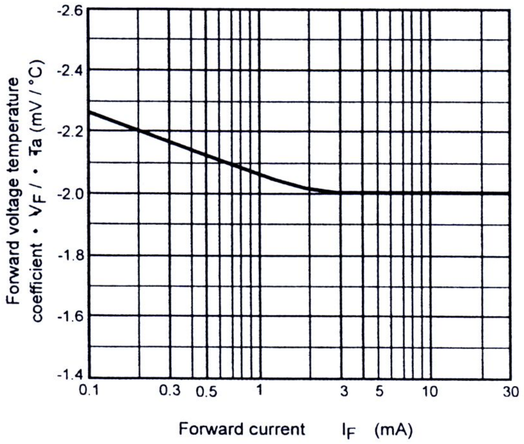
$$C_{MH} = \frac{480\ (V)}{t_{f\ (\mu s)}}$$

C_{ML}(C_{MH}) is the maximum rate of rise (fall) of the common mode voltage that can be sustained with the output voltage in the low (high) state.

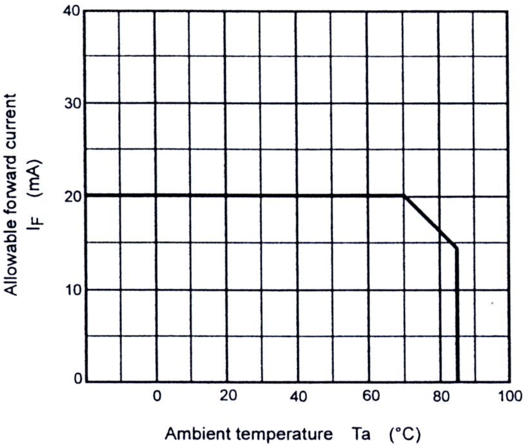
I_F – V_F



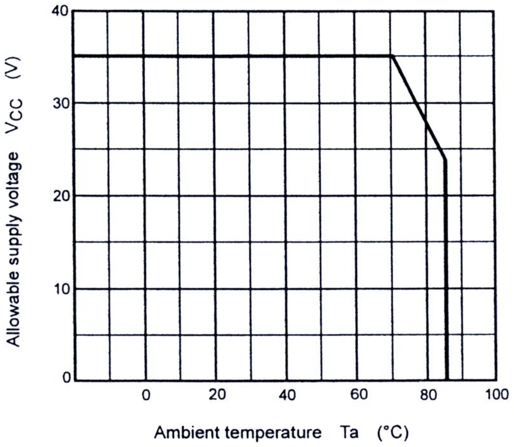
• V_F / • Ta – I_F



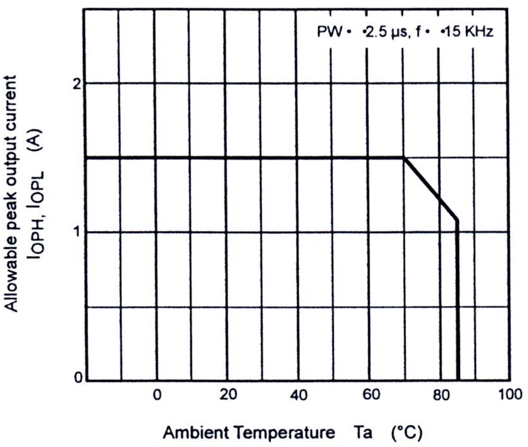
I_F – Ta



V_{CC} – Ta



I_{OPH}, I_{OPL} – Ta



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ภาคผนวก ข

ดาต้าชีตเพาเวอร์มอสเฟต เบอร์ IRFP460

FAIRCHILD
SEMICONDUCTOR™

IRFP460

Data Sheet **July 1999** **File Number 2291.3**

20A, 500V, 0.270 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17465.

Ordering Information

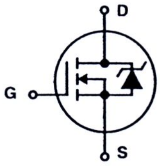
PART NUMBER	PACKAGE	BRAND
IRFP460	TO-247	IRFP460

NOTE: When ordering, use the entire part number.

Features

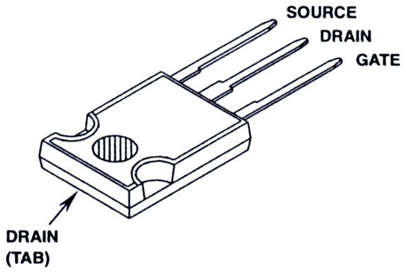
- 20A, 500V
- $r_{DS(ON)} = 0.270\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC STYLE TO-247



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

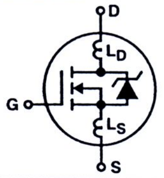
		IRFP460	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	500	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	500	V
Continuous Drain Current	I_D	20	A
$T_C = 100^oC$	I_D	12	A
Pulsed Drain Current (Note 3)	I_{DM}	80	A
Gate to Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation	P_D	250	W
Linear Derating Factor		2.0	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4)	E_{AS}	960	mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^{o}C
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

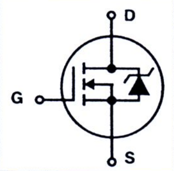
NOTE:

1. $T_J = 25^oC$ to $T_J = 125^oC$.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 10)	500	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$	2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, $V_{GS} = 0V$	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, $V_{GS} = 0V$, $T_J = 125^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = 10V$	20	-	-	A
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$I_D = 11A$, $V_{GS} = 10V$ (Figures 8, 9)	-	0.24	0.27	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \geq 50V$, $I_{DS} > 11A$ (Figure 12)	13	19	-	S
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 250V$, $I_D = 21A$, $R_{GS} = 4.3\Omega$, $R_D = 12\Omega$, $V_{GS} = 10V$ MOSFET Switching Times are Essentially Independent of Operating Temperature	-	23	35	ns
Rise Time	t_r		-	81	120	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	85	130	ns
Fall Time	t_f		-	65	98	ns
Total Gate Charge (Gate to Source + Gate-Drain)	$Q_{g(TOT)}$	$V_{GS} = 10V$, $I_D = 21A$, V_{DS} = 0.8 x Rated BV_{DSS}, $I_{G(REF)} = 1.5mA$ (Figure 14). Gate Charge is Essentially Independent of OperatingTemperature	-	120	190	nC
Gate to Source Charge	Q_{gs}		-	18	-	nC
Gate to Drain "Miller" Charge	Q_{gd}		-	62	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 10)	-	4100	-	pF
Output Capacitance	C_{OSS}		-	480	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	84	-	pF
Internal Drain Inductance	L_D	Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad	-	13	-	nH
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.50	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier		-	-	20	A
Pulse Source to Drain Current (Note 3)	I_{SDM}			-	-	80	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 21A$, $V_{GS} = 0V$ (Figure 13)		-	-	1.8	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 21A$, $dI_{SD}/dt = 100A/\mu s$		280	580	1200	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 21A$, $dI_{SD}/dt = 100A/\mu s$		3.8	8.1	18	μC

NOTES:

2. Pulse test: pulse width ≤ 300μs, duty cycle ≤ 2%.
3. Repetitive rating: pulse width limited by Max junction temperature. See Transient Thermal Impedance curve (Figure 3).
4. $V_{DD} = 50V$, starting $T_J = 25^oC$, $L = 4.3mH$, $R_{GS} = 25\Omega$, Peak $I_{AS} = 20A$.

Typical Performance Curves Unless Otherwise Specified

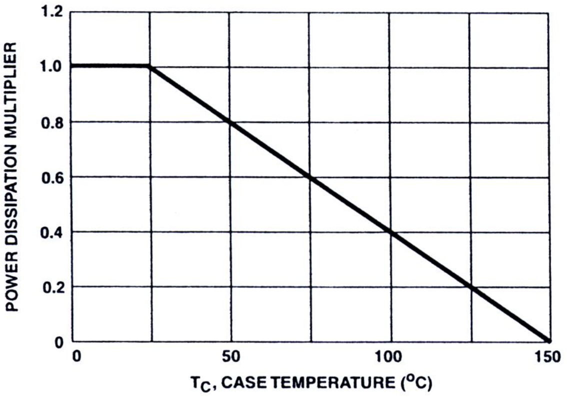


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

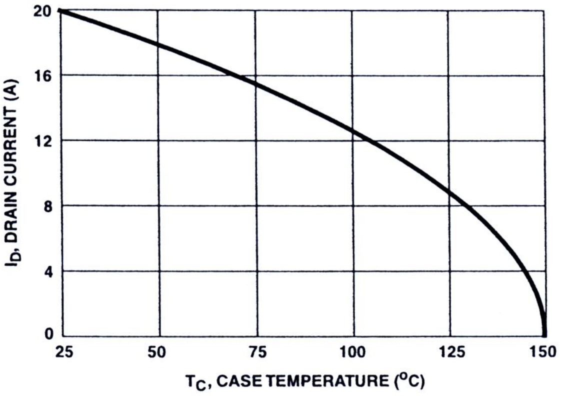
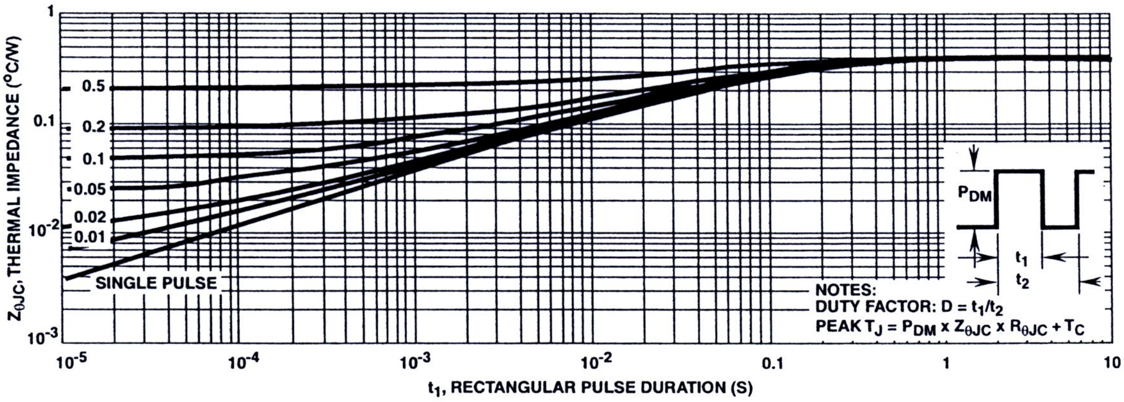


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE



NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

FIGURE 3. MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

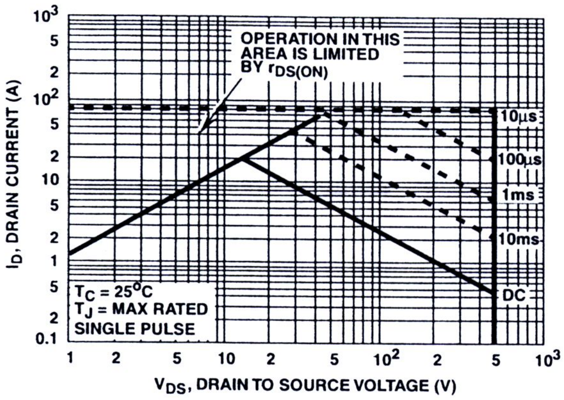


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

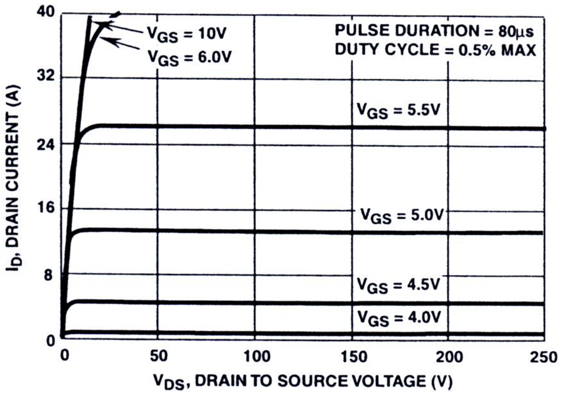


FIGURE 5. OUTPUT CHARACTERISTICS

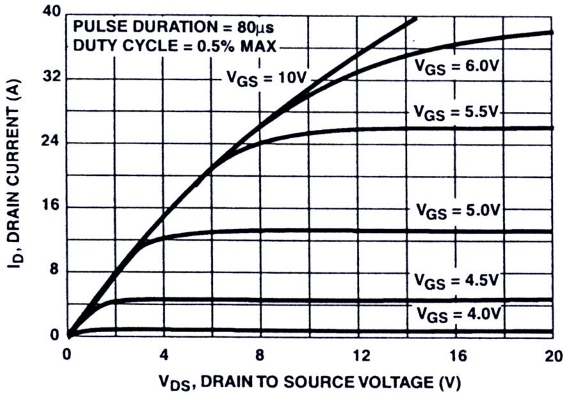


FIGURE 6. SATURATION CHARACTERISTICS

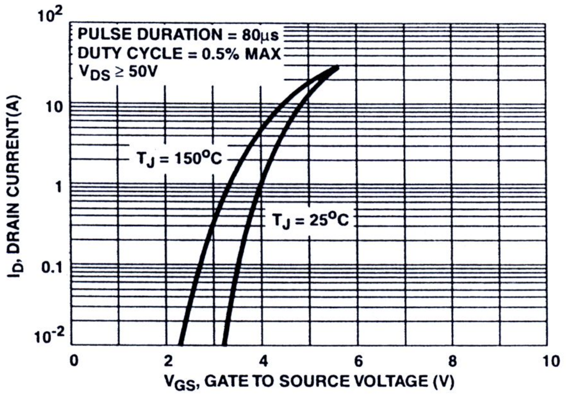


FIGURE 7. TRANSFER CHARACTERISTICS

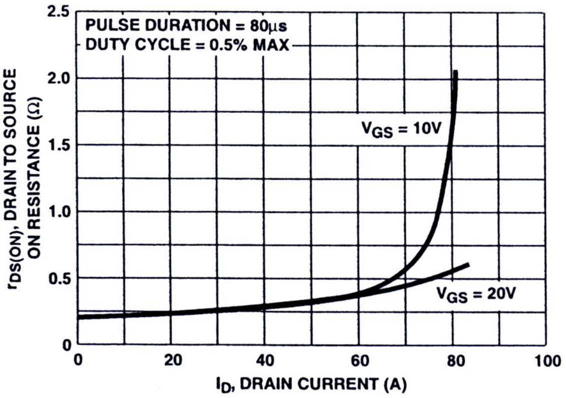


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

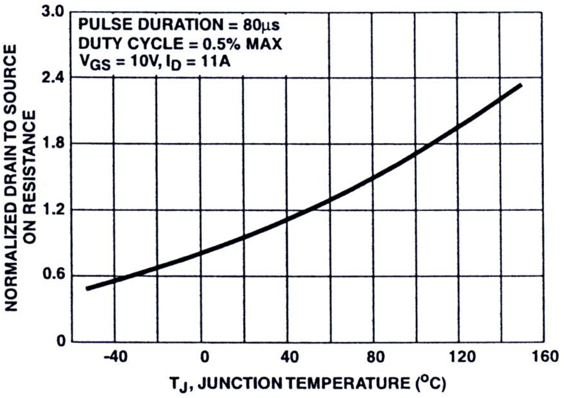


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

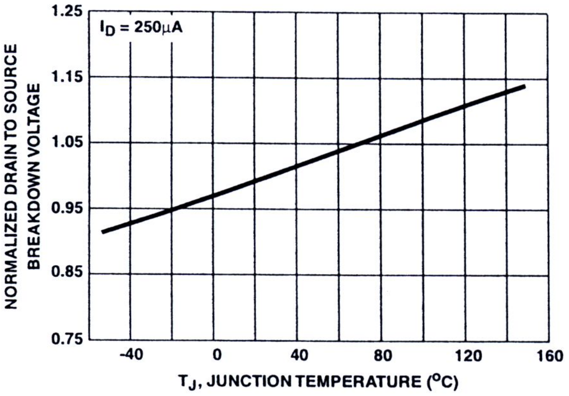


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

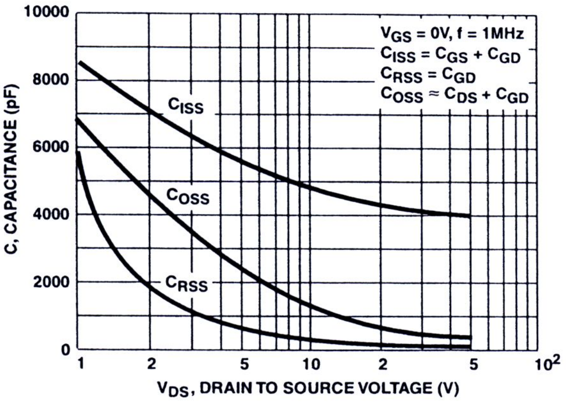


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

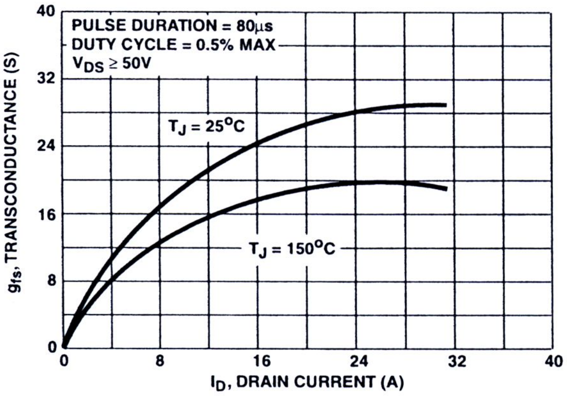


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

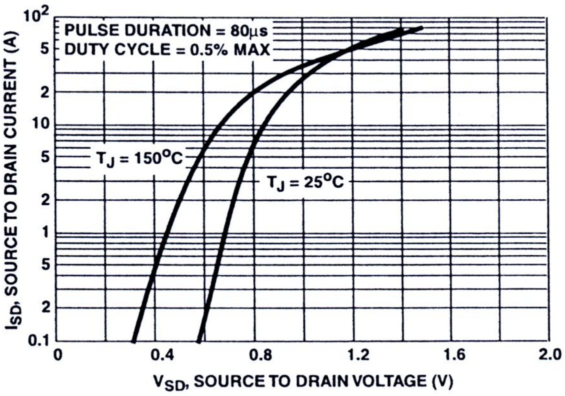


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

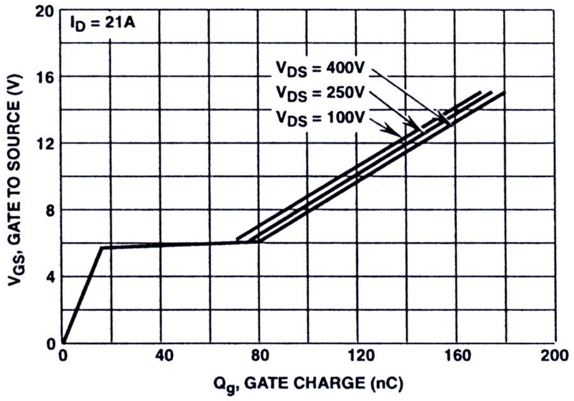


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

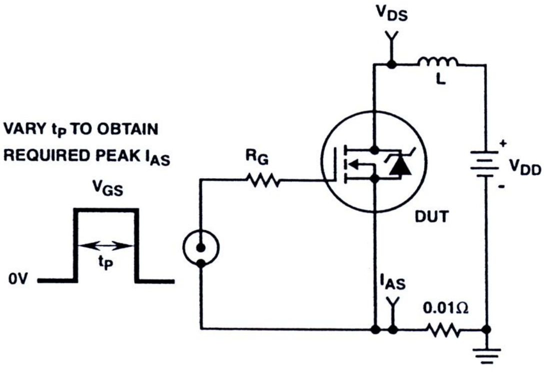


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

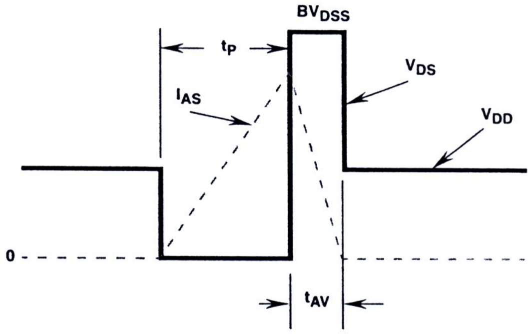


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

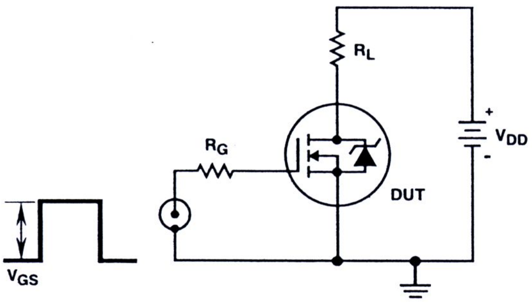


FIGURE 17. SWITCHING TIME TEST CIRCUIT

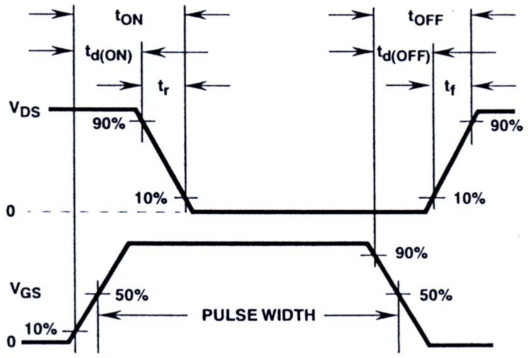


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

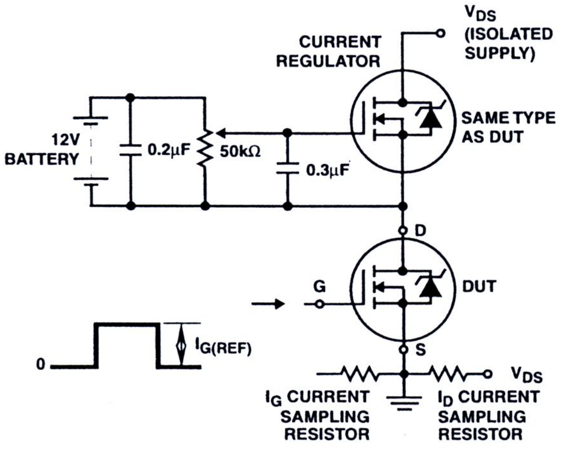


FIGURE 19. GATE CHARGE TEST CIRCUIT

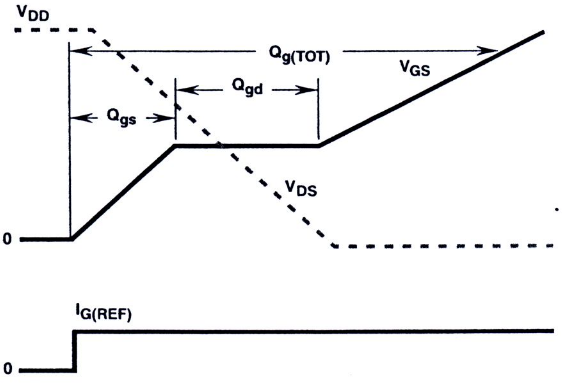


FIGURE 20. GATE CHARGE WAVEFORMS

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H

ภาคผนวก ค
ดาต้าชีตไอซีเบอร์ TL494

TL494

SWITCHMODE™ Pulse Width Modulation Control Circuit

The TL494 is a fixed frequency, pulse width modulation control circuit designed primarily for SWITCHMODE power supply control.

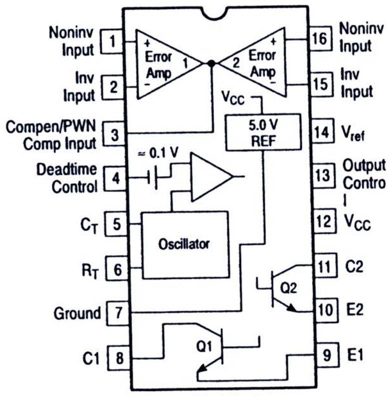
- Complete Pulse Width Modulation Control Circuitry
- On–Chip Oscillator with Master or Slave Operation
- On–Chip Error Amplifiers
- On–Chip 5.0 V Reference
- Adjustable Deadtime Control
- Uncommitted Output Transistors Rated to 500 mA Source or Sink
- Output Control for Push–Pull or Single–Ended Operation
- Undervoltage Lockout

MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	TL494C	TL494I	Unit
Power Supply Voltage	V_{CC}	42		V
Collector Output Voltage	V_{C1}, V_{C2}	42		V
Collector Output Current (Each transistor) (Note 1.)	I_{C1}, I_{C2}	500		mA
Amplifier Input Voltage Range	V_{IR}	–0.3 to +42		V
Power Dissipation @ $T_A \leq 45°C$	P_D	1000		mW
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	80		°C/W
Operating Junction Temperature	T_J	125		°C
Storage Temperature Range	T_{stg}	–55 to +125		°C
Operating Ambient Temperature Range	T_A			°C
TL494C		0 to +70		
TL494I		–40 to +85		
Derating Ambient Temperature	T_A	45		°C

1. Maximum thermal limits must be observed.

PIN CONNECTIONS



(Top View)

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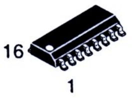
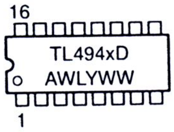
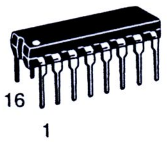
MARKING DIAGRAMS

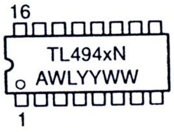


SO–16
D SUFFIX
CASE 751B





PDIP–16
N SUFFIX
CASE 648



x	=	C or I
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week

ORDERING INFORMATION

Device	Package	Shipping
TL494CD	SO–16	48 Units/Rail
TL494CDR2	SO–16	2500 Tape & Reel
TL494CN	PDIP–16	500 Units/Rail
TL494IN	PDIP–16	500 Units/Rail

July, 2000 – Rev. 2

Publication Order Number:
TL494/D

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	7.0	15	40	V
Collector Output Voltage	V_{C1}, V_{C2}	–	30	40	V
Collector Output Current (Each transistor)	I_{C1}, I_{C2}	–	–	200	mA
Amplified Input Voltage	V_{in}	–0.3	–	V_{CC} – 2.0	V
Current Into Feedback Terminal	I_{fb}	–	–	0.3	mA
Reference Output Current	I_{ref}	–	–	10	mA
Timing Resistor	R_T	1.8	30	500	kΩ
Timing Capacitor	C_T	0.0047	0.001	10	μF
Oscillator Frequency	f_{osc}	1.0	40	200	kHz

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 μF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

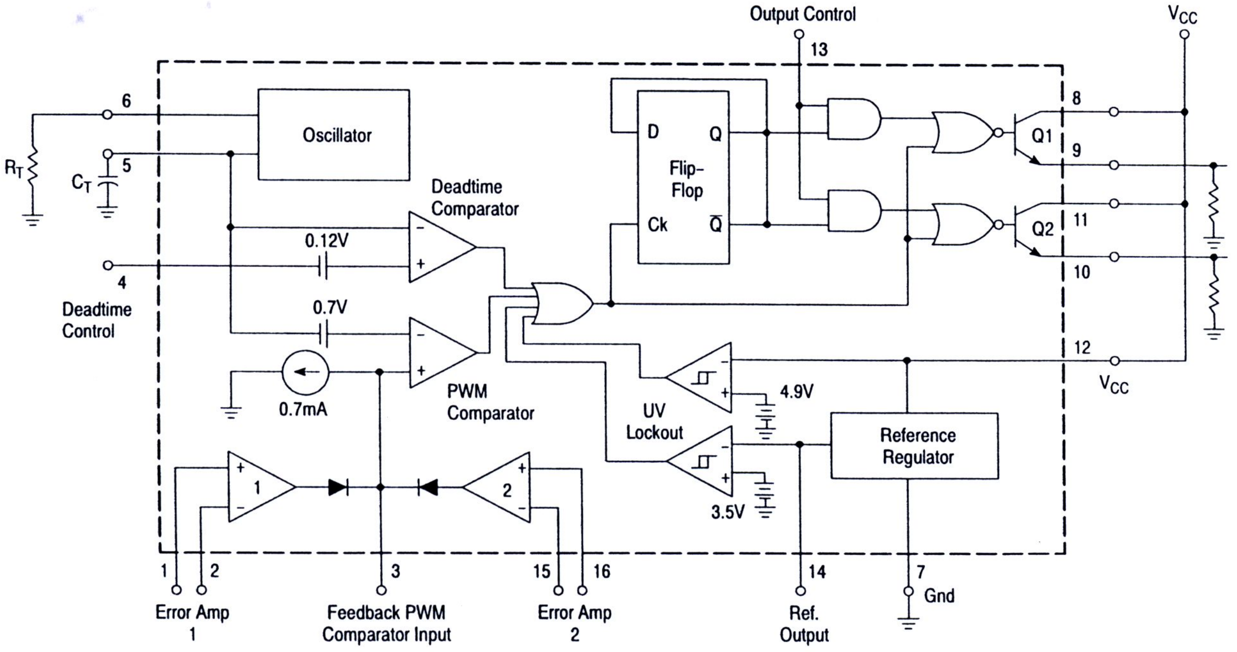
Characteristics	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Voltage (I_O = 1.0 mA)	V_{ref}	4.75	5.0	5.25	V
Line Regulation (V_{CC} = 7.0 V to 40 V)	Reg_{line}	–	2.0	25	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	–	3.0	15	mV
Short Circuit Output Current (V_{ref} = 0 V)	I_{SC}	15	35	75	mA
OUTPUT SECTION					
Collector Off–State Current (V_{CC} = 40 V, V_{CE} = 40 V)	$I_{C(off)}$	–	2.0	100	μA
Emitter Off–State Current V_{CC} = 40 V, V_C = 40 V, V_E = 0 V)	$I_{E(off)}$	–	–	–100	μA
Collector–Emitter Saturation Voltage (Note 2.)					V
Common–Emitter (V_E = 0 V, I_C = 200 mA)	$V_{sat(C)}$	–	1.1	1.3	
Emitter–Follower (V_C = 15 V, I_E = –200 mA)	$V_{sat(E)}$	–	1.5	2.5	
Output Control Pin Current					
Low State (V_{OC} ≤ 0.4 V)	I_{OCL}	–	10	–	μA
High State (V_{OC} = V_{ref})	I_{OCH}	–	0.2	3.5	mA
Output Voltage Rise Time	t_r				ns
Common–Emitter (See Figure 12)		–	100	200	
Emitter–Follower (See Figure 13)		–	100	200	
Output Voltage Fall Time	t_f				ns
Common–Emitter (See Figure 12)		–	25	100	
Emitter–Follower (See Figure 13)		–	40	100	

2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, C_T = 0.01 µF, R_T = 12 kΩ, unless otherwise noted.)
For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies, unless otherwise noted.

Characteristics	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage ($V_{O\ (Pin\ 3)}$ = 2.5 V)	V_{IO}	–	2.0	10	mV
Input Offset Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IO}	–	5.0	250	nA
Input Bias Current ($V_{O\ (Pin\ 3)}$ = 2.5 V)	I_{IB}	–	–0.1	–1.0	µA
Input Common Mode Voltage Range (V_{CC} = 40 V, T_A = 25°C)	V_{ICR}	–0.3 to V_{CC}–2.0			V
Open Loop Voltage Gain (ΔV_O = 3.0 V, V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	A_{VOL}	70	95	–	dB
Unity–Gain Crossover Frequency (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	f_{C-}	–	350	–	kHz
Phase Margin at Unity–Gain (V_O = 0.5 V to 3.5 V, R_L = 2.0 kΩ)	ϕ_m	–	65	–	deg.
Common Mode Rejection Ratio (V_{CC} = 40 V)	CMRR	65	90	–	dB
Power Supply Rejection Ratio (ΔV_{CC} = 33 V, V_O = 2.5 V, R_L = 2.0 kΩ)	PSRR	–	100	–	dB
Output Sink Current ($V_{O\ (Pin\ 3)}$ = 0.7 V)	I_{O-}	0.3	0.7	–	mA
Output Source Current ($V_{O\ (Pin\ 3)}$ = 3.5 V)	I_{O+}	2.0	–4.0	–	mA
PWM COMPARATOR SECTION (Test Circuit Figure 11)					
Input Threshold Voltage (Zero Duty Cycle)	V_{TH}	–	2.5	4.5	V
Input Sink Current ($V_{(Pin\ 3)}$ = 0.7 V)	I_{I-}	0.3	0.7	–	mA
DEADTIME CONTROL SECTION (Test Circuit Figure 11)					
Input Bias Current (Pin 4) ($V_{Pin\ 4}$ = 0 V to 5.25 V)	$I_{IB\ (DT)}$	–	–2.0	–10	µA
Maximum Duty Cycle, Each Output, Push–Pull Mode ($V_{Pin\ 4}$ = 0 V, C_T = 0.01 µF, R_T = 12 kΩ) ($V_{Pin\ 4}$ = 0 V, C_T = 0.001 µF, R_T = 30 kΩ)	DC_{max}	 45 –	 48 45	 50 50	%
Input Threshold Voltage (Pin 4) (Zero Duty Cycle) (Maximum Duty Cycle)	V_{th}	 – 0	 2.8 –	 3.3 –	V
OSCILLATOR SECTION					
Frequency (C_T = 0.001 µF, R_T = 30 kΩ)	f_{osc}	–	40	–	kHz
Standard Deviation of Frequency* (C_T = 0.001 µF, R_T = 30 kΩ)	σf_{osc}	–	3.0	–	%
Frequency Change with Voltage (V_{CC} = 7.0 V to 40 V, T_A = 25°C)	Δf_{osc} (ΔV)	–	0.1	–	%
Frequency Change with Temperature (ΔT_A = T_{low} to T_{high}) (C_T = 0.01 µF, R_T = 12 kΩ)	Δf_{osc} (ΔT)	–	–	12	%
UNDERVOLTAGE LOCKOUT SECTION					
Turn–On Threshold (V_{CC} increasing, I_{ref} = 1.0 mA)	V_{th}	5.5	6.43	7.0	V
TOTAL DEVICE					
Standby Supply Current (Pin 6 at V_{ref}, All other inputs and outputs open) (V_{CC} = 15 V) (V_{CC} = 40 V)	I_{CC}	 – –	 5.5 7.0	 10 15	mA
Average Supply Current (C_T = 0.01 µF, R_T = 12 kΩ, $V_{(Pin\ 4)}$ = 2.0 V) (V_{CC} = 15 V) (See Figure 12)		–	7.0	–	mA

* Standard deviation is a measure of the statistical distribution about the mean as derived from the formula, $\sigma \sqrt{\frac{\sum_{n=1}^{N} (X_n - \overline{X})^2}{N-1}}$



This device contains 46 active transistors.

Figure 1. Representative Block Diagram

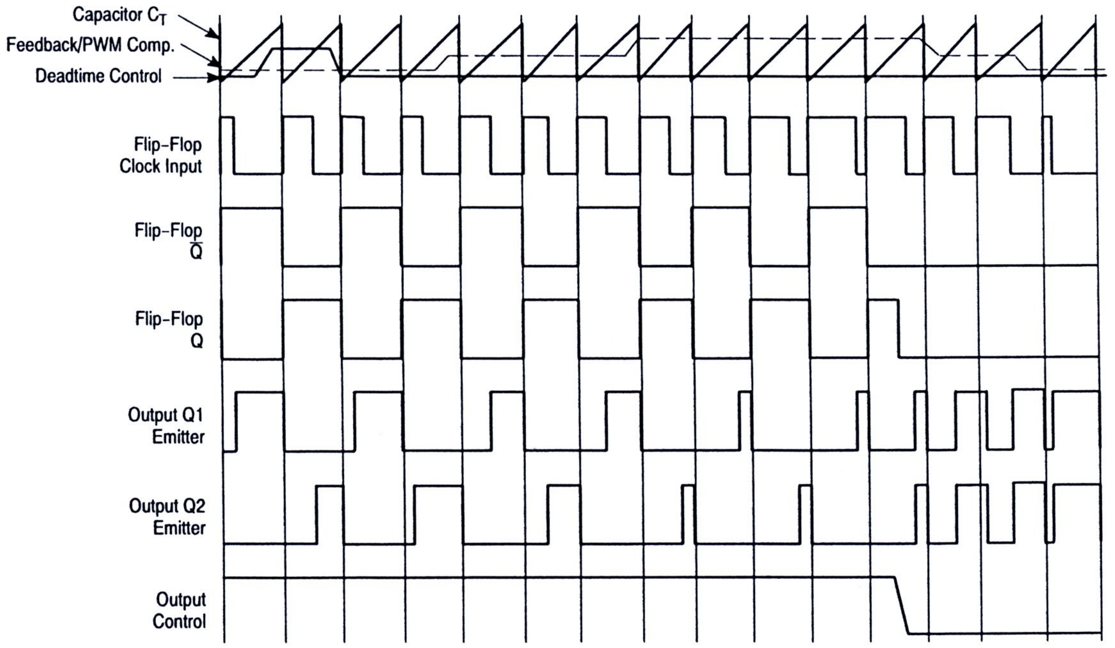


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

Description

The TL494 is a fixed–frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (See Figure 1.) An internal–linear sawtooth oscillator is frequency– programmable by two external components, R_T and C_T. The approximate oscillator frequency is determined by:

$$f_{osc} \approx \frac{1.1}{R_T \bullet C_T}$$

For more information refer to Figure 3.

Output pulse width modulation is accomplished by comparison of the positive sawtooth waveform across capacitor C_T to either of two control signals. The NOR gates, which drive output transistors Q1 and Q2, are enabled only when the flip–flop clock–input line is in its low state. This happens only during that portion of time when the sawtooth voltage is greater than the control signals. Therefore, an increase in control–signal amplitude causes a corresponding linear decrease of output pulse width. (Refer to the Timing Diagram shown in Figure 2.)

The control signals are external inputs that can be fed into the deadtime control, the error amplifier inputs, or the feedback input. The deadtime control comparator has an effective 120 mV input offset which limits the minimum output deadtime to approximately the first 4% of the sawtooth–cycle time. This would result in a maximum duty cycle on a given output of 96% with the output control grounded, and 48% with it connected to the reference line. Additional deadtime may be imposed on the output by setting the deadtime–control input to a fixed voltage, ranging between 0 V to 3.3 V.

Functional Table

Input/Output Controls	Output Function	$\frac{f_{out}}{f_{osc}}$ =
Grounded	Single–ended PWM @ Q1 and Q2	1.0
@ V_{ref}	Push–pull Operation	0.5

The pulse width modulator comparator provides a means for the error amplifiers to adjust the output pulse width from the maximum percent on–time, established by the deadtime control input, down to zero, as the voltage at the feedback pin varies from 0.5 V to 3.5 V. Both error amplifiers have a common mode input range from –0.3 V to (V_{CC} – 2V), and may be used to sense power–supply output voltage and current. The error–amplifier outputs are active high and are ORed together at the noninverting input of the pulse–width modulator comparator. With this configuration, the amplifier that demands minimum output on time, dominates control of the loop.

When capacitor C_T is discharged, a positive pulse is generated on the output of the deadtime comparator, which clocks the pulse–steering flip–flop and inhibits the output transistors, Q1 and Q2. With the output–control connected to the reference line, the pulse–steering flip–flop directs the modulated pulses to each of the two output transistors alternately for push–pull operation. The output frequency is equal to half that of the oscillator. Output drive can also be taken from Q1 or Q2, when single–ended operation with a maximum on–time of less than 50% is required. This is desirable when the output transformer has a ringback winding with a catch diode used for snubbing. When higher output–drive currents are required for single–ended operation, Q1 and Q2 may be connected in parallel, and the output–mode pin must be tied to ground to disable the flip–flop. The output frequency will now be equal to that of the oscillator.

The TL494 has an internal 5.0 V reference capable of sourcing up to 10 mA of load current for external bias circuits. The reference has an internal accuracy of ±5.0% with a typical thermal drift of less than 50 mV over an operating temperature range of 0° to 70°C.

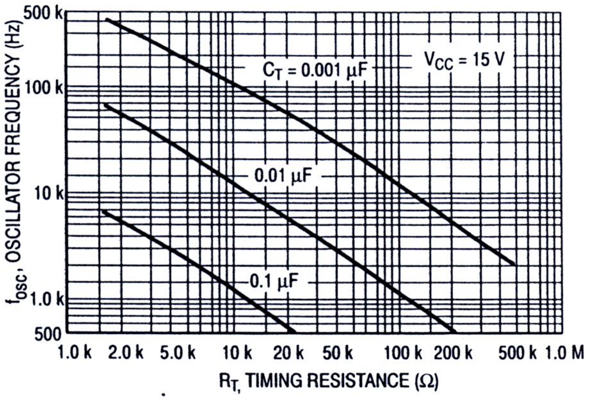


Figure 3. Oscillator Frequency versus Timing Resistance

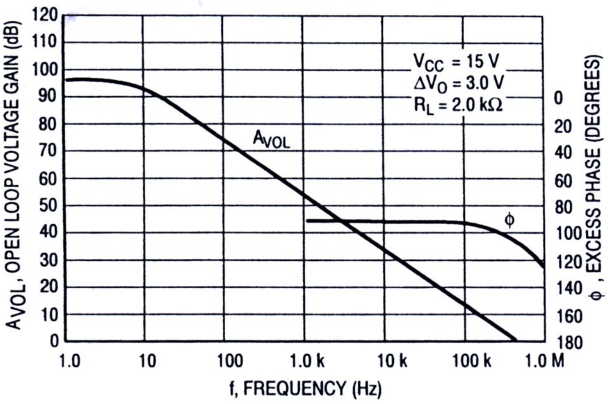


Figure 4. Open Loop Voltage Gain and Phase versus Frequency

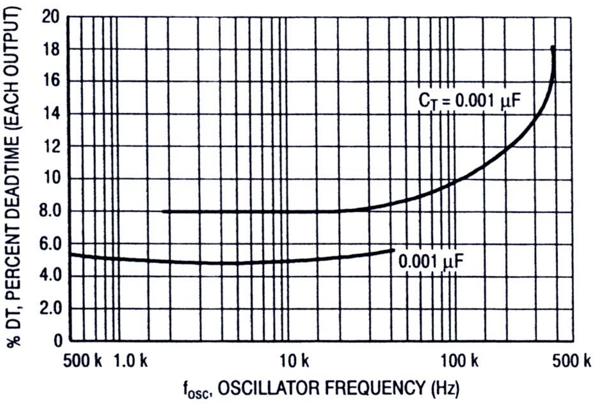


Figure 5. Percent Deadtime versus Oscillator Frequency

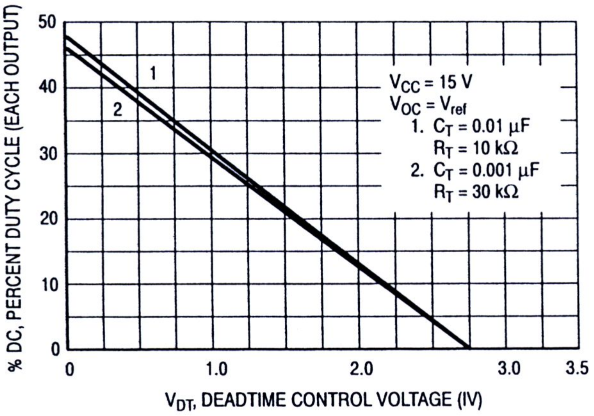


Figure 6. Percent Duty Cycle versus Deadtime Control Voltage

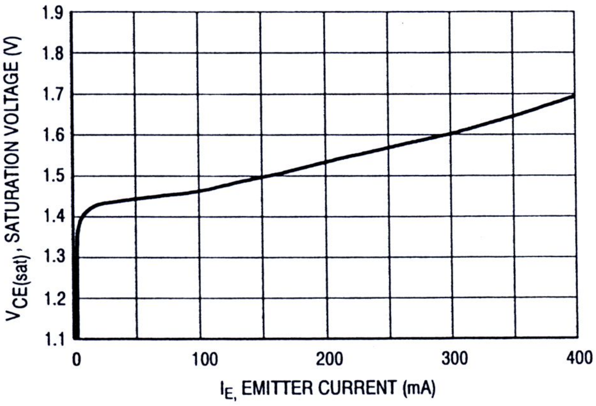


Figure 7. Emitter–Follower Configuration Output Saturation Voltage versus Emitter Current

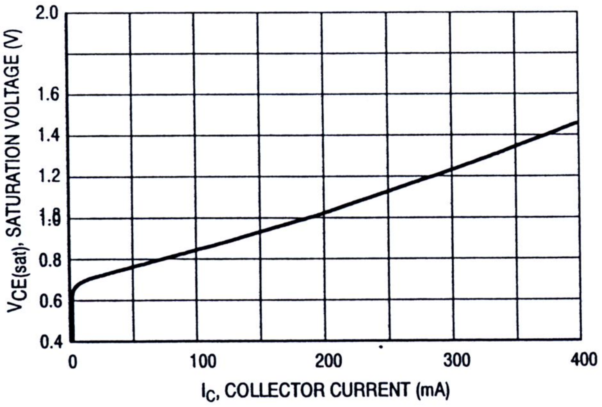


Figure 8. Common–Emitter Configuration Output Saturation Voltage versus Collector Current

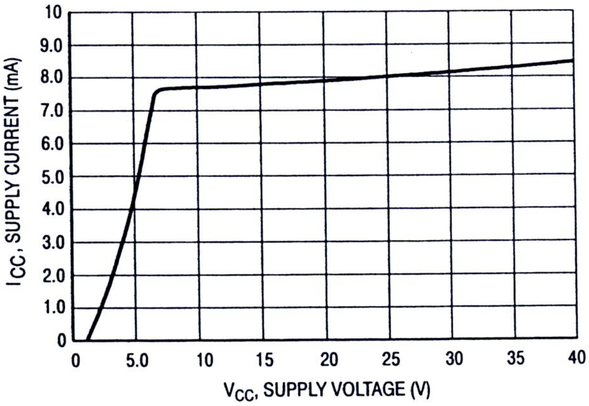


Figure 9. Standby Supply Current versus Supply Voltage

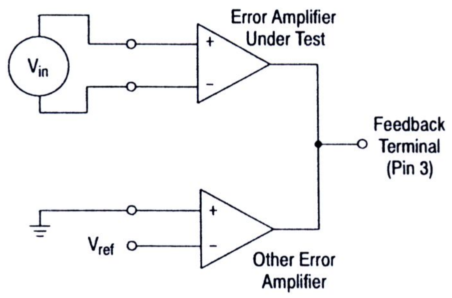


Figure 10. Error–Amplifier Characteristics

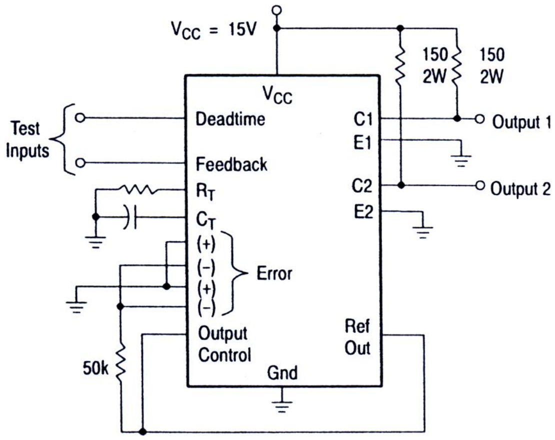


Figure 11. Deadtime and Feedback Control Circuit

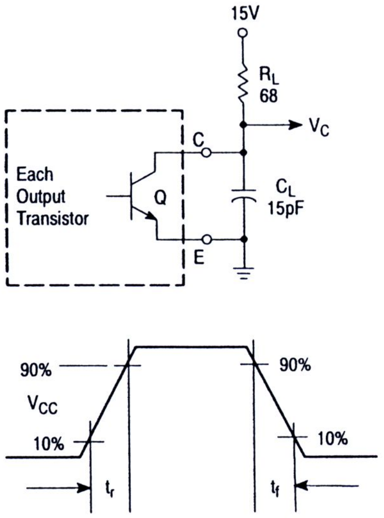


Figure 12. Common–Emitter Configuration
Test Circuit and Waveform

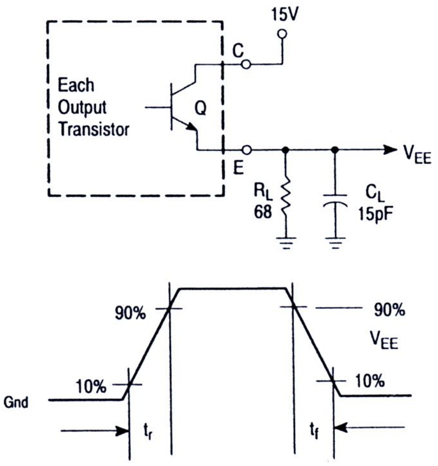
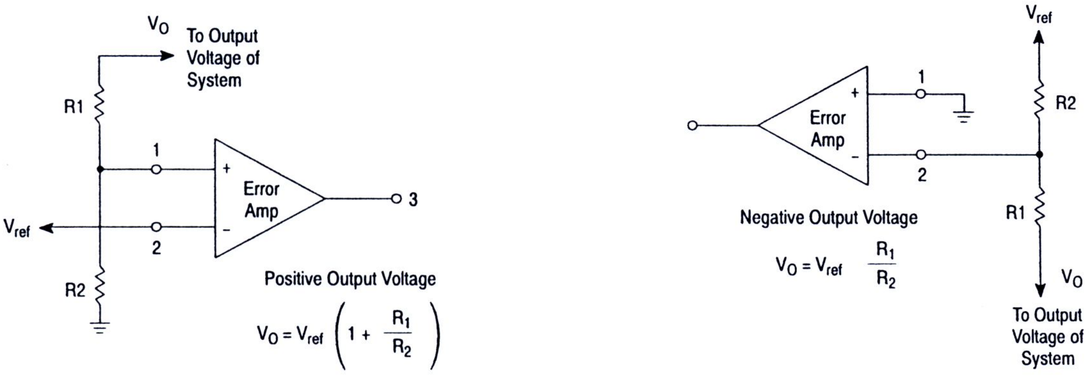


Figure 13. Emitter–Follower Configuration
Test Circuit and Waveform



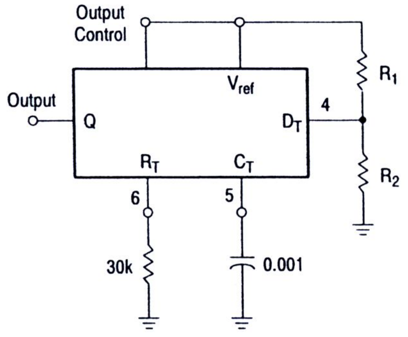
Positive Output Voltage

$$V_O = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$

Negative Output Voltage

$$V_O = V_{ref}\frac{R_1}{R_2}$$

Figure 14. Error–Amplifier Sensing Techniques



$$\text{Max. \% on Time, each output} \approx 45 - \left(\frac{80}{1 + \frac{R1}{R2}}\right)$$

Figure 15. Deadtime Control Circuit

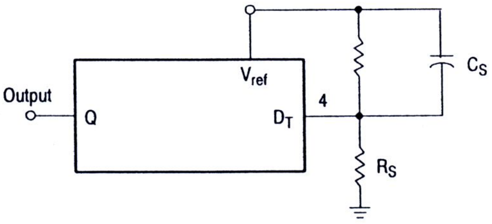


Figure 16. Soft–Start Circuit

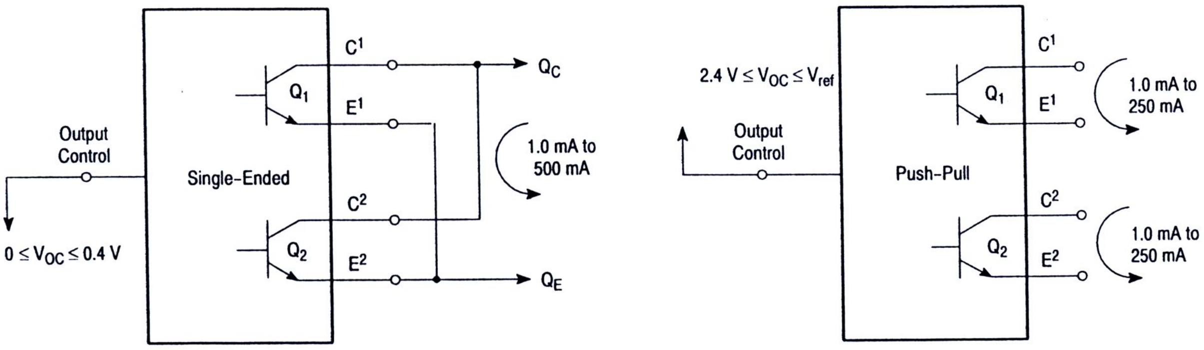


Figure 17. Output Connections for Single–Ended and Push–Pull Configurations

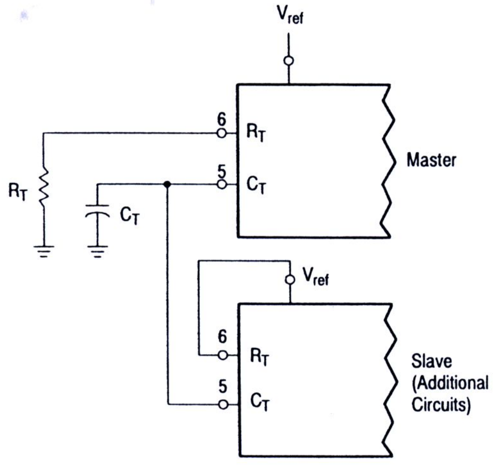


Figure 18. Slaving Two or More Control Circuits

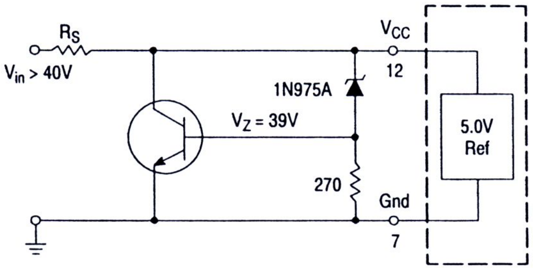
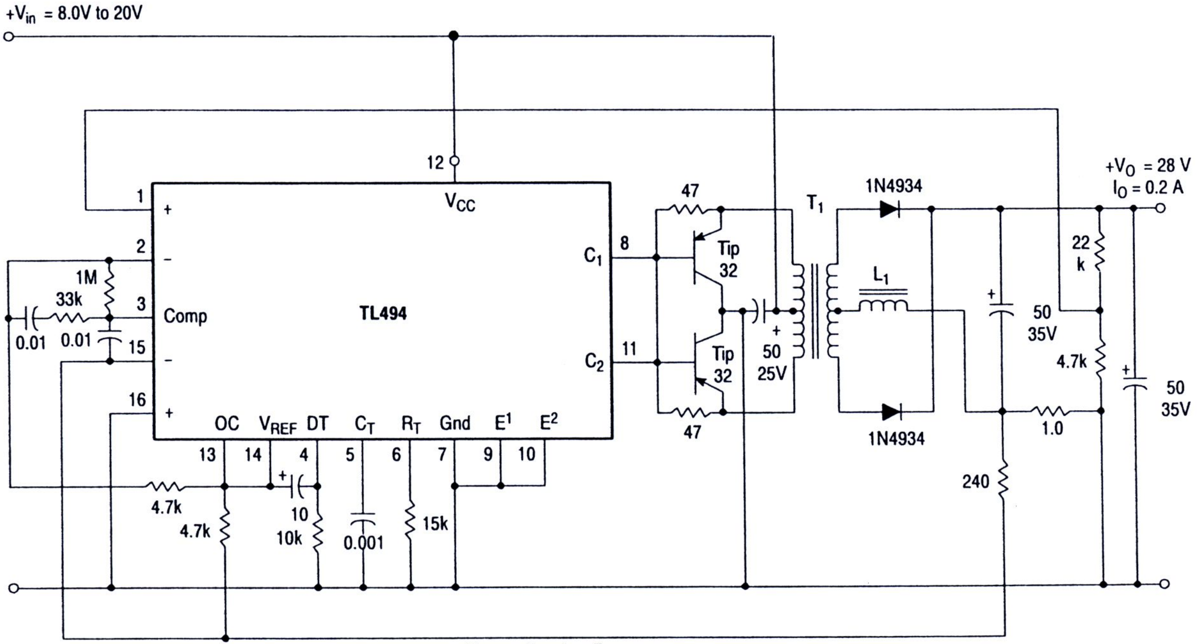


Figure 19. Operation with V_{in} > 40 V Using External Zener



All capacitors in µF

Figure 20. Pulse Width Modulated Push–Pull Converter

Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 40 V	14 mV 0.28%
Load Regulation	V_{in} = 28 V, I_O = 1.0 mA to 1.0 A	3.0 mV 0.06%
Output Ripple	V_{in} = 28 V, I_O = 1.0 A	65 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 28 V, I_O = 1.0 A	71%

L1 – 3.5 mH @ 0.3 A
T1 – Primary: 20T C.T. #28 AWG
Secondary: 120T C.T. #36 AWG
Core: Ferroxcube 1408P-L00-3CB

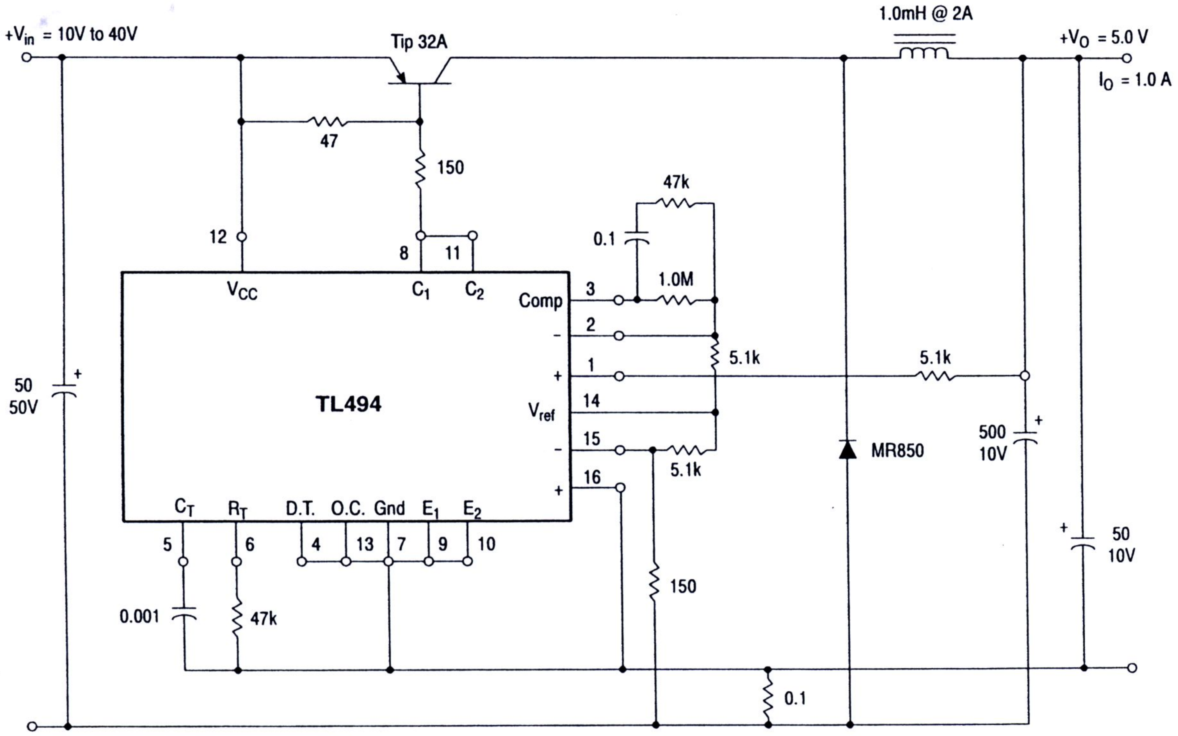
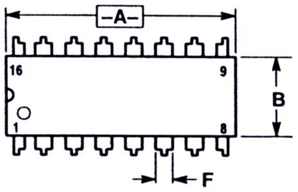


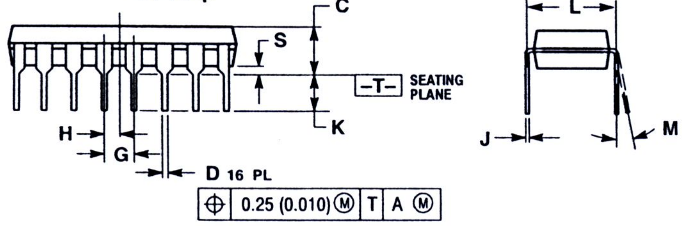
Figure 21. Pulse Width Modulated Step–Down Converter

Test	Conditions	Results
Line Regulation	V_{in} = 8.0 V to 40 V	3.0 mV 0.01%
Load Regulation	V_{in} = 12.6 V, I_O = 0.2 mA to 200 mA	5.0 mV 0.02%
Output Ripple	V_{in} = 12.6 V, I_O = 200 mA	40 mV pp P.A.R.D.
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	250 mA
Efficiency	V_{in} = 12.6 V, I_O = 200 mA	72%

PACKAGE DIMENSIONS

PDIP–16
N SUFFIX
CASE 648–08
ISSUE R

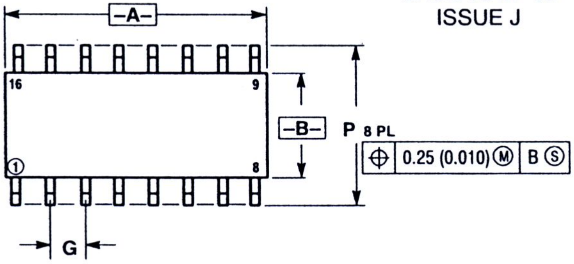


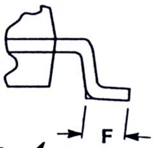


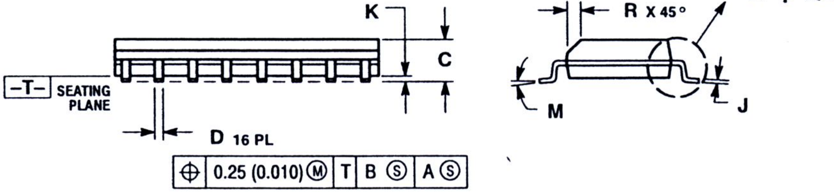
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

SO–16
D SUFFIX
CASE 751B–05
ISSUE J







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2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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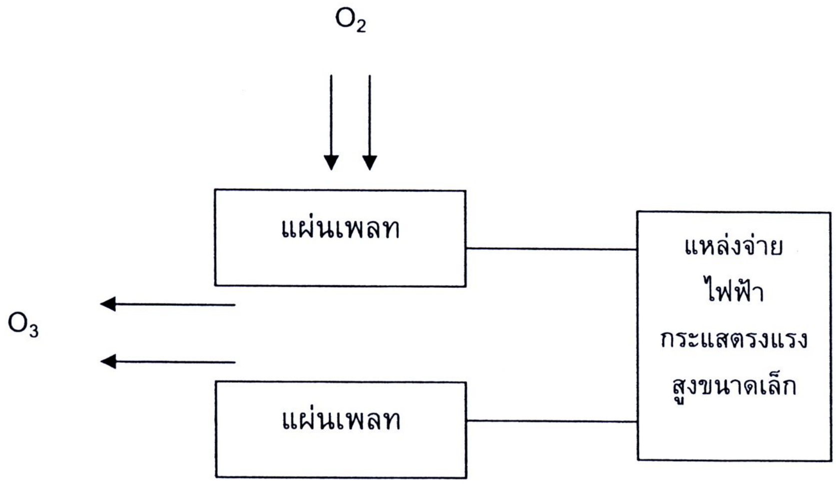
ภาคผนวก ง

การออกแบบและเลือกใช้แผ่นเพลท

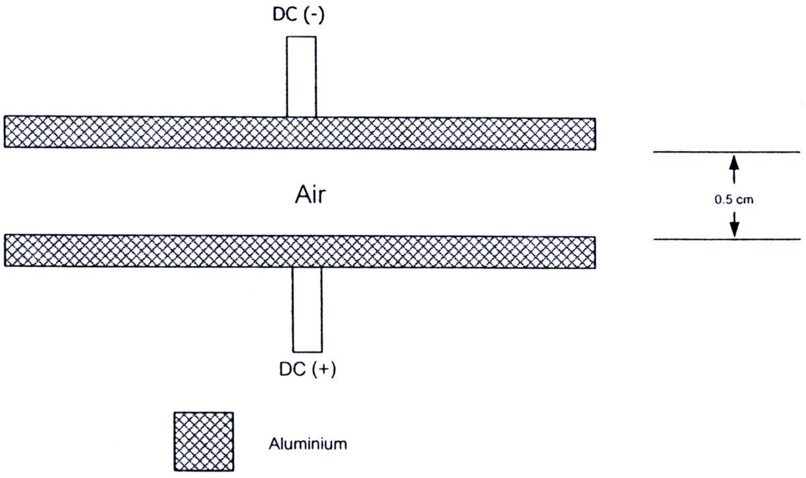
(โหลดของแหล่งจ่ายไฟฟ้ากระแสตรงแรงสูง)

การออกแบบและเลือกใช้แผ่นเพลท (โหลดของแหล่งจ่ายไฟฟ้ากระแสตรงแรงสูง)

จากรูปที่ ง.1 ได้ออกแบบและเลือกใช้แผ่นอะลูมิเนียมมาใช้เป็นแผ่นเพลท เพราะแผ่นอะลูมิเนียมสามารถนำไฟฟ้าได้ดี น้ำหนักเบา และราคาไม่แพง โดยทำการป้อนไฟฟ้ากระแสตรงแรงสูงให้กับแผ่นเพลทจนทำให้อากาศโดยรอบแตกตัว (การทำให้อากาศแตกตัวจะทำให้เกิดก๊าซโอโซนออกมาด้วย) แต่ไม่ควรไม่ทำให้เกิดการเบรคดาวน์ เพราะการเบรคดาวน์จะส่งผลทำให้หม้อแปลง ฟลายแบคในวงจรแหล่งจ่ายไฟฟ้ากระแสตรงแรงสูงพังเสียหาย อันเนื่องมาจากการเสื่อมสภาพของฉนวนที่อยู่ภายในหม้อแปลงฟลายแบค



รูปที่ ง.1 โครงสร้างของแผ่นเพลท (แผ่นอะลูมิเนียม)



รูปที่ ง.2 ลักษณะแผ่นเพลทที่เลือกใช้

ปริมาตรอากาศในแกป = กว้าง x ยาว x สูง

= (0.005 m x 0.13 m x 0.25 m) x 16 ชุด

= $260 \times 10^{-5}\ m^3$

= $2600\ cm^3$

ที่ย่านพลังงานไฟฟ้า 1.172 kWh/m^3 $= 1.172 \times 10^3 \times 260 \times 10^{-5}$

$= 3.0472$ Wh

ถึงย่านพลังงานไฟฟ้า 1.62 kWh/m^3 $= 1.62 \times 10^3 \times 260 \times 10^{-5}$

$= 4.212$ Wh

พลังงานไฟฟ้าในการผลิตเกิดเนื่องจากสนามไฟฟ้า E สามารถหาได้จาก

$$W = \frac{1}{2}\int \varepsilon E^2 dv \qquad (ง.1)$$

$$E = \sqrt{\frac{2W}{\varepsilon V}} \qquad (ง.2)$$

$$E = \sqrt{\frac{2(3.0472)}{(8.854x10^{-12})(2600)}}$$

$$E = 16.27kV\ /cm$$

ถึงค่า

$$E = \sqrt{\frac{2(4.212)}{(8.854x10^{-12})(2600)}}$$

$$E = 19.129kV\ /cm$$

ที่ระยะห่างระหว่างแผ่นอะลูมิเนียม (d) = 0.5 cm, กำหนดให้แฟคเตอร์ของสนามไฟฟ้า (η^*)เท่ากับ 20%

$$V_i = E_i \times d \times \eta^* \qquad (ง.3)$$

ที่ E_{max} = 16.27 kV/cm $V_i = 16.27kV \times 0.5 \times 0.2$

$$V_i = 1.627kV$$

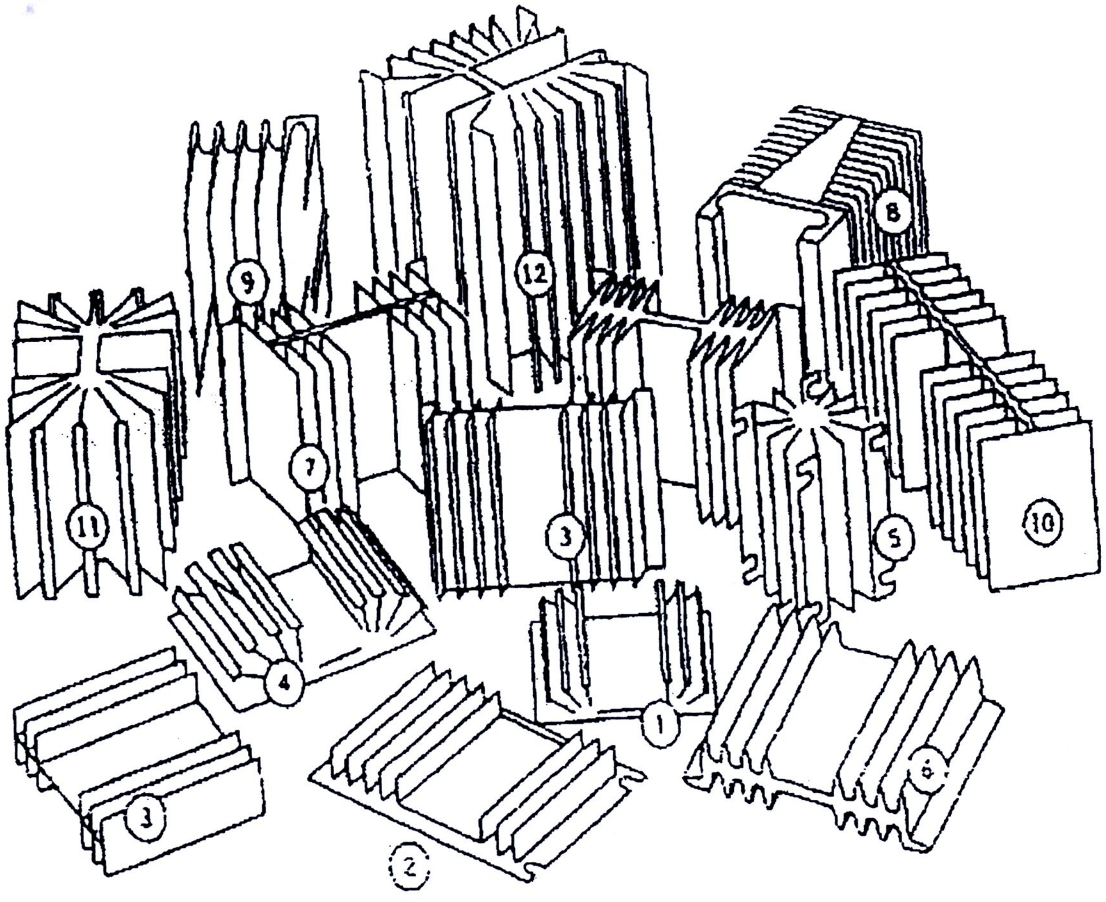
ที่ E_{max} = 19.129 kV/cm $V_i = 19.27kV \times 0.5 \times 0.2$

$$V_i = 1.927kV$$

ดังนั้น ย่านแรงดันไฟฟ้าที่ทำให้เริ่มเกิดอากาศแตกตัว คือ 1.627 – 1.927 kV ย่านสนามไฟฟ้าที่ใช้ คือ 16.27 – 19.129 kV/cm และย่านพลังงานไฟฟ้า คือ 3.0472 – 4.212 Wh

ภาคผนวก จ

ขนาดแผ่นระบายความร้อนของเพาเวอร์มอสเฟต



Heat Sink No.	1	2	3	4	5	6	7	8	9	10	11	12
$R_{\theta sa}$ (°C / W)	3.2	2.3	2.2	-	2.1	1.7	1.3	1.3	1.25	1.2	0.8	0.65
Vol.(cm^3)	76	99	181	-	198	298	435	675	608	634	695	1311

ภาคผนวก ฉ

ดาต้าชีตไดโอด เบอร์ MUR860

FAIRCHILD
SEMICONDUCTOR®

MUR840, MUR860, RURP840, RURP860

Data Sheet ***January 2002***

8A, 400V - 600V Ultrafast Diodes

The MUR840, MUR860, RURP840 and RURP860 are low forward voltage drop ultrafast recovery rectifiers (t_{rr} < 60ns). They use a glass-passivated ion-implanted, epitaxial construction.

These devices are intended for use as output rectifiers and flywheel diodes in a variety of high-frequency pulse-width modulated switching regulators. Their low stored charge and attendant fast reverse-recovery behavior minimize electrical noise generation and in many circuits markedly reduce the turn-on dissipation of the associated power switching transistors.

Formerly developmental type TA09616.

Ordering Information

PART NUMBER	PACKAGE	BRAND
MUR840	TO-220AC	MUR840
RURP840	TO-220AC	RURP840
MUR860	TO-220AC	MUR860
RURP860	TO-220AC	RURP860

NOTE: When ordering, use the entire part number.

Symbol

Features

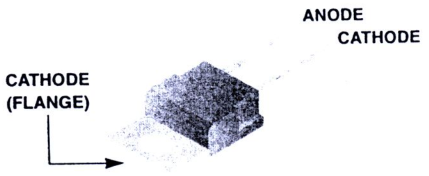
- Ultrafast with Soft Recovery . . . . <60ns
- Operating Temperature. . . . . 175°C
- Reverse Voltage 600V
- Avalanche Energy Rated
- Planar Construction

Applications

- Switching Power Supplies
- Power Switching Circuits
- General Purpose

Packaging

JEDEC TO-220AC



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		MUR840 RURP840	**MUR860 RURP860**	**UNITS**
Peak Repetitive Reverse Voltage	V_{RRM}	400	600	V
Working Peak Reverse Voltage	V_{RWM}	400	600	V
DC Blocking Voltage	V_R	400	600	V
Average Rectified Forward Current ($T_C = 155^oC$)	$I_{F(AV)}$	8	8	A
Repetitive Peak Surge Current (Square Wave, 20kHz)	I_{FRM}	16	16	A
Nonrepetitive Peak Surge Current (Halfwave, 1 Phase, 60Hz)	I_{FSM}	100	100	A
Maximum Power Dissipation	P_D	75	75	W
Avalanche Energy (See Figures 10 and 11)	E_{AVL}	20	20	mJ
Operating and Storage Temperature	T_{STG}, T_J	-65 to 175	-65 to 175	°C
Maximum Lead Temperature for Soldering				
Leads at 0.063 in. (1.6mm) from case for 10s	T_L	300	300	°C
Package Body for 10s, see Tech Brief 334	T_{PKG}	260	260	°C

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

SYMBOL	TEST CONDITION	MUR840, RURP840			MUR860, RURP860			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
V_F	$I_F = 8A$	-	-	1.3	-	-	1.5	V
	$I_F = 8A$, $T_C = 150^oC$	-	-	1.0	-	-	1.2	V
I_R	$V_R = 400V$	-	-	100	-	-	-	μA
	$V_R = 600V$	-	-	-	-	-	100	μA
	$V_R = 400V$, $T_C = 150^oC$	-	-	500	-	-	-	μA
	$V_R = 600V$, $T_C = 150^oC$	-	-	-	-	-	500	μA
t_{rr}	$I_F = 1A$, $dI_F/dt = 200A/\mu s$	-	-	60	-	-	60	ns
	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	-	70	-	-	70	ns
t_a	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	32	-	-	32	-	ns
t_b	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	21	-	-	21	-	ns
Q_{RR}	$I_F = 8A$, $dI_F/dt = 200A/\mu s$	-	195	-	-	195	-	nC
C_J	$V_R = 10V$, $I_F = 0A$	-	25	-	-	25	-	pF
$R_{\theta JC}$		-	-	2	-	-	2	$^oC/W$

DEFINITIONS

V_F = Instantaneous forward voltage (pw = 300μs, D = 2%).

I_R = Instantaneous reverse current.

t_{rr} = Reverse recovery time (See Figure 9), summation of $t_a + t_b$.

t_a = Time to reach peak reverse current (See Figure 9).

t_b = Time from peak I_{RM} to projected zero crossing of I_{RM} based on a straight line from peak I_{RM} through 25% of I_{RM} (See Figure 9).

Q_{RR} = Reverse recovery charge.

C_J = Junction Capacitance.

$R_{\theta JC}$ = Thermal resistance junction to case.

pw = pulse width.

D = duty cycle.

Typical Performance Curves

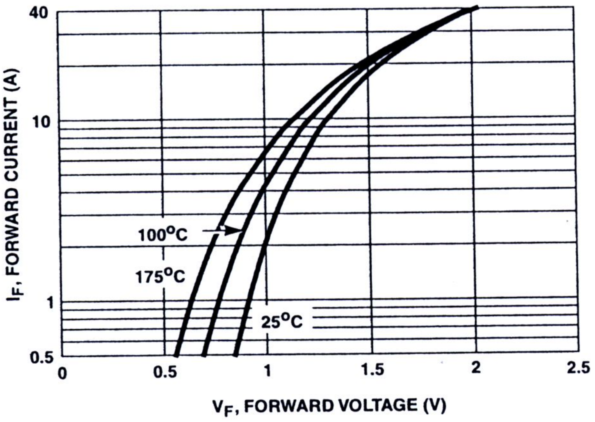


FIGURE 1. FORWARD CURRENT vs FORWARD VOLTAGE

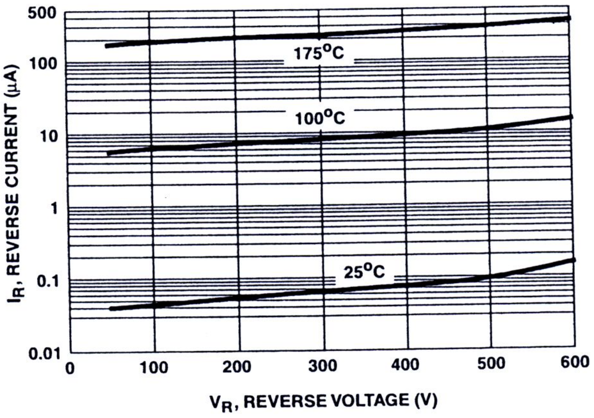


FIGURE 2. REVERSE CURRENT vs REVERSE VOLTAGE

Typical Performance Curves (Continued)

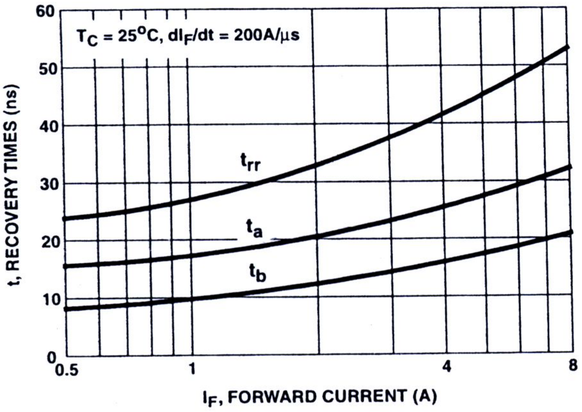


FIGURE 3. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

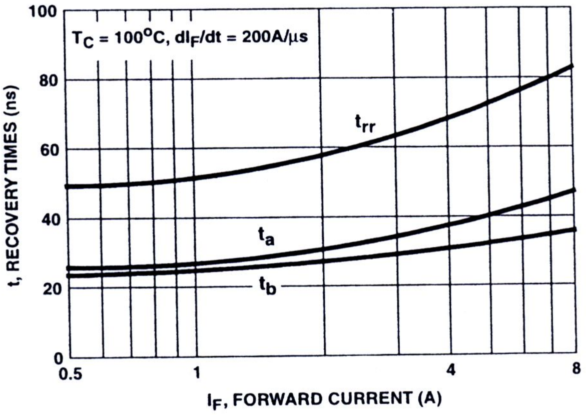


FIGURE 4. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

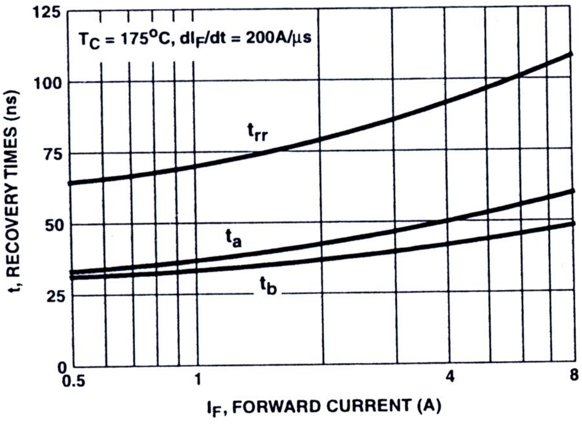


FIGURE 5. t_{rr}, t_a AND t_b CURVES vs FORWARD CURRENT

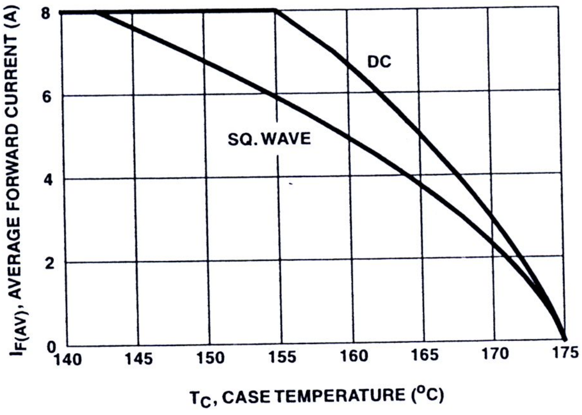


FIGURE 6. CURRENT DERATING CURVE

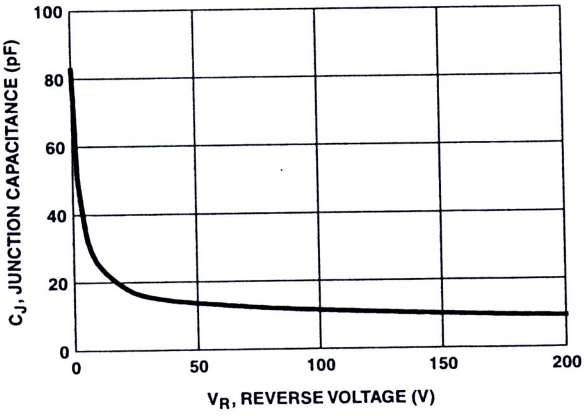


FIGURE 7. JUNCTION CAPACITANCE vs REVERSE VOLTAGE

Test Circuits and Waveforms

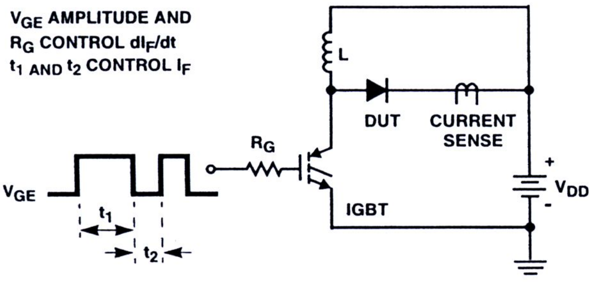


FIGURE 8. t_{rr} TEST CIRCUIT

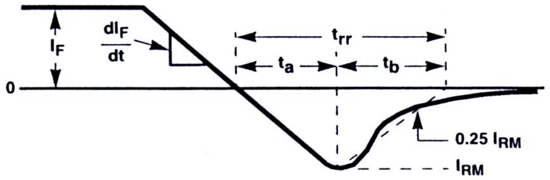


FIGURE 9. t_{rr} WAVEFORMS AND DEFINITIONS

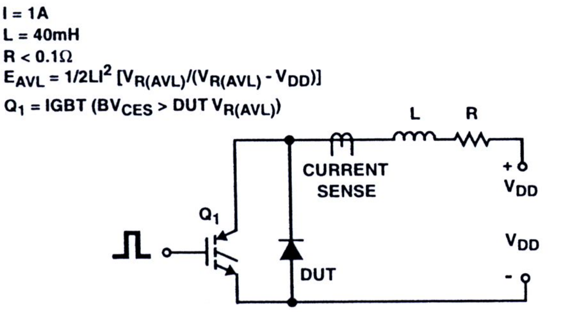


FIGURE 10. AVALANCHE ENERGY TEST CIRCUIT

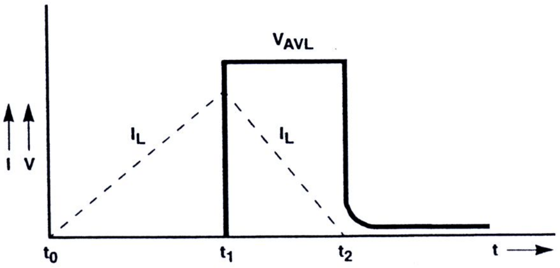


FIGURE 11. AVALANCHE CURRENT AND VOLTAGE WAVEFORMS

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