FLOATING INDUCTANCE SIMULATOR USING CBTA

SUPACHAI LERTWICHA

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Thesis
entitled

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ABSTRACT

Since integrated circuits have very small dimension, an ideal inductor is difficult to implement. The objectives of this work is to design a simulated inductor that can perform as an ideal inductor but has a smaller size. Moreover, the proposed circuit should be able for use in the designing of integrated circuits that works on the radio frequency. The design of the proposed circuit uses a building block named a current backward transconductance amplifier (CBTA). The CBTA was realized by MOS transistors with the MOSIS TSMC $0.25\mu m$ model. The performance of the proposed circuit was analysed by a simulation program. The power consumption of the proposed circuit was compared with an inductance simulator using ZC-CFTA, which was introduced in 2012. The application of the proposed circuit on the second order band pass filter was tested as an example. For the simulation results, the proposed circuit could be linearly performed with errors less than 1% at maximum operating frequency of $20MHz$. The quality factor of this circuit at $20MHz$ was 227 for an inductance value of $0.392mH$. It was observed that the power consumptions of the proposed circuit and inductance simulator using ZC-CFTA were $6.29mW$ and $11.6mW$ respectively. The quality factors of the filter, using the proposed circuit and an ideal inductor, were almost identical.

KEY WORDS: CBTA / FLOATING INDUCTANCE SIMULATOR

77 pages

การจำลองตัวเหนี่ยวนำแบบลอยโดยใช้อุปกรณ์ CBTA

FLOATING INDUCTANCE SIMULATOR USING CBTA

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บทคัดย่อ

เนื่องจากวงจรรวมนั้นมีขนาดที่เล็กมาก ตัวเหนี่ยวนำแบบอุดมคติจึงยากต่อการนำไปใช้งาน เป้าหมายของงานวิจัยนี้คือการออกแบบตัวจำลองตัวเหนี่ยวนำที่สามารถทำงานได้เหมือนตัวเหนี่ยวนำแบบอุดมคติแต่มีขนาดที่เล็กกว่า และวงจรที่นำเสนอนั้นสามารถที่จะนำไปใช้ในการออกแบบวงจรรวมที่ทำงานที่ความถี่คลื่นวิทยุ โดยวงจรที่นำเสนอนั้นได้ทำการออกแบบโดยใช้อุปกรณ์ขยายความนำถ่ายโอนที่กระแสมีการย้อนกลับ (CBTA) โดยอุปกรณ์ CBTA นั้นได้ใช้มอสทรานซิสเตอร์โมเดลของ MOSIS TSCM $0.25\mu m$ เป็นส่วนประกอบ ซึ่งผลการทำงานของวงจรที่นำเสนอจะถูกวิเคราะห์ด้วยโปรแกรมจำลองการทำงาน ค่าการกินพลังงานของวงจรที่นำเสนอจะถูกนำไปเปรียบเทียบกับวงจรจำลองตัวเหนี่ยวนำที่ออกแบบโดย ZC-CFTA ที่มีการนำเสนอในปี 2012 และจะมีการแสดงตัวอย่างเป็นการประยุกต์ใช้งานวงจรที่นำเสนอบนวงจรกรองความถี่แบบแถบผ่านอันดับสอง ผลการจำลองการทำงานนั้นวงจรที่นำเสนอมีการทำงานเป็นเชิงเส้นโดยมีอัตราความผิดพลาดต่ำกว่า 1% ที่ความถี่การทำงานสูงสุด 20MHz และค่าควอลิตี้แฟกเตอร์ของวงจรที่ความถี่ 20MHz นั้นมีค่า 227 สำหรับค่าความเหนี่ยวนำ 0.392mH ผลการสังเกตุการกินพลังงานของวงจรที่นำเสนอกับวงจรที่ออกแบบโดย ZC-CFTA นั้นมีค่า 6.29mW และ 11.6mW ตามลำดับ ค่าควอลิตี้แฟกเตอร์ของวงจรกรองความถี่ที่ประยุกต์ใช้วงจรที่นำเสนอกับตัวเหนี่ยวนำแบบอุดมคตินั้นมีค่าที่ใกล้เคียงจนเกือบจะมีค่าที่เท่ากัน

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CHAPTER I
INTRODUCTION

1.1 Introduction

An inductor is a passive element used in several electronic circuit applications. But in the integrated circuit design, it is very difficult to fabricate inductors on chip, while in the process of making active or passive elements, it is possible to fabricate resistors or capacitors on the integrated circuits. Unfortunately, passive inductors are usually large due to coil's size at high inductance, which the fabrication on the integrated circuits are most likely impossible. For the better understanding on this subject, some of the passive inductors disadvantages will be listed here [1]. For the first disadvantage, the decreasing in inductor's size also decrease its quality factor. Second, the highest quality factor that a passive inductor can possibly achieve is 1000 due to loss in large size inductors, while dissipation factor like 5000 to 10,000 can be achieved by a capacitor. Third, the passive inductors are usually made by ferromagnetic materials, they naturally have low linearity and often cause the harmonic noise in a circuit. Finally, an inductor usually acts as a mini antenna in a circuit. Therefore, it will radiate and receive electromagnetic wave in the air and it will cause noise in a circuit.

An inductance simulator is being introduced because of disadvantages in passive inductors [1]. It is a circuit that acts exactly like a passive inductor except for the following advantages. It consists of active elements like CMOS transistors and grounded capacitors. Because of that, its size is very small and has low power consumption. Moreover, active elements like CMOS transistors can control their parameters via theirs biasing currents. Because of that, an inductance simulator with good designing can adjust its inductance values via its biasing current.

1.2 Literature Review

Gyrators was the earliest circuit that being used to produce an inductance simulator [1], which can be illustrated in Figure 1.1. Gyrator circuits can be described as two ports network circuits, which these ports can be labeled as 1-2 and 3-4. The current and voltage relationship of these two ports can be shown as equation (1.1) and (1.2).

$$V_1 = -KI_2 \tag{1.1}$$

$$V_2 = KI_1 \tag{1.2}$$

Given that I_1, I_2 and V_1, V_2 are currents and voltages at port 1-2 and 3-4 respectively, equation (1.1) and (1.2) can be written as Gyrator impedance matrix Z (1.3).

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & -K \\ K & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{1.3}$$

where K parameter is referred to gyrator resistance. If a capacitor is connected between port 3-4, Gyrator impedance Z_{in} will be calculated as equation (1.4).

$$Z_{in} = sK^2C \tag{1.4}$$

Since equation (1.4) can be looked as the general equation of an ideal inductor, it can be assumed that Gyrator circuits can act as an actual inductor for this case.

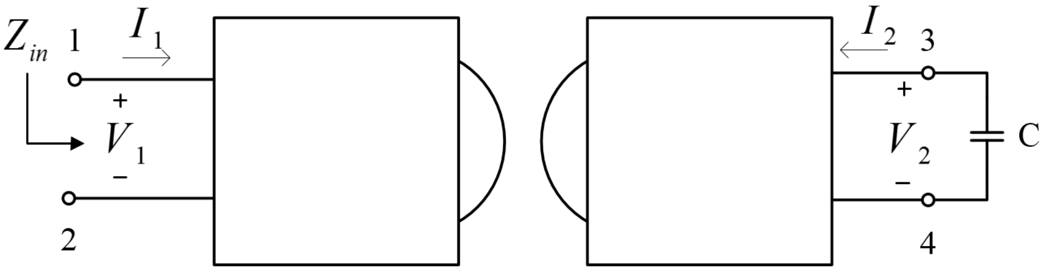


Figure 1.1 Gyrator circuit [1]

From the inductance simulator theory introduced by Gyrator, an active inductance simulator consists of the operational amplifier (OA), capacitors and resistors can be made. The name of that circuit is Riordan circuit, which can be illustrated in Figure 1.2. The input impedance of Riordan circuit can be shown as equation (1.5).

$$Z_{in} = \frac{R_1 R_3 R_5}{R_4} Z_2 \tag{1.5}$$

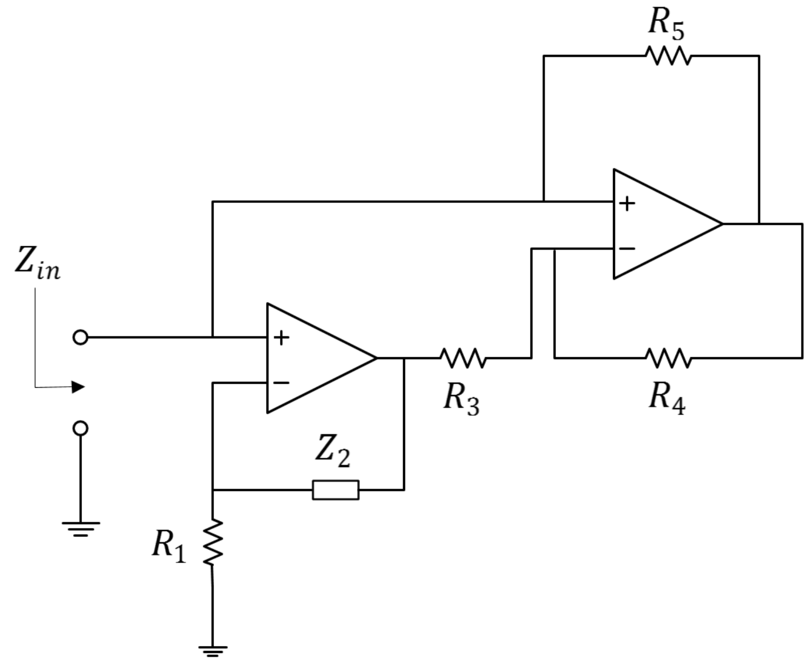


Figure 1.2 Riordan circuit [1]

Knowing from the above explanation, inductance simulator theory can apply to many kind of electronic components. The review about proposed works from past to present will be provided as examples. The review are also including advantages, disadvantages of each proposed work and application of each work on electronic circuits.

There was an introduction of a current conveyer in 1970 by A. Sedra and K.C. Smith [2]. The circuit was operated in current mode and it was achieved good linearity, low power consumption, wide bandwidth and high dynamic range. Because of that attractive performances, a floating inductance simulator based on current conveyors was reported [3]. The circuit was consisted of four current conveyors, two grounded resistors and one grounded capacitor. The circuit worked quite well to act as an actual inductor. Unfortunately, because of the excessive use of the current conveyors, outside resistors and capacitors, the circuit is oversized and consumes high power. Moreover, because a current conveyor did not provide any means to adjust the parameters via the biasing current, a floating inductance simulator based on current conveyors cannot adjust its parameters via the biasing current either. In years 2009, there was a proposed inductance simulator based on Current Controlled Differential Current Voltage Conveyors (CCDVCCs) [6]. Its structure was a little more complicated than standard current conveyors, but it came with an adjustable feature. The parasitic resistance of simulated inductor can be directly tuned via the biasing current. Because of that explained advantages, a floating inductance simulator based on CCDVCCs can adjust its inductance values via the biasing current. Moreover, its structure components were further reduced to two CCDVCCs, comparing to the previous work which contained four current conveyors. The researches after that has been focused on minimalizing the active and passive components of the floating inductance simulator. In the recent years, there was a floating inductance simulator based on Differential Voltage Current-Controlled Conveyor Transconductance Amplifiers (DVCCCTAs) [7]. In order to minimalize the active components, DVCCCTAs structure are more complicated comparing to CCDVCCs. Like CCDVCCs, this circuit also came with tunable features. To show the simplicity of the circuit, the floating inductance simulator using DVCCCTAs can be illustrated in figure 1.3. As seen in the figure, the composition of the inductance simulation consisted of only a single block of DVCCCTA. Moreover, its circuit contains only one grounded capacitor without any grounded resistors. Because of that, the power consumption of this circuit is very low and its structure is much simpler.

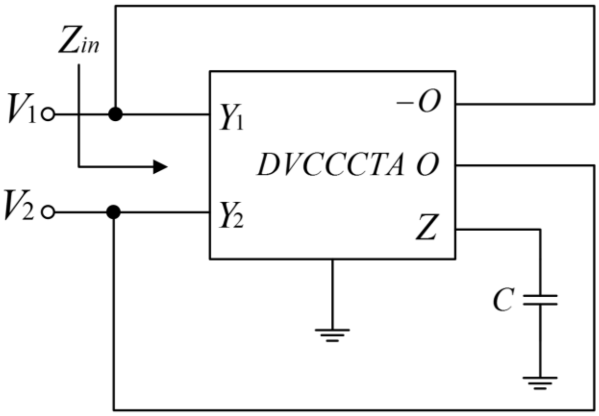


Figure 1.3 Inductance simulator based on DVCCCTA [7]

1.3 Research Objective

The objective of this research is to test, design and simulate on floating inductance simulators. The basic information such as characteristic of transistor, differential amplifier and the building block will be studied. That information will be used in the circuit designing process. A building block and its active components that is suitable for the designing of inductance simulators will be chosen. In addition, the characteristic of that chosen building block will be analyzed. After that, the inductance simulator will be realized by the chosen building block. This work aims to designs an inductance simulator that has simple structure and electronically tunable. The experiments are focusing on an active inductor's structure, linearity and power consumption. In order to verify the performance of inductance simulator, the test on simulation program will be provided. A designed circuit will be simulated by Cadence Orcad Pspice program. Inductance values, power consumption, operating ranges will be given as results. Comparison between a designed circuit, previous work and an ideal inductor will also be provided. For the application of the designed circuit, it will be used in common electronic circuits that benefit in the present time, for example filters, oscillators, square rooting circuits and multipliers.

1.4 Thesis Outline

This thesis is organized as follows. The details about characteristic of MOSFET and operation of the MOSFET circuits are presented in chapter 2. The details about CBTA realization using MOSFET circuit and the investigation on the frequency response, non-ideal effect, and operating condition are provided in chapter 3. The realization of inductance simulator using CBTA and the simulation result are presented in chapter 4. The discussion on the simulation results and the future application of the circuit are presented in chapter 5.

CHAPTER II

FREQUENCY RESPONSE OF MOSFET CIRCUITs

2.1 Introduction

In this chapter, an explanation on the characteristics of Metal-Oxide Semiconductor Field Effect Transistors will be provided [8]. In addition, the basic understanding of basic building blocks such as OTA (Operational transconductance amplifier) which make use of active circuits like MOSFETs will be introduced [9]. A Building block is simply the integration of complex configuration of active circuits. It takes shape in a single element to simplify the designation of circuits that use large amounts of active components such as filter, oscillator and inductance simulator. In this chapter, the example of a building blocks and their frequency response will be provided.

2.2 Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)

2.2.1 Cross-section and circuit symbol of MOSFET

Semiconductors are devices that can be both conductor and insulator. A biasing current/voltage that being applied on the semiconductor is the main factor for deciding its properties. The circuit symbol and cross-section of a MOSFET can be shown in figure 2.1 [8].

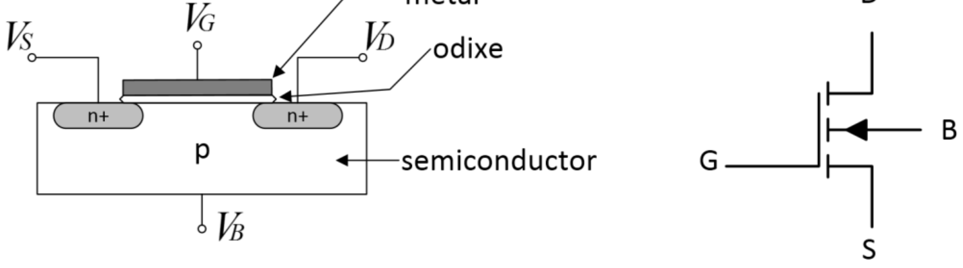


Figure 2.1 cross-section of a MOSFET and circuit symbol [8]

A circuit symbol in figure 2.1 showing that MOSFET has four terminals which are gate, source, drain and body. The source terminal is the place where the charged carriers begin to flow, while the drain terminal is the place that receive those charged carriers. The gate terminal will act as the control terminal of that flowing carriers between those two terminals.

In the cross-section of MOSFET in figure 2.1, the semiconductor part is usually made of silicon. The existing of an oxide layer between the metal gate and the semiconductor substrate is the origin of the name Metal-Oxide Semiconductor. A MOSFET generally has two types which is determined by its induced channel. If the arrow in a circuit symbol is going from p substrate to n-channel, that MOSFET will be n-channel MOSFET. The opposite of that will be p-channel MOSFET. The illustration of MOSFET n-channel and p-channel can be shown in figure 2.2, which the body terminal is joined to the source for a simpler circuit symbol.

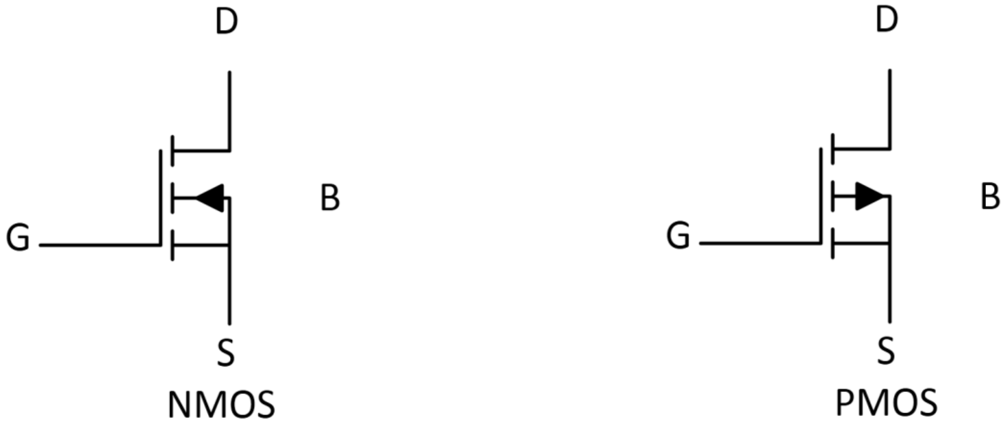
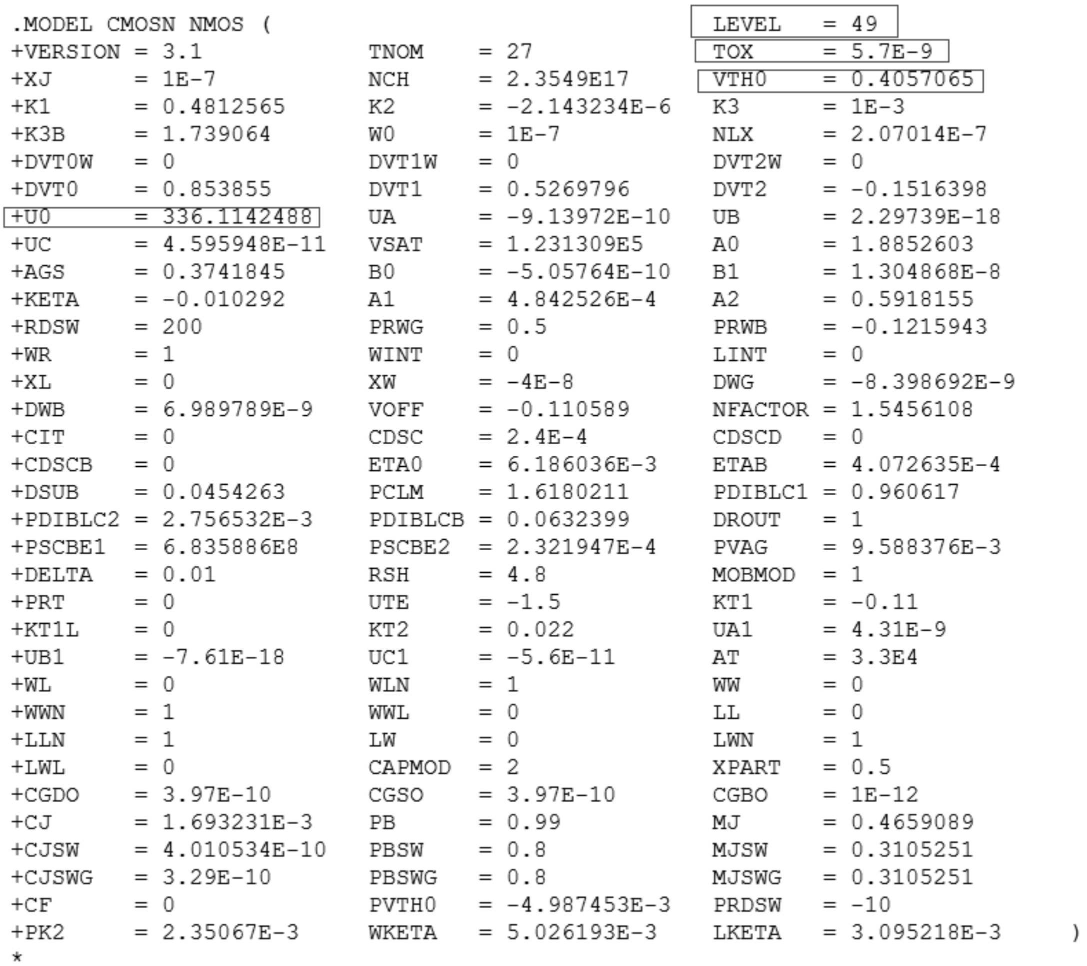


Figure 2.2 MOSFET n-type and p-type [8]

2.2.2 Basic operation of MOSFET

The Taiwan Semiconductor Manufacturing Company (TSMC) MOSFET parameter model is represented by Berkeley Short-channel IGFET Model 3 Version 4 (BSIM3V4) and can be shown as an example in figure 2.4. The level-49 parameter refers to the number of MOS device models that was developed. The parameters in square marks are the first group of parameters that will be used for the analysis of basic operation of MOSFET.



```
.MODEL CMOSN NMOS (                                   LEVEL   = 49
+VERSION = 3.1          TNOM    = 27                  TOX     = 5.7E-9
+XJ      = 1E-7         NCH     = 2.3549E17           VTH0    = 0.4057065
+K1      = 0.4812565    K2      = -2.143234E-6        K3      = 1E-3
+K3B     = 1.739064     W0      = 1E-7                NLX     = 2.07014E-7
+DVT0W   = 0            DVT1W   = 0                   DVT2W   = 0
+DVT0    = 0.853855     DVT1    = 0.5269796           DVT2    = -0.1516398
+U0      = 336.1142488  UA      = -9.13972E-10        UB      = 2.29739E-18
+UC      = 4.595948E-11 VSAT    = 1.231309E5          A0      = 1.8852603
+AGS     = 0.3741845    B0      = -5.05764E-10        B1      = 1.304868E-8
+KETA    = -0.010292    A1      = 4.842526E-4         A2      = 0.5918155
+RDSW    = 200          PRWG    = 0.5                 PRWB    = -0.1215943
+WR      = 1            WINT    = 0                   LINT    = 0
+XL      = 0            XW      = -4E-8               DWG     = -8.398692E-9
+DWB     = 6.989789E-9  VOFF    = -0.110589           NFACTOR = 1.5456108
+CIT     = 0            CDSC    = 2.4E-4              CDSCD   = 0
+CDSCB   = 0            ETA0    = 6.186036E-3         ETAB    = 4.072635E-4
+DSUB    = 0.0454263    PCLM    = 1.6180211           PDIBLC1 = 0.960617
+PDIBLC2 = 2.756532E-3  PDIBLCB = 0.0632399           DROUT   = 1
+PSCBE1  = 6.835886E8   PSCBE2  = 2.321947E-4         PVAG    = 9.588376E-3
+DELTA   = 0.01         RSH     = 4.8                 MOBMOD  = 1
+PRT     = 0            UTE     = -1.5                KT1     = -0.11
+KT1L    = 0            KT2     = 0.022               UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11            AT      = 3.3E4
+WL      = 0            WLN     = 1                   WW      = 0
+WWN     = 1            WWL     = 0                   LL      = 0
+LLN     = 1            LW      = 0                   LWN     = 1
+LWL     = 0            CAPMOD  = 2                   XPART   = 0.5
+CGDO    = 3.97E-10     CGSO    = 3.97E-10            CGBO    = 1E-12
+CJ      = 1.693231E-3  PB      = 0.99                MJ      = 0.4659089
+CJSW    = 4.010534E-10 PBSW    = 0.8                 MJSW    = 0.3105251
+CJSWG   = 3.29E-10     PBSWG   = 0.8                 MJSWG   = 0.3105251
+CF      = 0            PVTH0   = -4.987453E-3        PRDSW   = -10
+PK2     = 2.35067E-3   WKETA   = 5.026193E-3         LKETA   = 3.095218E-3     )
*
```

Figure 2.3 BSIM3V4 MOSFET Parameters for TSMC 0.25 micron

The basic operation of MOSFET can be explained as following. To start the operation, a MOSFET has to be biased with a DC current or voltage. When the gate voltage is reaching a certain point, there will be a channel forming underneath the gate from the source terminal to the drain terminal and the current will be conducted in the MOSFET. The current that flow through the transistor is depending on the voltage between the gate and the source terminal of the transistors (V_{GS}). The sufficient gate voltage for the transistor to form a conduction path is called 'threshold voltage' (V_{TH}). When $V_{GS} = V_{TH}$, the current will be conducting between the drain terminal and the source terminal via the formed conduction path. If gate-to-source voltage still keep increasing, the drain current I_D will also linearly increase as well for a certain point. The base threshold voltage is one of the BSIM3V4 parameter that being in a square mark in figure 2.3 and that value is $VTH0$. The actual V_{TH} is normally affected by the back-gate bias voltage (V_{BS}) and it highly depends on the parameter K1, K2 and K3 of the BSIM3V4 parameter in figure 2.3. In this case, the nMOS body terminal and the source terminal are joined together, the back-gate voltage V_{BS} will be zero. Because of that, the base threshold voltage can directly be used as threshold voltage, ($V_{BS} = 0$ and $V_{TH} = VTH0$).

When the increasing of drain current I_D hits a certain point of drain-to-source voltage (V_{DS}), the current I_D will stop increasing and go into flat band instead. The drain-to-source voltage and a current at that point will be called $I_{D(sat)}$ and V_{Dsat} respectively. At the same time, the gate-to-drain voltage (V_{GD}) that the drain current I_D stop increasing will be equal to the threshold voltage ($V_{GD} = V_{TH}$). The drain current of nMOSFET can be estimated in two cases which are the equation 2.1 and 2.2.

For $V_{GS} > V_{TH}$ and $V_{DS} < V_{Dsat}$

$$I_D = K\left[2\left(V_{GS} - V_{TH}\right) - V_{DS}\right]V_{DS} \qquad (2.1)$$

For $V_{GS} > V_{TH}$ and $V_{DS} \geq V_{Dsat}$

$$I_D = K\left(V_{GS} - V_{TH}\right)^2 \qquad (2.2)$$

where $V_{Dsat} = V_{GS} - V_{TH}$. If the threshold voltage V_{TH} is constant, the conduction coefficient K can be defined by intrinsic conductivity and feature size of nMOS transistor. The conduction coefficient K can be shown in equation 2.3

$$K = \frac{1}{2}\mu_0 C_{OX}\frac{W}{L} \qquad (2.3)$$

where parameter μ_0 is the carrier's mobility and is the parameter $U0$ in BSIM3V4 parameters model in figure 2.3. Parameter C_{OX} is the gate oxide capacitance per unit area which is determined by oxide thickness t_{OX} of MOSFET and is the parameter TOX in the BSIM3V4 parameters model in figure 2.3. The W/L in the equation 2.3 is referred to the channel width/length of MOSFET which can be shown in cross-section in figure 2.4.

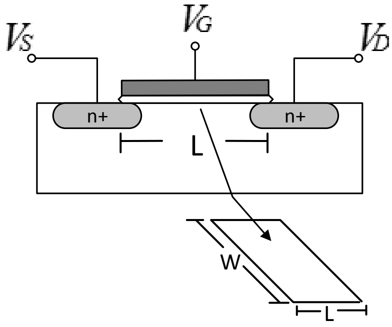


Figure 2.4 feature sizes W and L of MOSFET [8]

Knowing the drain current and the conduction coefficient, the transconductance (g_m) of nMOS transistor can be calculated as equation 2.4.

$$g_m = 2\sqrt{KI_D} \tag{2.4}$$

2.2.3 Transistor Parasitics [8]

Most of the electronic components have their own limitation and the part that put the limitation on the MOSFETs is called transistor parasitics. Parasitics are the unseen capacitances and inductances in the transistors which the latter are usually involved in the part of transmission line. This chapter will not consider parasitic inductances into calculation since the building blocks are more related to the structure of MOSFET. The parasitic capacitances are the one that more crucial on the structure part which are junctions and layers of MOSFET. Parasitic capacitances are usually in the order of pF and fF, which mean they will not have much effect on low frequencies. If MOSFETs are dealing with the high frequencies, this parasitic capacitances have to be taken into calculation which are going put the limitation on the MOSFET.

MOSFET has four important parasitic capacitances which can be explained using figure 2.5. The first pair is the gate capacitances C_{GS} and C_{GD} that occurs between the overlapping of the gate and the source/drain terminals. The others are junction capacitances C_{JS} and C_{JD} that occurs on the side wall and area of each drain and source terminals. The necessary parameters for parasitic capacitances calculation can be found in BSIM3V4 parameters in the square mark which is illustrated in figure 2.6.

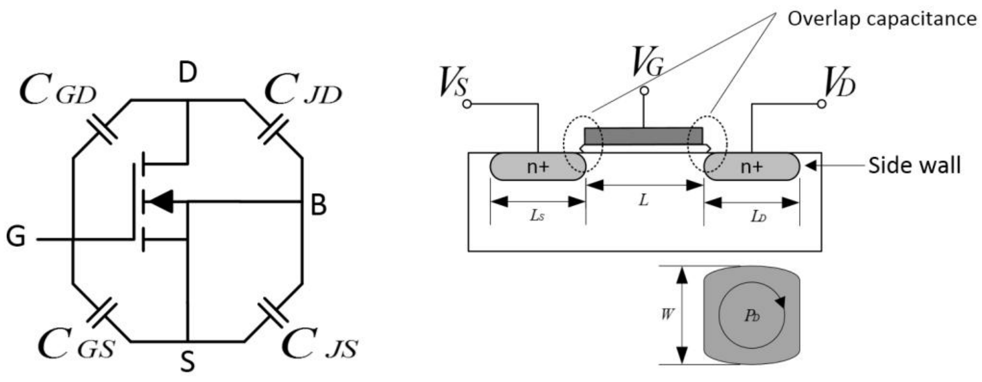
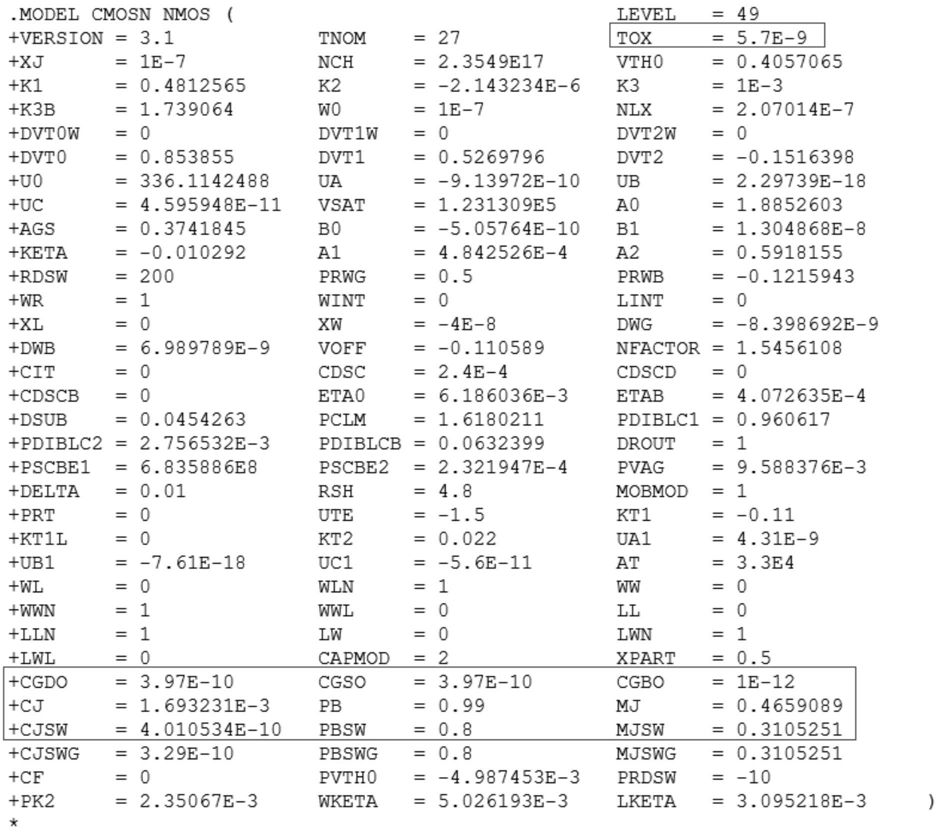


Figure 2.5 Parasitic capacitances of MOSFET [8]

The gate capacitances C_{GS} and C_{GD} can be calculated by these equations

$$C_{GS} = \frac{2}{3} C_{OX} (W \times L) + CGSO \times W \tag{2.5}$$

$$C_{GD} = CGDO \times W \tag{2.6}$$



```
.MODEL CMOSN NMOS (                                     LEVEL   = 49
+VERSION = 3.1             TNOM    = 27                 TOX     = 5.7E-9
+XJ      = 1E-7            NCH     = 2.3549E17          VTH0    = 0.4057065
+K1      = 0.4812565       K2      = -2.143234E-6       K3      = 1E-3
+K3B     = 1.739064        W0      = 1E-7               NLX     = 2.07014E-7
+DVT0W   = 0               DVT1W   = 0                  DVT2W   = 0
+DVT0    = 0.853855        DVT1    = 0.5269796          DVT2    = -0.1516398
+U0      = 336.1142488     UA      = -9.13972E-10       UB      = 2.29739E-18
+UC      = 4.595948E-11    VSAT    = 1.231309E5         A0      = 1.8852603
+AGS     = 0.3741845       B0      = -5.05764E-10       B1      = 1.304868E-8
+KETA    = -0.010292       A1      = 4.842526E-4        A2      = 0.5918155
+RDSW    = 200             PRWG    = 0.5                PRWB    = -0.1215943
+WR      = 1               WINT    = 0                  LINT    = 0
+XL      = 0               XW      = -4E-8              DWG     = -8.398692E-9
+DWB     = 6.989789E-9     VOFF    = -0.110589          NFACTOR = 1.5456108
+CIT     = 0               CDSC    = 2.4E-4             CDSCD   = 0
+CDSCB   = 0               ETA0    = 6.186036E-3        ETAB    = 4.072635E-4
+DSUB    = 0.0454263       PCLM    = 1.6180211          PDIBLC1 = 0.960617
+PDIBLC2 = 2.756532E-3     PDIBLCB = 0.0632399          DROUT   = 1
+PSCBE1  = 6.835886E8      PSCBE2  = 2.321947E-4        PVAG    = 9.588376E-3
+DELTA   = 0.01            RSH     = 4.8                MOBMOD  = 1
+PRT     = 0               UTE     = -1.5               KT1     = -0.11
+KT1L    = 0               KT2     = 0.022              UA1     = 4.31E-9
+UB1     = -7.61E-18       UC1     = -5.6E-11           AT      = 3.3E4
+WL      = 0               WLN     = 1                  WW      = 0
+WWN     = 1               WWL     = 0                  LL      = 0
+LLN     = 1               LW      = 0                  LWN     = 1
+LWL     = 0               CAPMOD  = 2                  XPART   = 0.5
+CGDO    = 3.97E-10        CGSO    = 3.97E-10           CGBO    = 1E-12
+CJ      = 1.693231E-3     PB      = 0.99               MJ      = 0.4659089
+CJSW    = 4.010534E-10    PBSW    = 0.8                MJSW    = 0.3105251
+CJSWG   = 3.29E-10        PBSWG   = 0.8                MJSWG   = 0.3105251
+CF      = 0               PVTH0   = -4.987453E-3       PRDSW   = -10
+PK2     = 2.35067E-3      WKETA   = 5.026193E-3        LKETA   = 3.095218E-3     )
*
```

Figure 2.6 BSIM3V4 MOSFET parameters that required for parasitic capacitances calculation.

The parameters CGSO, CGDO and TOX that required for equation 2.5 and 2.6 are already in the figure 2.6. For the junction capacitances C_{JS} and C_{JD}, the required parameters in figure 2.6 are CJ and CJW. The junction capacitances C_{JD} can be calculated using this equation.

$$C_{JD} = CJ \times A_D + CJSW \times P_D \tag{2.7}$$

where P_D is the perimeter of the drain junction and A_D is the dimension of the drain junction. Both values can be calculated using this equation

$$A_D = W \times L_D \tag{2.8}$$

$$P_D = 2 \times (W + L_D) \tag{2.9}$$

where L_D is the drain extension length of MOSFET. The position of P_D and L_D are already included in the figure 2.5. It should be mentioned that C_{JS} will be in the same value as C_{JD} if these parameters for both terminals are identical ($P_D = P_S, L_D = L_S$).

To clarify the parasitic capacitances effect on MOSFET at the high frequencies, all these four capacitances have to be taken into calculation. In this case, only C_{GS} and C_{GD} will be taken into calculation for the basic understanding. The small signal model of MOSFET that include the parasitic capacitance C_{GS} and C_{GD} can be illustrated in figure 2.7.

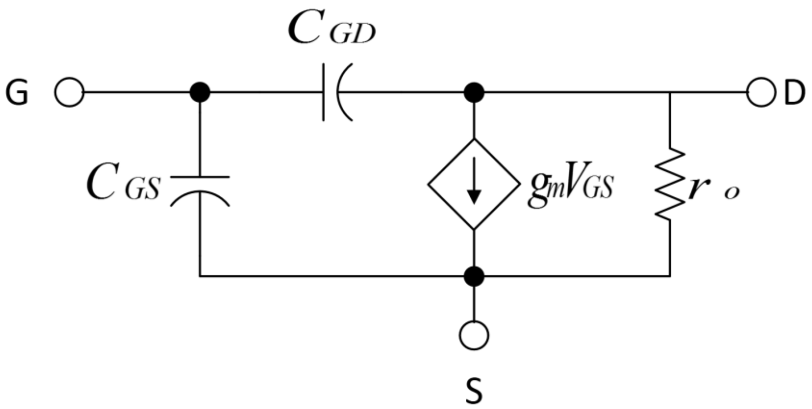


Figure 2.7 MOSFET small signal model at high frequencies [8].

To show the example of the limitation of parasitic capacitances on MOSFET, The common-drain amplifier configuration is used as the case study for frequency response. This configuration can be illustrated in figure 2.8

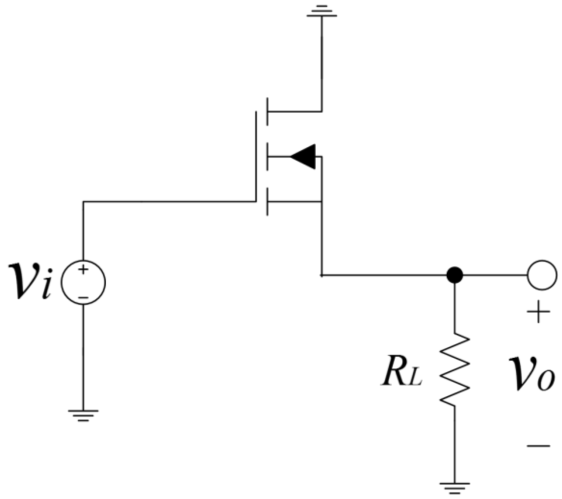


Figure 2.8 MOSFET common drain amplifier [9]

In order to determine the voltage gain of the above figure at high frequencies, its transfer function has to be specified. The small signal model of figure 2.8 that already included parasitic capacitances can be illustrated in figure 2.9. This figure has a resistor R_S that assumed to be the resistance of the voltage source and a resistor load R_L that connected at the source terminal to the ground.

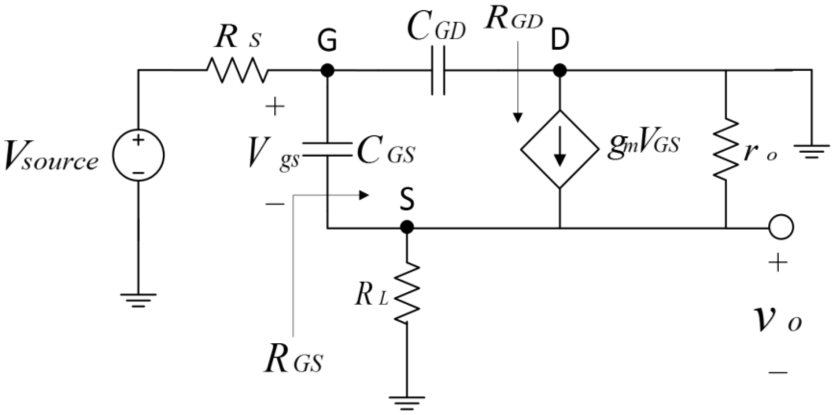


Figure 2.9 High frequency model of MOSFET common drain amplifier

The gain at the low frequency A_M of figure 2.9 can be obtained by setting all the parasitic capacitances to zero. As a result, the low frequency gain can be described by equation 2.10.

$$A_M = \frac{(R_L \| r_o)}{(R_L \| r_o) + (1/g_m)} \tag{2.10}$$

The cut-off at high frequency (f_H) can be derived by using the open-circuit time constants method. This method requires to look for the resistance that associated with each of capacitance in figure 2.9 separately. Assumed that V_{source} is zero and C_{GD} open circuit ($C_{GD} = 0$), the resistance that associated with C_{GD} can be calculated as equation 2.11.

$$R_{GD} = R_S \tag{2.11}$$

For the resistance that associated with the capacitance C_{GD}, a test voltage source will be applied between gate and drain terminals. This can be shown in figure 2.10.

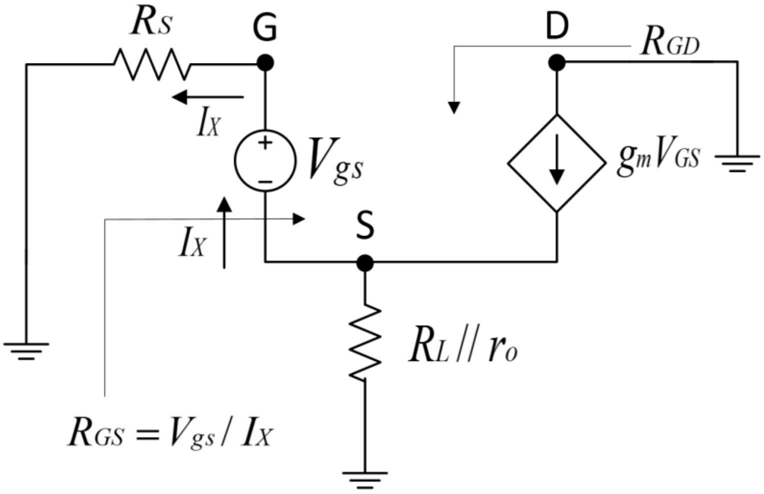


Figure 2.10 The MOSFET model for determine the resistance R_{GS}

The resistance associated with capacitance C_{GS} can be shown in this equation.

$$R_{GS} = \frac{R_{GD} + (R_L \| r_o)}{1 + g_m (R_L \| r_o)} \tag{2.12}$$

The value of resistance r_o is usually much higher than R_L and can be ignored. Combine both time constants together to determine the cut-off frequency f_H, the result can be shown as equation 2.13.

$$f_H = \frac{1}{2\pi\tau_H} = 1/2\pi(C_{GD}R_{GD} + C_{GS}R_{GS}) \tag{2.13}$$

The MOSFET common drain amplifier with the bias section can be illustrated in figure 2.11. The components that being added to figure 2.8 are a constant current source, two voltage sources and three bypass capacitors.

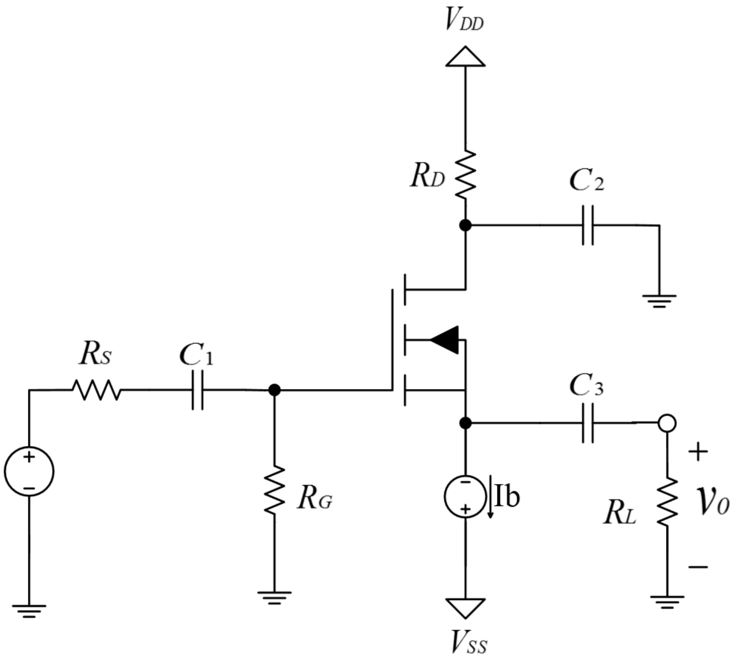


Figure 2.11 Common drain amplifier with bias section [9]

Because some of resistors added in figure 2.11, equation 2.11 will become this equation

$$R_{GD} = R_S \| R_G \tag{2.14}$$

And equation 2.12 will become

$$R_{GS} = \frac{R_S \| R_G + (R_L \| r_o)}{1 + g_m (R_L \| r_o)} \tag{2.15}$$

For the frequency response calculation, set the channel width and length of MOSFET to $2.5\mu m$ and $0.7\mu m$ respectively. With MOSFET parameters from figure 2.6, the parasitic capacitances can be calculated as $C_{GS} = 11.59\,fF$, $C_{GD} = 0.99\,fF$ using equations 2.5 and 2.6 respectively. Setting the constant current source in figure 2.11 to $50\mu A$, transconductance of MOSFET can be calculated as $g_m = 0.26mA/V^2$ using equation 2.4. Setting the resistors $R_S = 10k$, $R_G = 100k$, the resistances that associated with both parasitic capacitances can be calculated by equation 2.14 and 2.15. As results, those resistance values can be calculated as $R_{GD} = 909\Omega$ and $R_{GS} = 3372\Omega$. Using equation 2.13., the cut-off at high frequency f_H of figure 2.11 can be estimated as 4.13 GHz. For the more accurate value of f_H, the calculation by Pspice software is provided. Setting all the bypassed capacitors in figure 2.11 to $1uF$, DC bias voltages to $\pm 1.5V$ and AC input voltage to 1V, the circuit in the figure 2.11 can be redrawn in Pspice and it can be illustrated in figure 2.12.

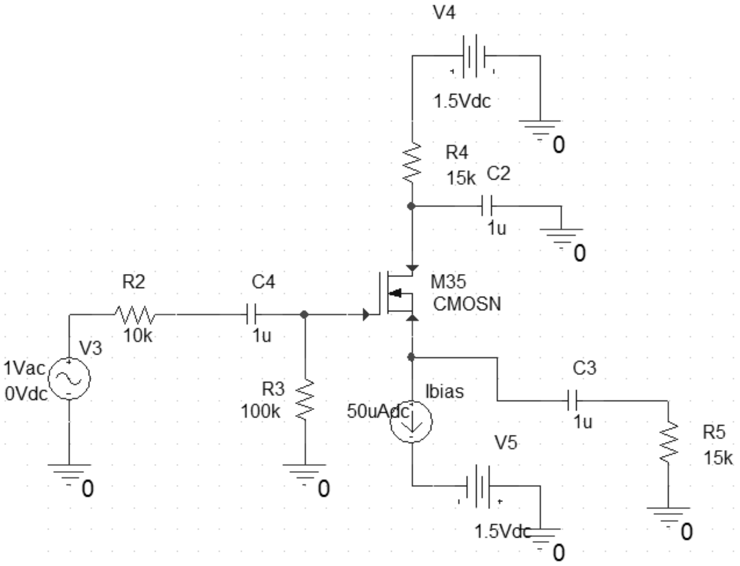


Figure 2.12 Common drain amplifier circuit using Pspice

The voltage gain of figure 2.12 versus frequency can be illustrated in figure 2.13

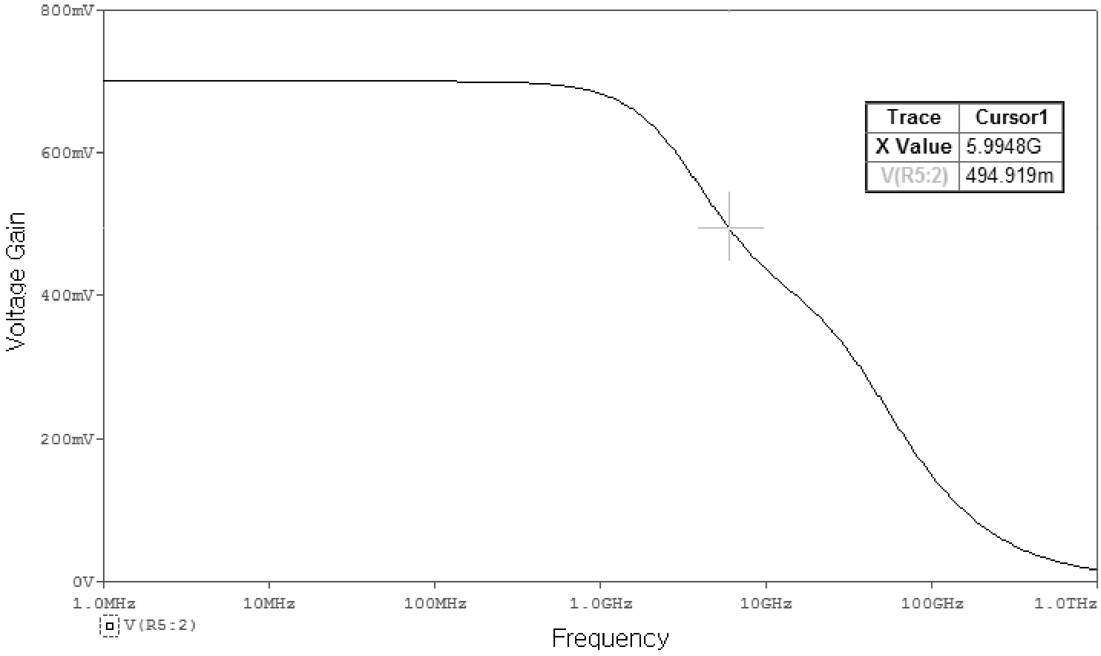


Figure 2.13 Frequency response of MOSFET common drain amplifier

The cursor in figure 2.13 indicated that the -3dB of figure 2.12 is equals to 5.99GHz. This serve as a proof that the parasitic capacitances are affecting the performance of MOSFET on high frequency. If comparing this value to the one that being calculated by hand, the error of hand calculation will be about 30%. The value that acquired by Pspice is more accurated because the hand calculation use only capacitances C_{GD} and C_{GS} . Anyway, it is enough to explain the effect of parasitic capacitances on the MOSFET on high frequency.

2.3 Differential Amplifiers [9]

A differential amplifier is considered to be one of the amplifier circuit and it is a circuit that often used in integrated-circuit design. It takes an important part for being an input port of many building-blocks. An example is the operational amplifier (Op-Amp). The basic structure of differential amplifier can be implemented using discrete bipolar or CMOS technology. For this work, The MOSFETs are chosen because they consume less power. The different pair that is constructed by two MOSFETs n-channel technology can be illustrated in figure 2.14.

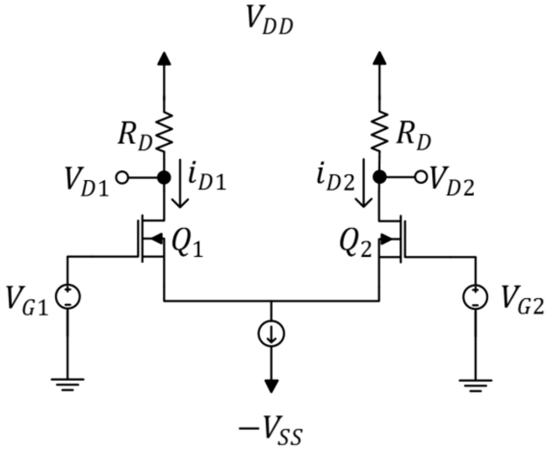


Figure 2.14 MOS Differential Amplifier [9]

It should be included that the setup of both transistors are perfectly matched. The source terminals of these two transistors are connected together and having voltages $|V_{DD}|=|-V_{SS}|$ and a constant-current source I_B as bias section. This constant current source can be created using a simple MOSFET current mirror. The load resistors R_D

are connected between the voltage supply V_{DD} and the drain terminals of both transistors. These resistors can be replaced later with active loads in case that the MOS different pair is connected to the resistances from other circuits. For the explanation of basic operation of a different pair, only normal resistive loads will be used for now. A differential pair has two operating modes that are common-mode and difference-mode.

2.3.1 Operation with common-mode

For the operation mechanic of the different pairs in common-mode, the circuit configuration can be illustrated in figure 2.15.

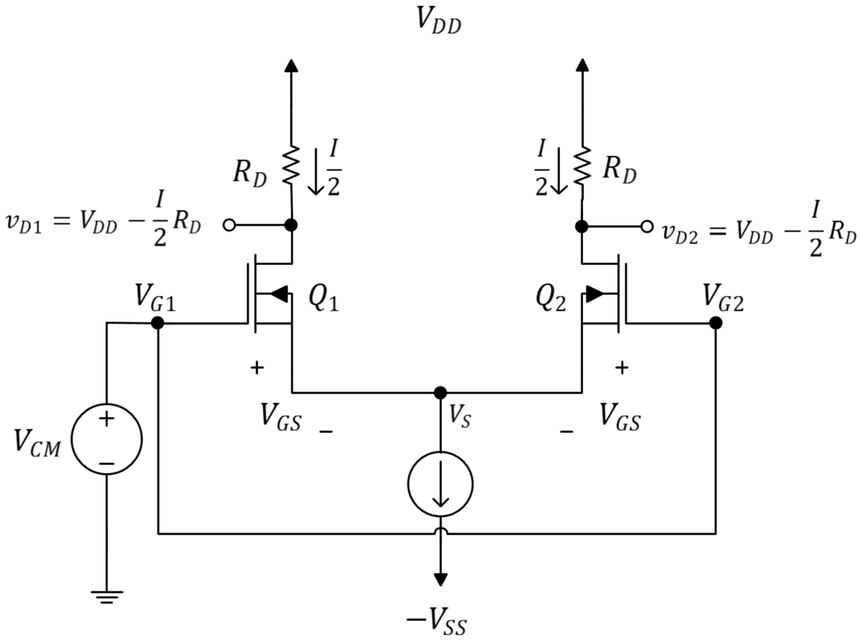


Figure 2.15 MOS different pair with common-mode input voltage [9].

The gate terminals of both MOSFETs in this configuration are joined together and connected to the input voltage source V_{CM}. This configuration sets the gate voltages of both transistors to $V_{CM} = V_{G1} = V_{G2}$ and also sets the gate-to-source voltages of both transistors to be equal. Because $V_{GS1} = V_{GS2}$ and transistors Q_1 and Q_2 are perfectly matched, the drain current of each transistor can assumed to be equal using equation 2.2. Since both MOSFETs are biased by a constant current source I, half of the biasing current will be splited into each transistor. The drain current in each transistors can be calculated as equation 2.16.

$$I_D = \frac{I}{2} = \frac{1}{2}\mu_0 C_{OX} \frac{W}{L}(V_{GS(1,2)} - V_t)^2 \tag{2.16}$$

Equation 2.16 can also be expressed in term of overdrive voltage (V_{OV}) like this

$$V_{OV} = V_{GS} - V_t \tag{2.17}$$

$$\frac{I}{2} = \frac{1}{2}\mu_0 C_{OX} \frac{W}{L} {V_{OV}}^2 \tag{2.18}$$

To conclude this section, the common-mode operation is the behavior of the different pairs with identical input that divided the current equally from the biasing current source.

2.3.2 Operation with differential-mode

For the operation mechanic of the different pairs in differential-mode, the circuit configuration can be illustrated in figure 2.16.

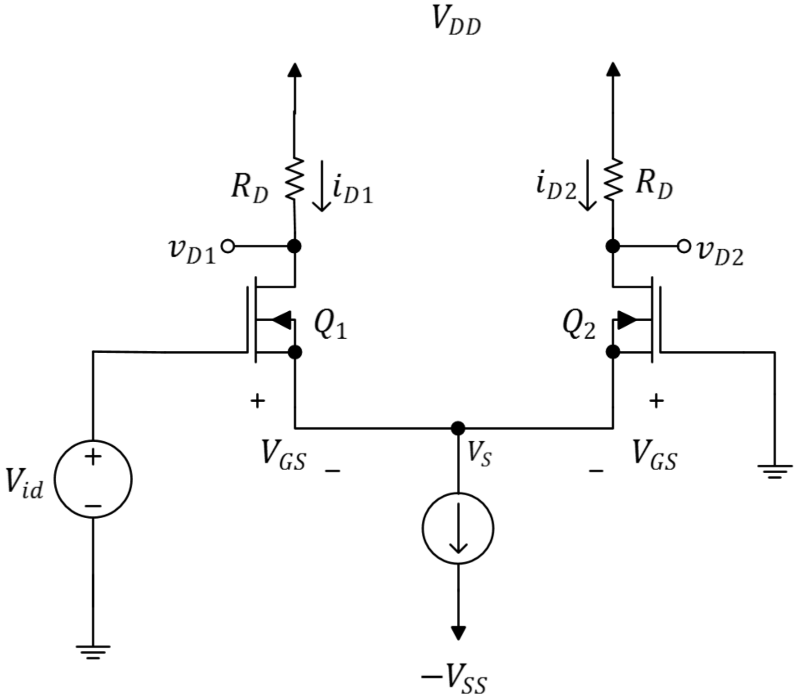


Figure 2.16 MOS differential pair with a differential input voltage [9]

In this case, There is an input voltage source connected to the gate terminal of Q_1 while the gate terminal of Q_2 is grounded. The differential input voltage now equals to $V_{id} = V_{GS1} - V_{GS2}$. Since the gate terminal of Q_2 is grounded, V_{GS1} will be higher than V_{GS2} for the positive values of V_{id}. At the same time, the drain current i_{D1} can be proven to be higher than i_{D2} by using equation 2.2. For the negative values of V_{id}, the drain current will be $i_{D2} > i_{D1}$. The different between the drain current of both MOSFET in differential mode is proportional. If the drain current i_{D1} is increasing by ΔI, i_{D2} will also decreasing by ΔI. The exact values of each drain current can be calculated in this equation.

$$i_{D1} = \frac{I}{2} + \frac{I}{V_{OV}}(\frac{V_{id}}{2})\sqrt{1-(\frac{(V_{id}/2)}{V_{OV}})^2} \qquad (2.19)$$

$$i_{D2} = \frac{I}{2} - \frac{I}{V_{OV}}(\frac{V_{id}}{2})\sqrt{1-(\frac{(V_{id}/2)}{V_{OV}})^2} \qquad (2.20)$$

The graph of I-V characteristic between the input differential voltage V_{id} and the drain currents of Q_1 and Q_2 can be illustrated in figure 2.17 using equation 2.19 and 2.20 respectively.

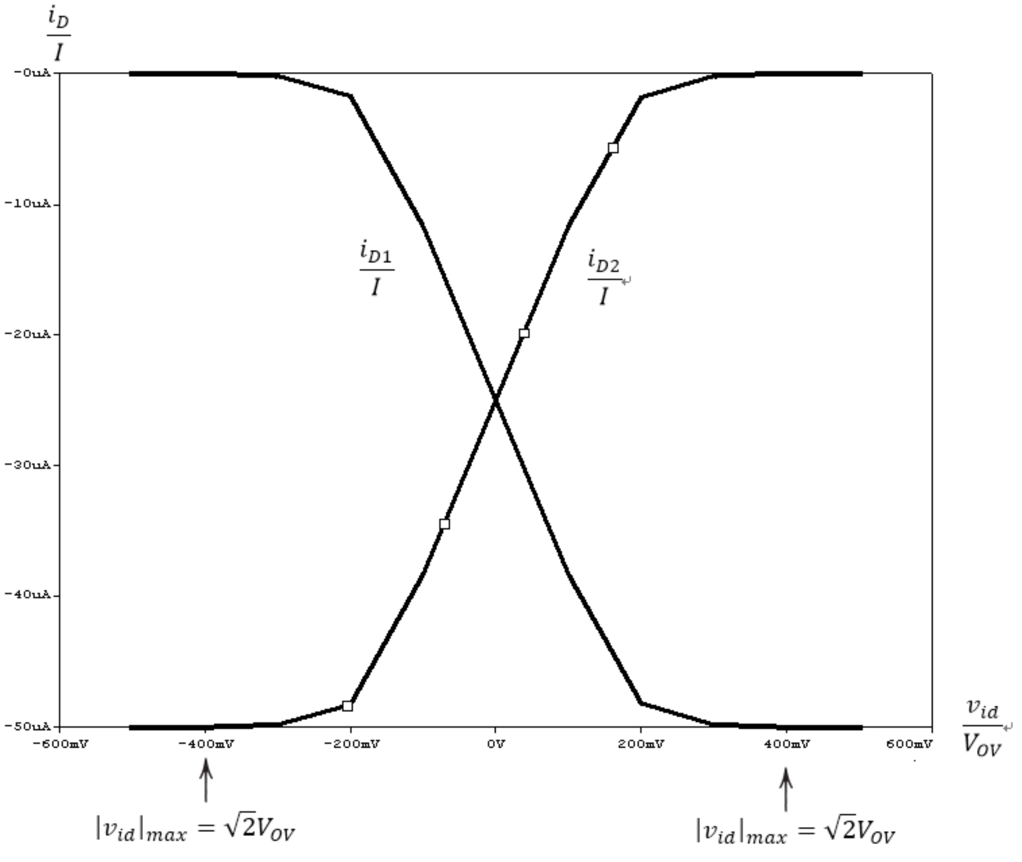


Figure 2.17 I-V characteristic between V_{id} and (i_{D1}, i_{D2}).

The plot in figure 2.17 is nonlinear because the equation 2.19 and 2.20 got the square term (V_{id}^{2}). In order to increase the linear ranges of figure 2.17, we have to keep the differential input V_{id} as small as possible ($V_{id}/2 << V_{OV}$). As a result, equation 2.19 and 2.20 can be estimated to this equation

$$i_{D1} \approx \frac{I}{2} + \frac{I}{V_{OV}}(\frac{V_{id}}{2}) \tag{2.21}$$

$$i_{D2} \approx \frac{I}{2} - \frac{I}{V_{OV}}(\frac{V_{id}}{2}) \tag{2.22}$$

The other approach is to increase the overdrive voltage V_{OV} in equation 2.19 and 2.20 rather than keeping the differential input voltage to small values. The overdrive voltage can be increased by using the smaller W/L ratio. Note that doing this will reduce the g_m as well as the gain of a differential pair. The graph of I-V characteristic using equation 2.21 and 2.22 for the different values of V_{OV} can be illustrated in figure 2.18. It can be clearly seen from the figure that the linear ranges of a differential pair can be increased with higher overdrive voltages.

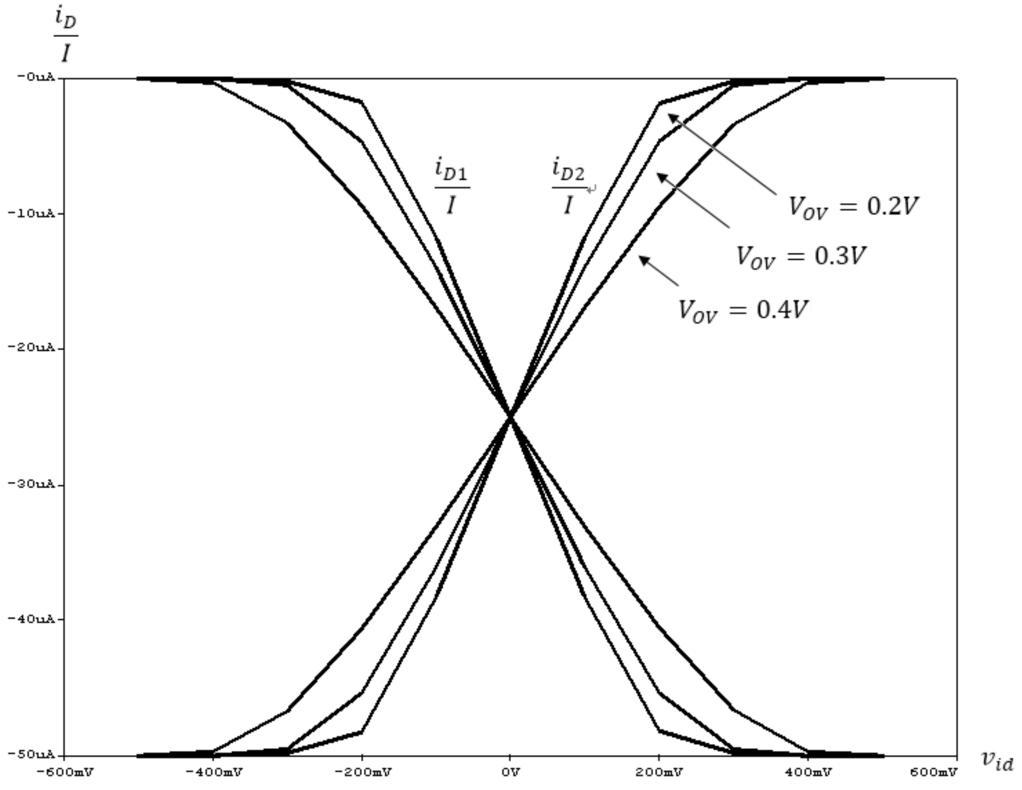


Figure 2.18 Linearity Extension of Differential Pair

2.3.3 Differential-mode Gain

In order to consider the gain of differential-mode, the configuration in figure 2.16 can be alternatively illustrated in figure 2.19

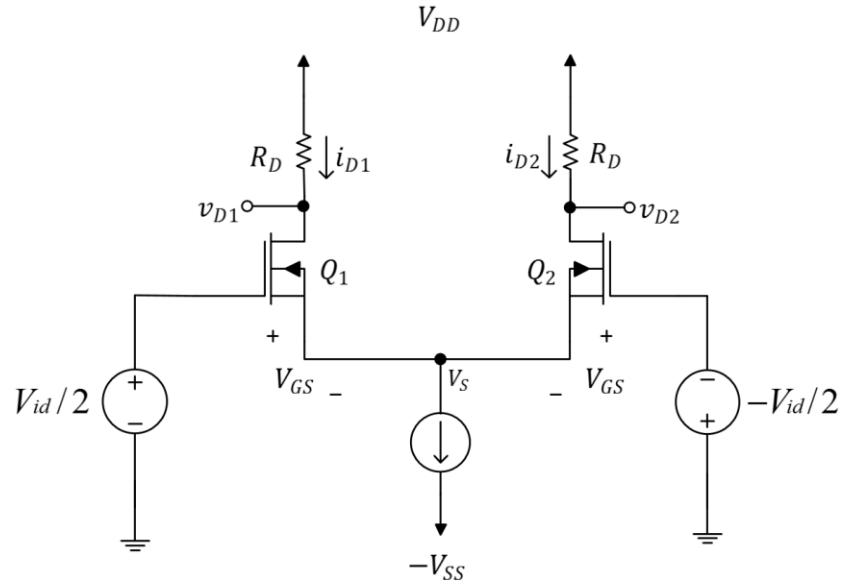


Figure 2.19 Different pair for the purpose of deriving the gain of differential mode [9]

There are input voltages with the same amount but not in the same phase on each gate terminal of the different pair. By using the MOSFET small signal model in figure 2.7, figure 2.19 can be redrawn in figure 2.20. Note that the parasitic capacitances are ignored for now.

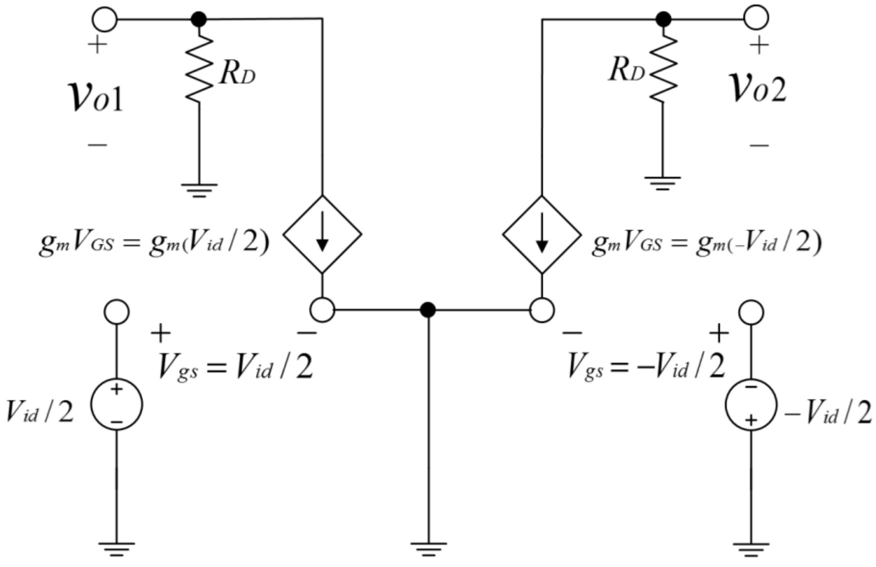


Figure 2.20 Small signal model of figure 2.19

The output voltages at the drain of Q_1 and Q_2 will be

$$v_{o1} = -g_m \frac{V_{id}}{2} R_D \tag{2.23}$$

$$v_{o2} = +g_m \frac{V_{id}}{2} R_D \tag{2.24}$$

The single-ended voltage gain of each transistor can be calculated as

$$\frac{v_{o1}}{V_{id}} = -\frac{1}{2} g_m R_D \tag{2.25}$$

$$\frac{v_{o2}}{V_{id}} = +\frac{1}{2} g_m R_D \tag{2.26}$$

The differential gain will be

$$A_d = \frac{v_{o2} - v_{o1}}{V_{id}} = g_m R_D \tag{2.27}$$

2.3.4 Common-Mode gain and Common-Mode Rejection Ratio (CMRR)

Before the deriving process of common-mode gain, take a look at the common-mode configuration in figure 2.15. The constant current source in that figure actually has a resistance R_{SS} but it is usually very large. The common-mode configuration with taking R_{SS} into consideration can be illustrated in figure 2.21.

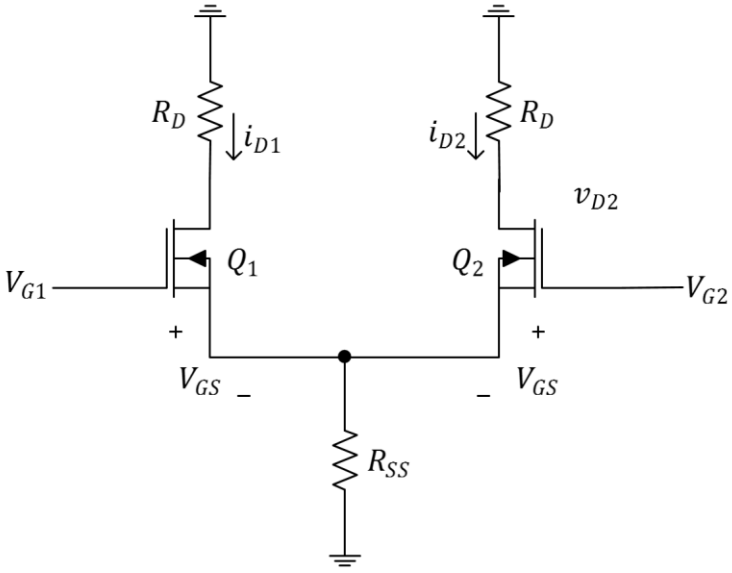


Figure 2.21 Common-mode configuration including source resistance [9]

To derive the gain of common-mode, figure 2.21 is redrawn into small-signal model which can be illustrated in figure 2.22.

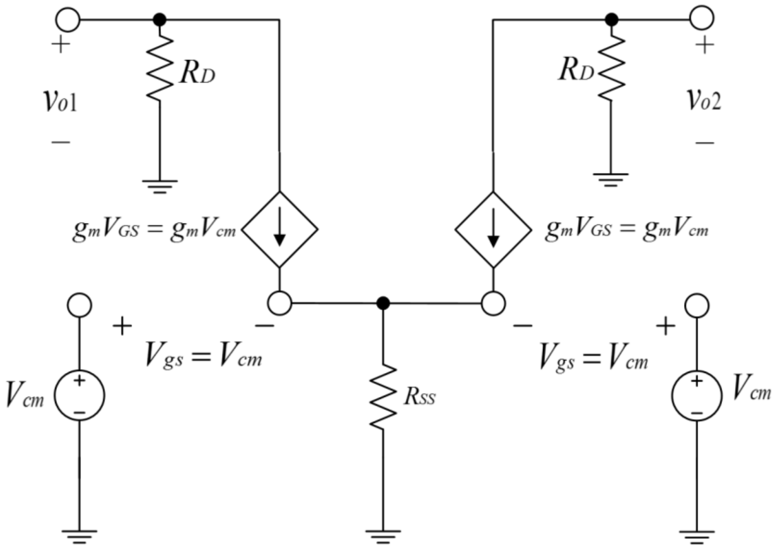


Figure 2.22 Small signal model of figure 2.21

The gate-to-source voltage at each transistor will be

$$V_{GS} = V_{cm}\frac{1}{1+2g_mR_{SS}} \tag{2.28}$$

and the output voltage at each transistor will be

$$v_{o(1,2)} = -g_mV_{GS}R_D = -\frac{R_D}{\frac{1}{g_m}+2R_{SS}}V_{cm} \tag{2.29}$$

Since the outputs of common-mode different pair have the same values, the common-mode gain with double-end output will be zero which can be shown in this equation.

$$\frac{v_{od}}{V_{cm}} = \frac{v_{o2}-v_{o1}}{V_{cm}} = 0 \tag{2.30}$$

Next will be the case where the load resistances R_D are not matched. Assuming that the load at Q_1 is R_D and the load at Q_2 is $R_D+\Delta R$, the output voltages for each transistor can be calculated using equation 2.29.

$$v_{o1} = -\frac{R_D}{2R_{SS}}V_{cm} \tag{2.31}$$

$$v_{o2} = -\frac{R_D+\Delta R}{2R_{SS}}V_{cm} \tag{2.32}$$

Note that the term $1/g_m$ in equation 2.29 is ignored for both equation since it is usually much smaller than the resistance R_{SS}. It can be clearly seen from equation 2.31 and 2.32 that the output voltages are now not the same values. The common-mode gain in equation 2.30 will not be zero anymore and it can be rewritten in this equation.

$$A_{cm} = \frac{v_{od}}{V_{cm}} = -\frac{\Delta R}{2R_{SS}} \tag{2.33}$$

The ratio of signals gain amplifier in differential-mode and the common-signal rejection gain in the common-mode is called Common-Mode Rejection Ratio (CMRR). The CMRR can be shown in this equation.

$$CMRR = \frac{|A_d|}{|A_{cm}|} \tag{2.34}$$

The highest value of CMRR occurs when there is no mismatch in the different pair ($A_{cm} = 0$). For the case that the different pair contains the mismatched value ΔR, the CMRR can be calculated in this equation.

$$CMRR = (2g_m R_{SS})/(\Delta R / R_D) \tag{2.35}$$

2.3.5 Parasitic capacitances effect on the different pair [10]

In order to determine the effect of parasitic capacitances, the figure 2.19 will be taken into consideration again. Since the different pair in figure 2.19 is perfectly symmetric, it can be redrawn into figure 2.23 using half-circuit technique.

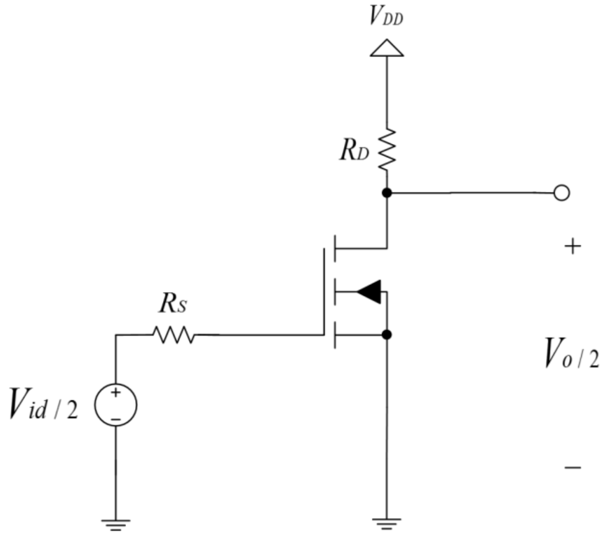


Figure 2.23 The Different pair using half-circuit technique [9].

Notice from the figure 2.23, the circuit configuration is identical to the configuration of a common-source amplifier. The effect of parasitic capacitances of differential pair can be alternatively calculated via this half circuit. The small-signal model of figure 2.23 can be illustrated in figure 2.24

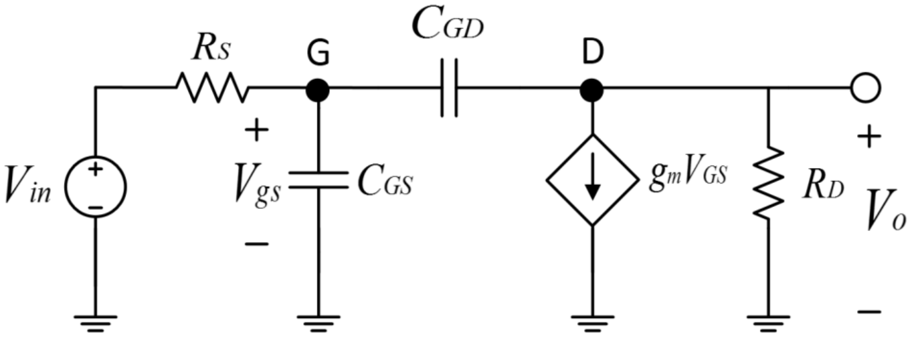


Figure 2.24 Small signal model of figure 2.23

Taking the nodal analysis on node G

$$V_G = (G_S + s(C_{GS} + C_{GD})) - V_{in}G_S - V_o s C_{GD} = 0 \tag{2.36}$$

where $G_S = 1/R_S$. Do it again on the output node D

$$V_o(sC_{GD} + G_D) - V_G sC_{GD} + g_m V_G = 0 \tag{2.37}$$

where $G_D = 1/R_D$ and $V_{GS} = V_G$. Rearranged equation 2.37 into

$$V_G = V_o\left(\frac{sC_{GD} + G_D}{-g_m + sC_{GD}}\right) \tag{2.38}$$

Substituting 2.38 into 2.36 will result in 2.39

$$V_o(G_D G_S + s[G_D(C_{GS} + C_{GD}) + G_S C_{GD} + g_m C_{GD}] + s^2[C_{GS}C_{GD}]) = -V_{in}G_S(g_m - sC_{GD}) \tag{2.39}$$

Multiplying 2.39 with $R_D R_S$, equation 2.39 can be taken in this format

$$\frac{V_o}{V_{in}} = \frac{-g_m R_D\left(1 - \frac{sC_{GD}}{g_m}\right)}{1 + sa + s^2 b} \tag{2.40}$$

where

$$a = R_S[C_{GS} + C_{GD}(1 + g_m R_D)] + R_D C_{GD} \tag{2.41}$$

and

$$b = R_D R_S C_{GS} C_{GD} \tag{2.42}$$

The transfer function at low frequency can be acquired by setting $s = 0$ in equation 2.40, which will result in.

$$A_d = -g_m R_D \tag{2.43}$$

From equation 2.40, it can be seen that this system has two poles and one zero. Assuming that the poles are real and the dominant pole $\omega_{p1} << \omega_{p2}$, the denominator term of equation 2.40 can be estimated in this format

$$D(s) \cong 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \tag{2.44}$$

Comparing equation 2.44 with the denominator in equation 2.40, the dominant pole can be estimated as

$$\omega_{p1} \cong \frac{1}{a} = \frac{1}{R_S[C_{GS} + C_{GD}(1 + g_m R_D)] + R_D C_{GD}} \tag{2.45}$$

The next pole will be

$$\omega_{p2} \cong \frac{1}{\omega_{p1} b} \approx \frac{g_m}{C_{GS}} \tag{2.46}$$

The MOSFET configuration of different pair in figure 2.19 will use the parameters in figure 2.6 so that the values of parasitic capacitances will be the same as the common-drain example ($C_{GS} = 11.59 fF$, $C_{GD} = 0.99 fF$ and). Setting the biasing current to $50\mu A$, the current in each transistor of the different pair will be $25\mu A$. Knowing the current in each transistor, the transcondctance g_m can be calculated to $0.19 mA/V^2$. Setting the other resistances to $R_S = 10k$ and $R_D = 1K$. The cut-off high frequency f_H is calculated to 1.237 GHz by using equation 2.45.

The more accurate value of f_H can be calculated using Pspice which the test circuit can be illustrated in figure 2.25. The frequency response of figure 2.25, which is the gain of differential pair can be illustrated in figure 2.26. The cursor of Pspice indicate the cut-off frequency f_H to 1.3119 GHz which make the error of estimated f_H using equation 2.45 equal to 5.7%.

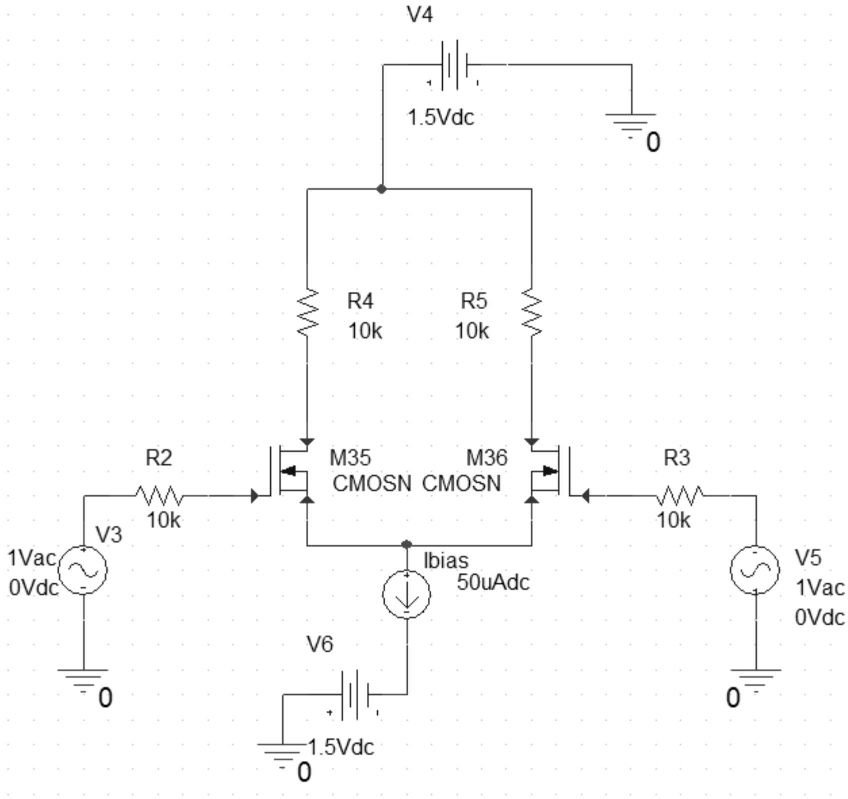
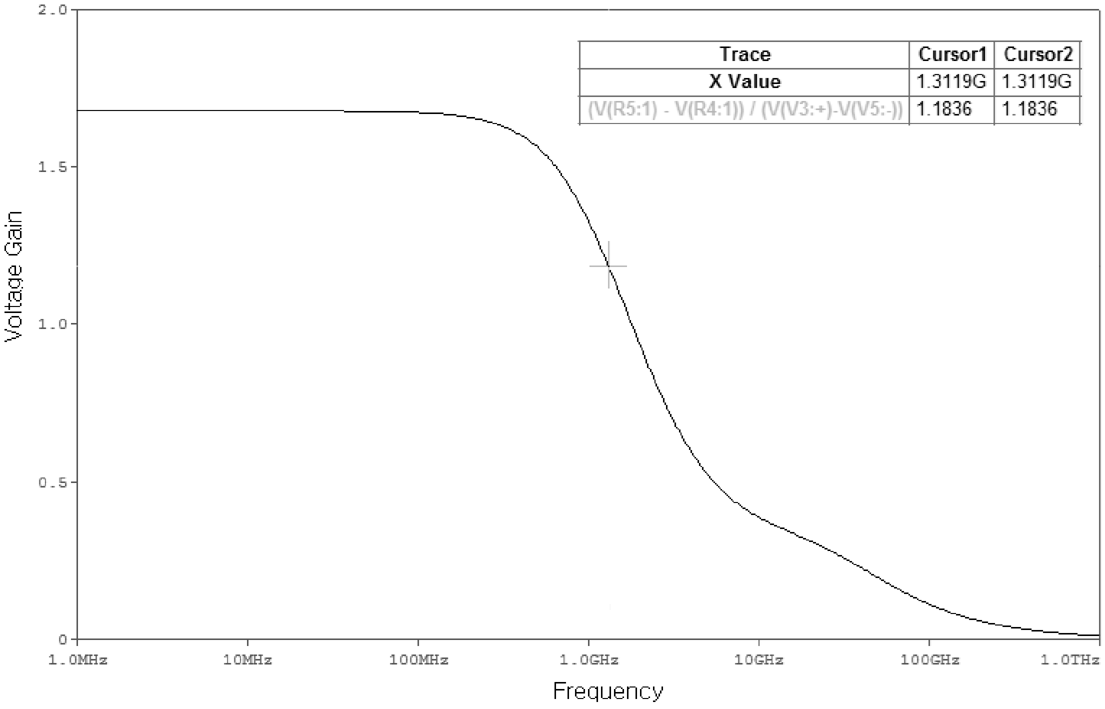


Figure 2.25 f_H testing circuit in Pspice for differential pair



Trace	Cursor1	Cursor2
X Value	1.3119G	1.3119G
(V(R5:1) - V(R4:1)) / (V(V3:+)-V(V5:-))	1.1836	1.1836

Figure 2.26 Frequency response of figure 2.25 with f_H measurement included

2.4 The Operational Transconductance Amplifier (OTA) [9]

In this section, The Operational transconductance amplifier (OTA) will be introduced as an example of basic building block. It is the combination of a differential pair and a current mirror as an active load which the whole circuit can be illustrated in figure 2.27.

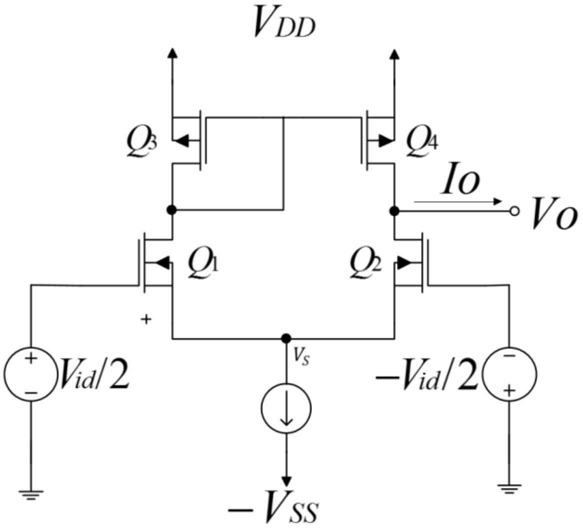


Figure 2.27 Structure of CMOS OTA [9]

To understand the operation of OTA, a small signal of figure 2.27 can be illustrated in figure 2.28.

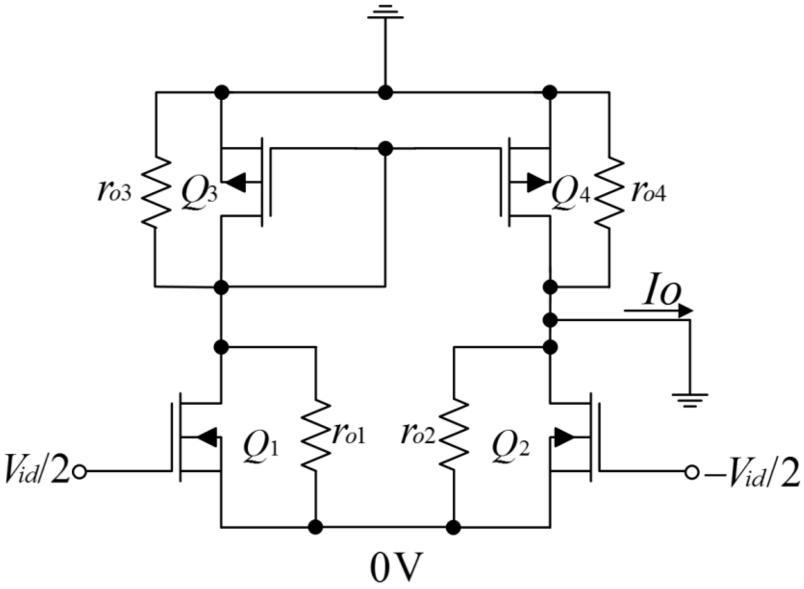


Figure 2.28 Small signal model of figure 2.27

Because the output node is shorted to the ground, it makes the circuit to perform in almost balanced fashion which the source of Q_1 and Q_2 can now assumed to be virtual ground. The equivalent circuit of small signal model in figure 2.28 can be alternatively illustrated in figure 2.29.

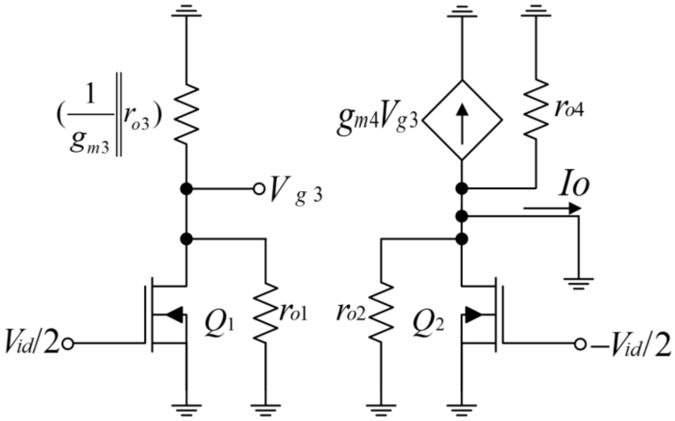


Figure 2.29 Equivalent circuit of figure 2.28

Note that the transistor Q_3 is replaced by equivalent resistance $(1/g_{m3} \| r_{o3})$. Using the property of differential mode of different pair, voltage at the gate of Q_3 can be found by using equation 2.23.

$$V_{g3} = -g_{m1}(\frac{V_{id}}{2})(\frac{1}{g_{m3}} \| r_{o3} \| r_{o1}) \tag{2.47}$$

Assuming that r_{o3} and $r_{o1} >> 1/g_{m3}$, equation 2.47 can be estimated to

$$V_{g3} \cong -(\frac{g_{m1}}{g_{m3}})(\frac{V_{id}}{2}) \tag{2.48}$$

This voltage also causes the current at Q_4 to be $g_{m4}V_{g3}$ which illustrated as dependent current source in figure 2.29. Because the output node is shorted to the ground, there will be no current in the output resistance r_{o2} and r_{o4}. The summation of current at output node will be

$$I_o = -g_{m4}V_{g3} + g_{m2}(\frac{V_{id}}{2}) \tag{2.49}$$

Substituting V_{g3} with equation 2.48, equation 2.49 will become

$$I_o = -g_{m1}(\frac{g_{m4}}{g_{m3}})(\frac{V_{id}}{2}) + g_{m2}(\frac{V_{id}}{2}) \tag{2.50}$$

Since $g_{m3} = g_{m4}$ and $g_{m1} = g_{m2} = g_m$, equation 2.50 can be shown as

$$I_o = g_m V_{id} \tag{2.51}$$

which is the main function of the OTA. The full circuit of OTA in figure 2.27 can be alternatively illustrated as a single block which can be shown in figure 2.10. Where the output current in figure 2.30 can be found as equation 2.52 using equation 2.51.

$$I_o = g_m(V_1 - V_2) = g_m V_{in} \tag{2.52}$$

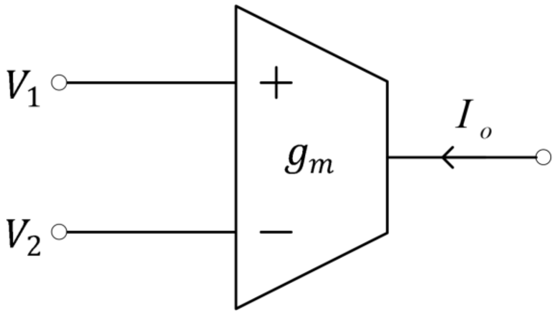


Figure 2.30 Operation transconductance amplifier as a building block

To determine the frequency response of OTA, consider the OTA circuit in figure 2.31. Note that C_L is the load capacitance that include parasitic capacitances of OTA which can be shown as

$$C_L = C_{GD2} + C_{GD4} + C_X \tag{2.53}$$

where C_X is the external load capacitance and is usually larger than parasitic capacitance of OTA.

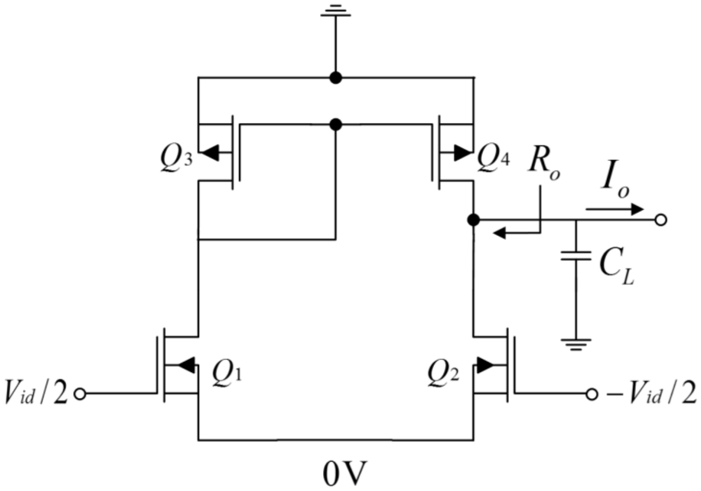


Figure 2.31 OTA circuit for the purpose of deriving transfer function

R_o is the output resistance that being seen at output port and can be estimated in equation 2.54 [2].

$$R_o = r_{o2} \parallel r_{o4} \tag{2.54}$$

Voltage at output port in figure 2.11 can be calculated as this equation

$$V_o = I_o(R_o \parallel C_L) = I_o \frac{1}{\frac{1}{R_o} + sC_L} \tag{2.55}$$

Substituting I_o with equation 2.51, equation 2.55 will become

$$V_o = g_m V_{id} \frac{R_o}{1 + sC_L R_o} \tag{2.56}$$

The voltage gain of OTA now can be shown as

$$\frac{V_o}{V_{id}} = (g_m R_o)(\frac{1}{1 + sC_L R_O}) \tag{2.57}$$

Note that the calculation in equation 2.57 is ignoring the parasitic capacitances in the other node since the output pole is often dominant. The OTA cut off frequency can be found as

$$f_H = 1/2\pi C_L R_O \tag{2.58}$$

The MOSFET configuration of OTA in figure 2.31 will use the parameters in figure 2.6 so that the values of parasitic capacitances will be the same as the differential pair example ($C_{GS} = 11.59 fF$, $C_{GD} = 0.99 fF$ and $g_m = 0.19 mA/V^2$). Set the biasing voltage to $\pm 1.5V$ and load capacitance to $1.5 pF$. The output resistance r_{o2} and r_{o4} in equation 2.54 can be found by calculating the inverse of slope $I_D - V_{DS}$ for various V_{GS} curve of transistors Q_2 and Q_4 which are resulting in $512 k\Omega$ and $1.32 M\Omega$ respectively. The cut-off high frequency is calculated to 287.614 kHz by using equation 2.58. The more accurate value of f_H can be calculated using Pspice which the test circuit can be illustrated in figure 2.32. The frequency response of figure 2.32, which is the voltage gain of OTA can be illustrated in figure 2.33. The cursor of Pspice indicate the cut-off frequency f_H to 323.764 kHz which make the error of estimated f_H using equation 2.58 equal to 11%.

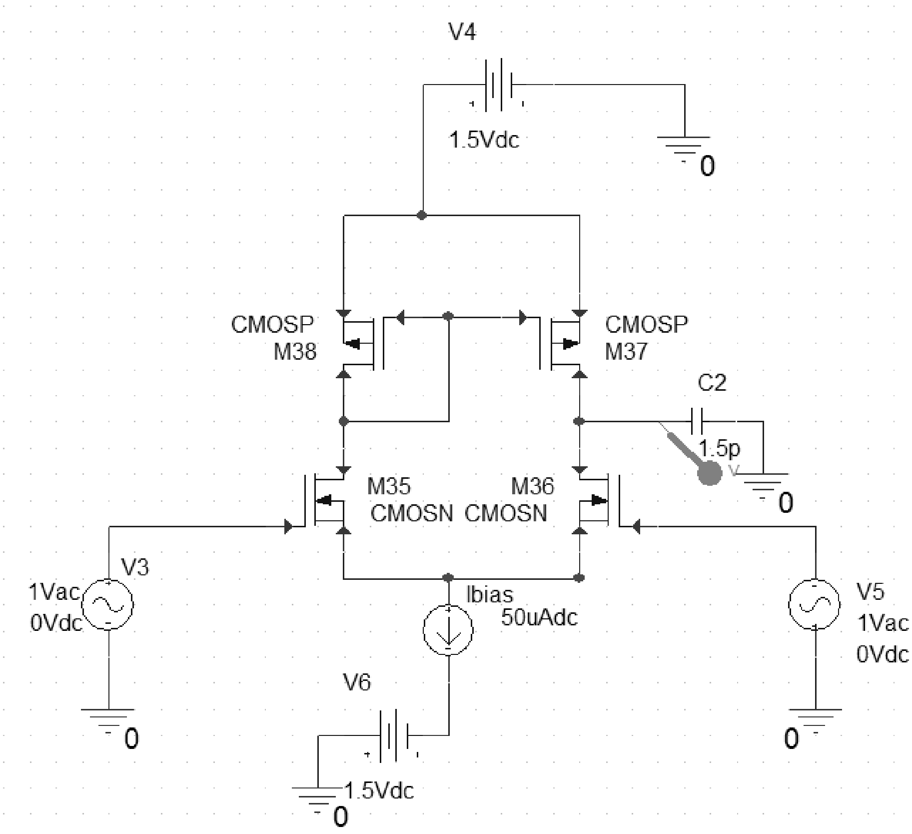
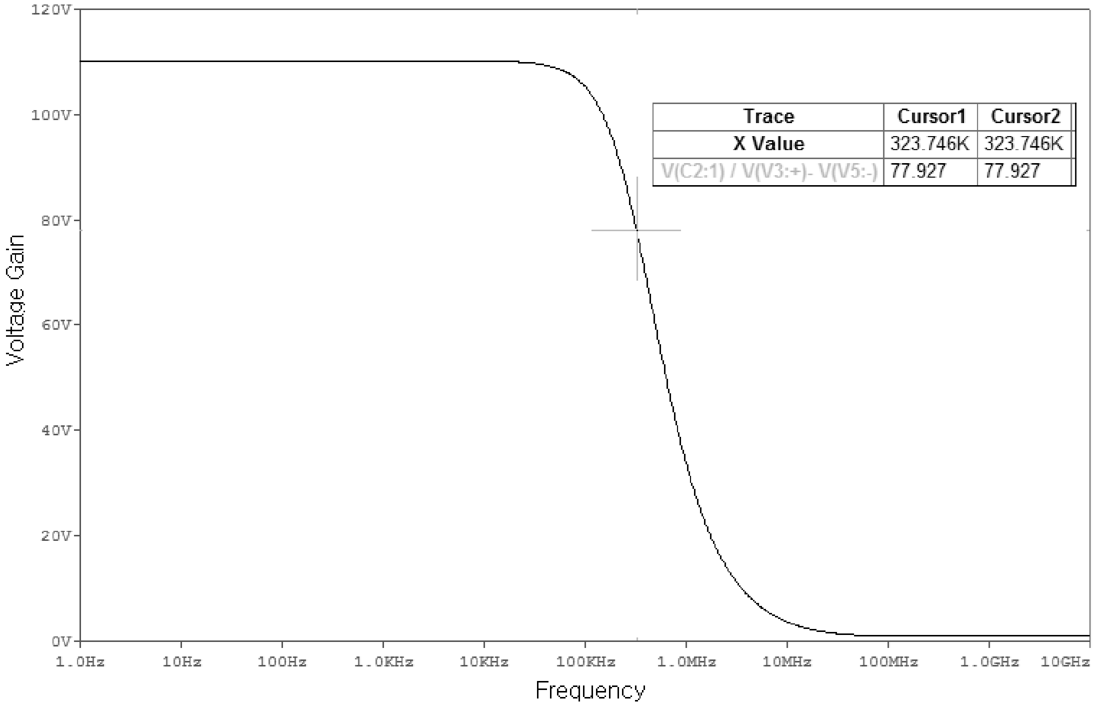


Figure 2.32 f_H testing circuit in Pspice for OTA



Trace	Cursor1	Cursor2
X Value	323.746K	323.746K
V(C2:1) / V(V3:+)- V(V5:-)	77.927	77.927

Figure 2.33 Frequency response of figure 2.32 with f_H measurement included

2.5 Summary

This chapter explains the characteristics of MOSFET and has a simulation on single transistor which TSMC 0.25μm is being used as an example. The example also included the effect of parasitic of transistors as well as how to calculate it using the parameters provided by MOSIS. This chapter also provide the application of MOSFETs such as common drain amplifier, differential amplifier, OTA as well as the frequency response of each circuit that being affected by the parasitic capacitances of transistor. The effect of parasitic that being study in this chapter will be important for the next chapter where the circuits that affected by parasitic capacitance are even more complicated

CHAPTER III

CURRENT BACKWARD TRANSCONDUCTANCE AMPLIFIER

3.1 Introduction

Follow the analysis on basic building block in the previous chapter, an active building block named current backward transconductance amplifier (CBTA) is introduced [11]. It is a combination of second generation current conveyor (CCII) and operational transconductance amplifier (OTA), which the latter is already analyzed in the previous chapter. This chapter will provide the derivation of CCII and the CBTA realization. In addition, the analysis on CBTA will also be provided. The topics are as follows; schematic symbols, characteristic, frequency response, non-ideality and loads effect. These analysis will be useful for the next chapter where CBTA is used as an application.

3.2 Second Generation Current Conveyor (CCII) [11]

The first generation current conveyor (CCI) was introduced by Sedra in 1986 [12]. After that, its development was reintroduced as Second Generation Current Conveyor (CCII) [2]. The structure of CMOS CCII can be illustrated in figure 3.1 and the derivation will be based on this figure.

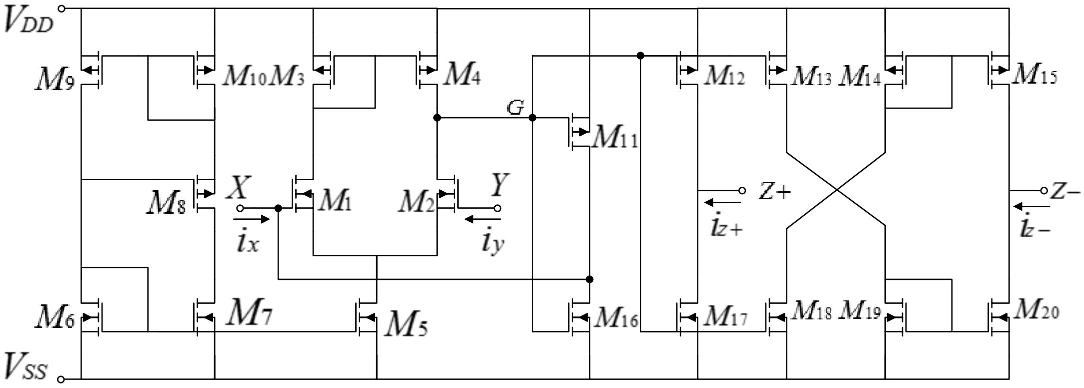


Figure 3.1 Second Generation Current Conveyor (CCII) [11]

To begin the derivation, assume that there is an input voltage V_Y being applied to port Y. Assumed that all the transistors operate in saturation region and are perfectly matched, the OTA part (M_1-M_4) will have the same drain current at M_1 and M_2 ($i_{D1} = i_{D2}$) as we described in previous chapter. Because of that, the voltages V_{GS} at M_1 and M_2 will be identical as a result of equation 2.2. The voltage V_X at port X will be forced to have the same value at the applied voltage V_Y .

$$V_X = V_Y \tag{3.1}$$

Because the port Y is basically the gate of a transistor M_2, there is no current in this port.

$$i_y = 0 \tag{3.2}$$

Next is the case where a current is being applied to port X or the current being generated by V_X connected to the load. Since the current cannot pass the gate of M_1, the current i_x will be split between the drain of M_{11} and M_{16} which can be shown in this equation.

$$i_x = i_{D16} - i_{D11} \tag{3.3}$$

Since the gate of M_{11}, M_{12}, M_{13} and M_{16}, M_{17}, M_{18} is being controlled by voltage V_G, the source to gate voltage V_{SG} of M_{11}, M_{12}, M_{13} can be written as

$$V_{SG(M_{11},M_{12},M_{13})} = V_{DD} - V_G \tag{3.4}$$

By using equation 2.2, the drain current at each transistor is

$$i_{D11} = i_{D12} = i_{D13} \tag{3.5}$$

For the transistors M_{16}, M_{17}, M_{18}

$$V_{GS(M_{16},M_{17},M_{18})} = V_G - V_{SS} \tag{3.6}$$

and the current is

$$i_{D16} = i_{D17} = i_{D18} \tag{3.7}$$

The current at port Z+ can be shown as

$$i_{z+} = i_{D17} - i_{D12} \tag{3.8}$$

From equation 3.5 and 3.7, equation 3.3 can be shown as

$$i_x = i_{z+} \tag{3.9}$$

For the next current mirror $M_{14}-M_{15}, M_{19}-M_{20}$, the drain current is

$$i_{D19}=i_{D13}=i_{D20} \tag{3.10}$$

and

$$i_{D14}=i_{D18}=i_{D15} \tag{3.11}$$

The current at port Z- can be shown as

$$i_{z-}=i_{D20}-i_{D15} \tag{3.12}$$

which also equals to

$$i_{z-}=-(i_{D16}-i_{D11})=-i_x \tag{3.13}$$

Equations 3.1, 3.2, 3.9, 3.13 can be alternatively expressed in matrix as [13]

$$\begin{bmatrix} i_y \\ V_X \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ i_x \\ V_Z \end{bmatrix} \tag{3.14}$$

The CCII in figure 3.1 can be alternatively shown as simple block as the figure 3.2

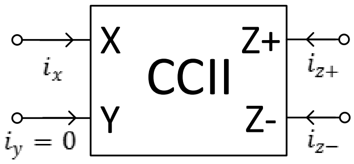


Figure 3.2 CCII as simple building block [13]

3.3 CBTA Realization [11]

Before going to the CBTA realization, let take a look at this modified version of OTA first.

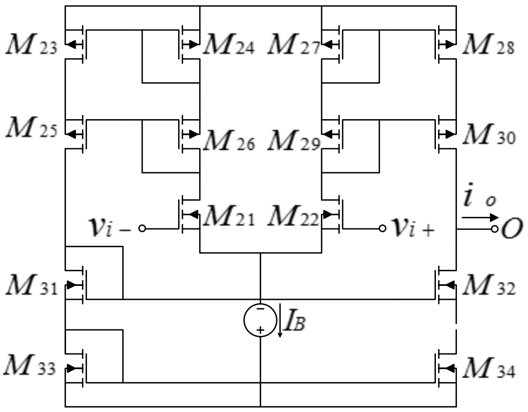


Figure 3.3 Modified OTA [11]

Although the figure 3.3 is slightly different from figure 2.27 in the previous chapter with the additional of cascode current mirror $M_{23}-M_{34}$, the operation of the circuit is still the same. The drain current at M_{30} can be expressed as

$$i_{D30} = g_m v_{i+} \tag{3.15}$$

The drain current of M_{32} can be expressed as

$$i_{D32} = g_m v_{i-} \tag{3.16}$$

The output current of figure 3.3 can be written as

$$i_o = i_{D30} - i_{D32} = g_m(v_{i+} - v_{i-}) = g_m v_{in} \tag{3.17}$$

which identical to equation 2.51 in the previous chapter.

For the CBTA realization, The CCII and OTA in figure 3.2-3.3 are connected in this following explanation. The drain of M_{30} or M_{32} is connected to the gate of M_2. The gate of M_{21} is connected to the drain of M_6. The gate of M_{22} is connected to the drain of M_9. The current mirror $M_{23}-M_{34}$ shares the same bias voltage as figure 3.1. the schematic symbol of connected circuit can be illustrated in figure 3.4.

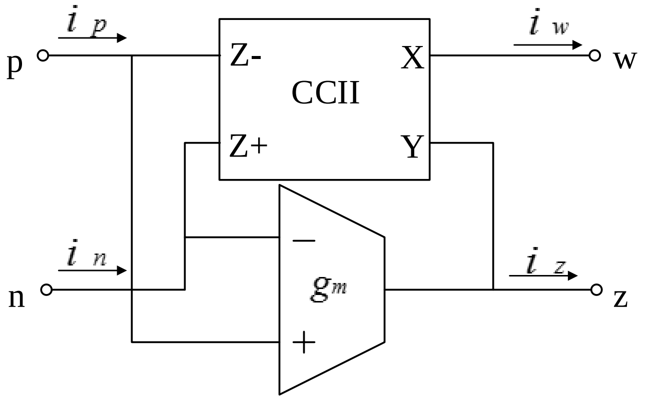


Figure 3.4 CBTA realization using CCII and OTA [11]

By using equation 3.2 and 3.17, the current i_z can be expressed as

$$i_z = g_m(v_p - v_n) \tag{3.18}$$

By using equation 3.1, the voltage v_w can be expressed as

$$v_w = v_z \tag{3.19}$$

Because the input port of OTA is basically the gate terminals, the current will not interfere with z-ports of CCII. Using equation 3.9 and 3.13 the current at p-port and n-port can be written as

$$i_w = i_p = -i_n \tag{3.20}$$

Equations 3.18-3.20 can be alternatively expressed in matrix as [11]

$$\begin{bmatrix} i_z \\ v_w \\ i_p \\ i_n \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \tag{3.21}$$

where the left hand side of the matrix is the parameter that being influenced by the parameters in the far right hand side of the matrix multiplied by the coefficient matrix that stand next to it. The structure of CBTA, schematic symbol and equivalent circuit can be illustrated figure 3.5, 3.6 and 3.7 respectively.

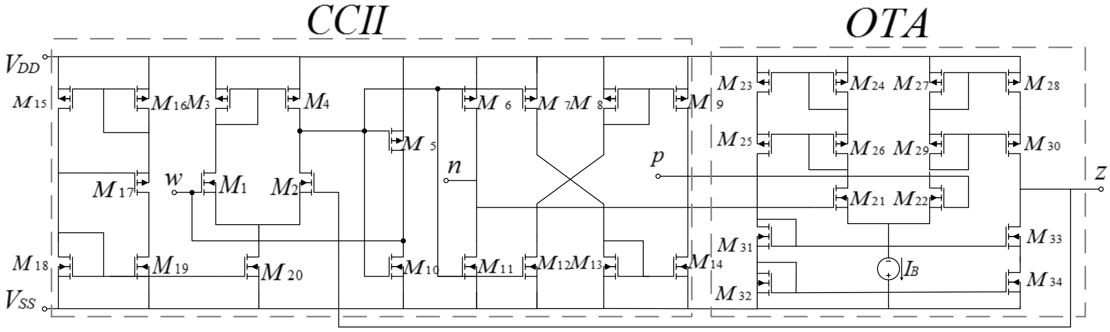


Figure 3.5 Structure of CBTA [11]

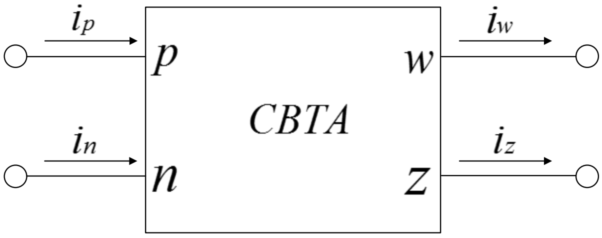


Figure 3.6 Schematic symbol of CBTA [11]

Unfortunately, there are errors occurred between theory and simulation. Equation 3.21 will not give the exact result in the simulation. These errors will be explained in the next section.

3.4 Non-ideal and Parasitic Effect of CBTA

In reality, the building blocks cannot perform at theirs full potential. The investigation on the non-ideal characteristic parameter of CBTA will be described in this section. Since the characteristic at each port of CBTA made of the differential pairs and current mirrors, the mismatch between transistors pairs will cause the errors and the parasitic capacitances of each transistor will affect the frequency response of CBTA. Assumed that the exact response values of each port can be defined by its ideal value multiplied by the non-ideal parameters, the non-ideal model of CBTA can be illustrated in figure 3.7. The non-ideal parameters $g_m(s)$, μ_w, $\alpha_p(s)$ and $\alpha_n(s)$ in figure 3.7 are transconductance, voltage gain and the current gain respectively.

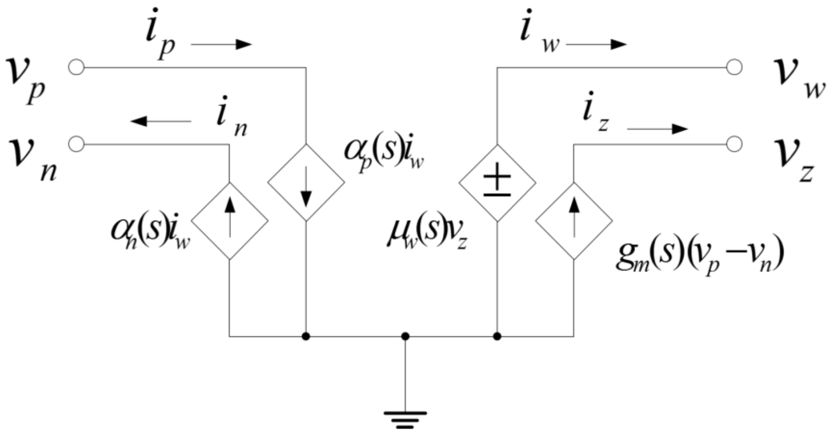


Figure 3.7 Equivalent circuit of CBTA with non-ideal parameters [11]

In order to define the equation for each non-ideal parameter, the response values from the simulation need to be acquired. The CBTA in figure 3.5 will be simulated using TSMC $0.25\mu m$ which parameters are listed in figure 2.3. The dimension of each transistor in figure 3.5 can be shown in table 3.1 [11]. With $\pm 1.5V$ voltage supplies and $50\mu A$ bias current, the transconductance g_m can be calculated using equation 2.4 ($g_m = 2\sqrt{KI_D}$). The conduction coefficient can be calculated using equation 2.3 ($K = \frac{1}{2}\mu_0 C_{OX}\frac{W}{L}$). The gate oxide capacitance per unit area C_{OX} in equation 2.3 can be calculated as.

$$C_{OX} = \varepsilon_{OX} / t_{OX} \qquad (3.22)$$

PMOS Transistors	W(μm)/L(μm)
$M_3 - M_9$	20/1
M_{15}	1/0.25
$M_{16}, M_{17}, M_{23} - M_{27}, M_{29}$	2.5/0.25
M_{28}, M_{30}	10/0.25
NMOS Transistors	W(μm)/L(μm)
M_1, M_2, M_{13}, M_{14}	10/1
$M_{10} - M_{12}$	2.5/1
M_{18}, M_{19}	0.5/0.25
M_{20}	2.5/0.25
M_{21}, M_{22}	2/0.25
M_{31}, M_{32}	2.25/0.25
M_{33}, M_{34}	10/0.25

Table 3.1 Dimension for transistors of CBTA [11]

Since the relative permittivity of SiO_2 ε_0 is 3.9, the permittivity of gate oxide can be calculated as $\varepsilon_{OX} = 3.9 \times \varepsilon_0 = 3.9 \times 8.85 \times 10^{-12} = 0.0345 fF / \mu m^2$. The parameter of TSMC $0.25\mu m$ in figure 2.3 illustrated that $TOX = 5.7nm = 0.0057\mu m$. The gate oxide capacitance can be calculated to $C_{OX} = 0.0345 / 0.0057 = 6.05 fF / \mu m^2$. Since figure 2.3 also illustrated that $UO = 336.114 cm^2 / V \cdot s$, the multiplication of μ_0 and C_{OX} is $\mu_0 C_{OX} = 336.114 \times 6.05 \times (0.1) \mu A / V^2 = 203.348 \mu A / V^2$. The transistors that responsible for transconductance are M_{21} and M_{22} and the channel width-length of this transistors are 2/0.25 according to table 3.1. Using equation 2.3, the conduction coefficient can be calculated as $K = 0.5 \times 203.348 \times 10^{-6} \times (2/0.25) = 813.392 \mu A / V^2$. Using equation 2.4, the value of transconnductance g_m for CBTA can be calculated as $g_m = \sqrt{4 \times 813.392 \times 50 \times 0.5 \times 10^{-12}} = 0.285 mS$.

Start with z-port, the simulation value of transconductance can be illustrated in figure 3.8. From the cursor 2 in the figure 3.8, the simulation value of transconductance g_m can be found as $0.212 mS$ for low frequency. The percent error between the simulation and theory can be defined as transconductance tracking error ε_{gm}, which is $\varepsilon_{gm} = (0.285 - 0.212 / 0.285) \times 100 = 25.6\%$. From the figure 3.8, the corner frequency of transconductance can be found as $565MHz\,(\omega_{gm} = 3550Mrad/s)$ using cursor 1.

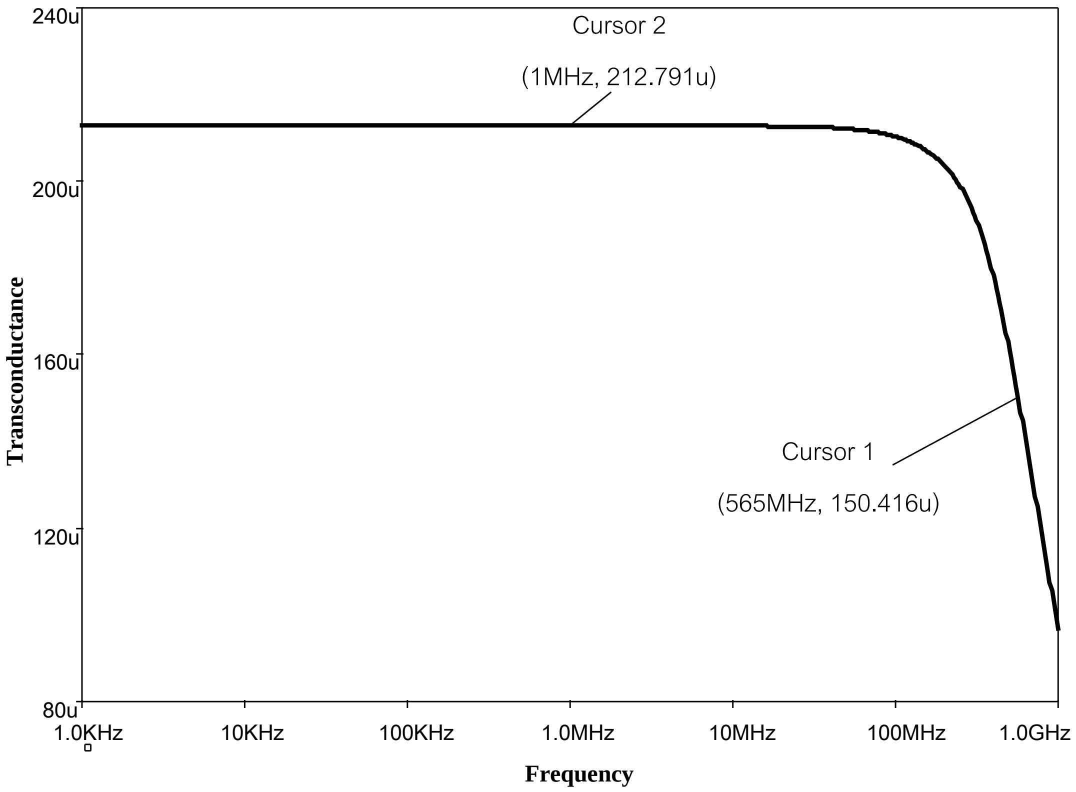


Figure 3.8 Bode plot of Transconductance $|I_z/(V_p - V_n)|$

The transconductance value in figure 3.8 can be written in equation 3.23

$$g_m(s) = [(0.285mS)(3550Mrad/s)(1-0.217)]/(s+(3550Mrad/s)) \quad (3.23)$$

The general form of non-ideal parameter $g_m(s)$ which including the transconductance error and the corner frequency can be expressed in this equation

$$g_m(s) = g_0\omega_{gm}(1-\varepsilon_{gp})/(s+\omega_{gm}) \quad (3.24)$$

where the parameter g_0 is the theory value of transcondcutance. The ω_{gm} is the cut-off corner frequency which caused by parasitic capacitances of transistors. The ε_{gp} is the different between the ideal value of transconductance and the non-ideal value that can be acquired through the simulation. The non-ideality for other three ports can also be described in the similar fashion.

The next investigation will be on voltage gain between w-port and z-port. The simulation result of voltage gain between these ports can be illustrated in figure 3.9. In the figure 3.9, the voltage gain for low frequency can be found as 0.983. Since the ideal gain value is unity, the percent error between value of simulation and theory can be found as $\varepsilon_{\mu} = (1 - 983.025m) \times 100 \approx 1.9\%$. From the figure 3.9, the corner frequency of this voltage gain can be found as $420MHz(\omega_{\mu} = 2639 Mrad/s)$. The general equation for voltage gain in figure 3.9 can be expressed as

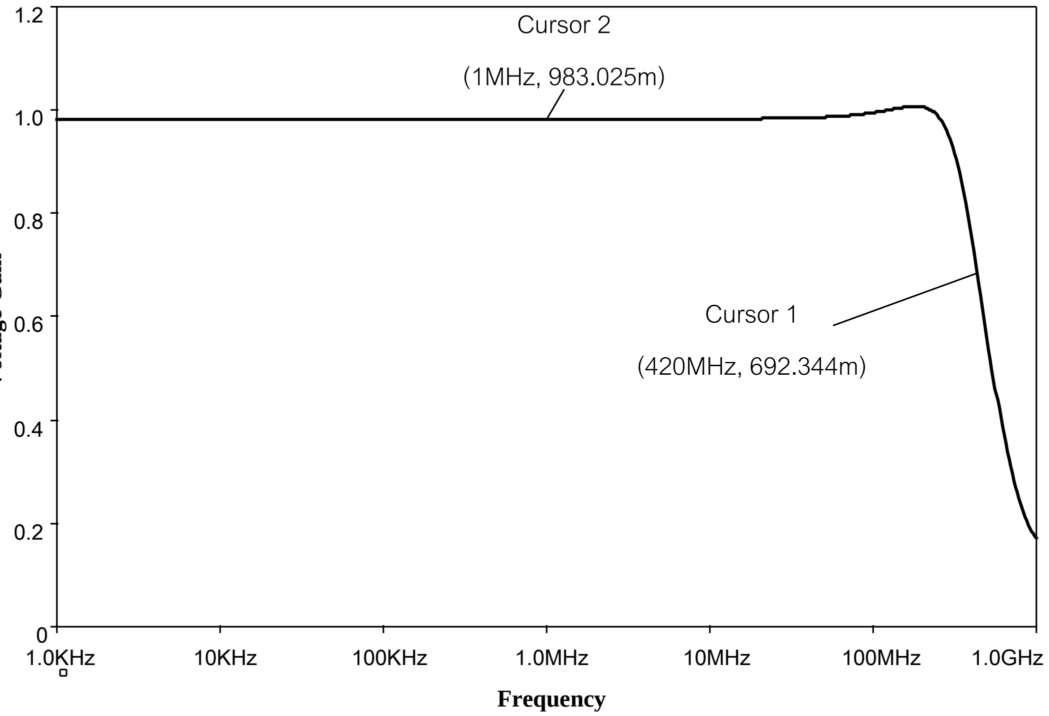


Figure 3.9 Bode plot of Voltage gain $|V_w / V_z|$

$$\mu_w(s) = \omega_w (1 - \varepsilon_w)/(s + \omega_w) \tag{3.25}$$

where ω_w is the -3dB corner frequency of voltage transfer function between voltage of w-port and z-port. The ε_w is voltage tracking error which is the different between the ideal voltage gain and the value of gain that can be acquired by simulation ($\varepsilon_w = 1 - Gain_{Simulation}$). In ideal case ($\varepsilon_w = 0$), this non-ideality function of voltage gain is unity $(\mu_w(s) = 1)$.

The next investigation will be the current gain between p-port and w-port. The simulation result of current gain between these ports can be illustrated in figure 3.10. In the figure 3.10, the current gain for low frequency can be found as 1.0269

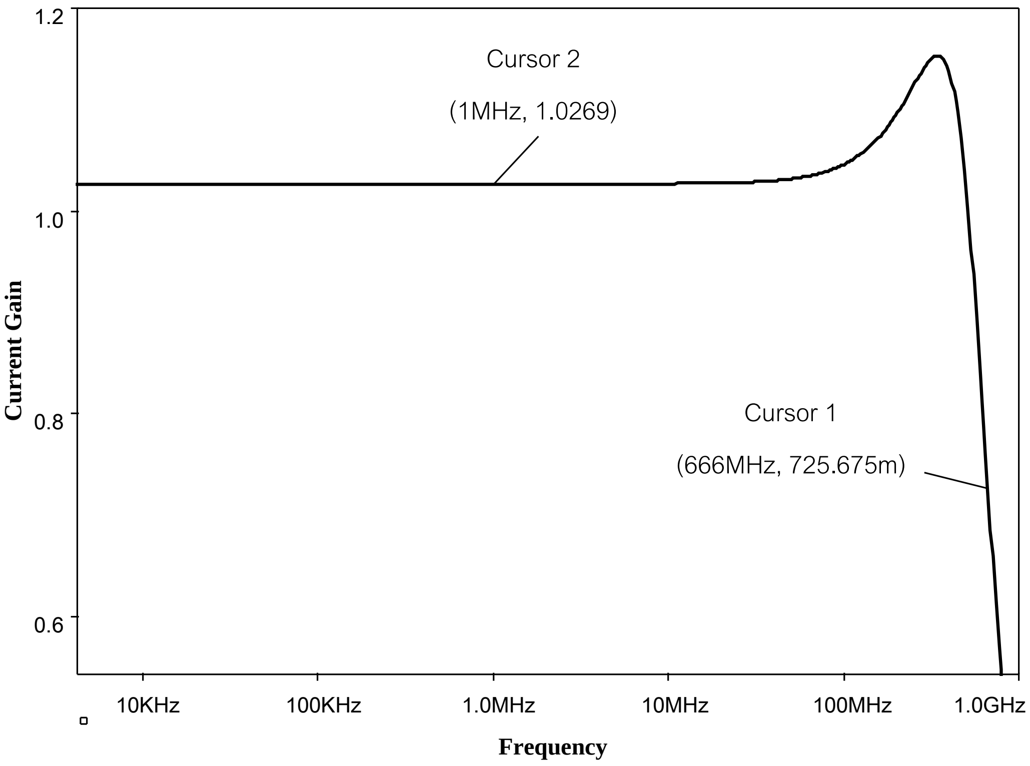


Figure 3.10 Bode plot of Current gain $\left|I_p / I_w\right|$

Since the ideal gain value is unity, the percent error between the value of simulation and theory can be found as $\varepsilon_{\alpha p} = (1-1.0269)\times 100 \approx 2.69\%$. From the response in the figure 3.10, the corner frequency of this current gain can be found as $666MHz(\omega_{\alpha p} = 4184Mrad/s)$. The general equation for current gain in figure 3.10 can be expressed as

$$\alpha_p(s) = \omega_{\alpha p}(1-\varepsilon_{\alpha p})/(s+\omega_{\alpha p}) \tag{3.26}$$

where $\omega_{\alpha p}$ are the -3dB corner frequencies of current between p-port and w-port. The $\varepsilon_{\alpha p}$ is current tracking errors which is the different between the ideal value of current gain and the value of gain that can be acquired by simulation ($\varepsilon_{\alpha p} = 1 - Gain_{Simulation}$). In ideal case ($\varepsilon_{\alpha p} = 0$), this non-ideality parameter of current gain is unity $(\alpha_p(s) = 1)$.

The last investigation will be the current gain between n-port and w-port. The simulation result of current gain between these ports can be illustrated in figure 3.11.

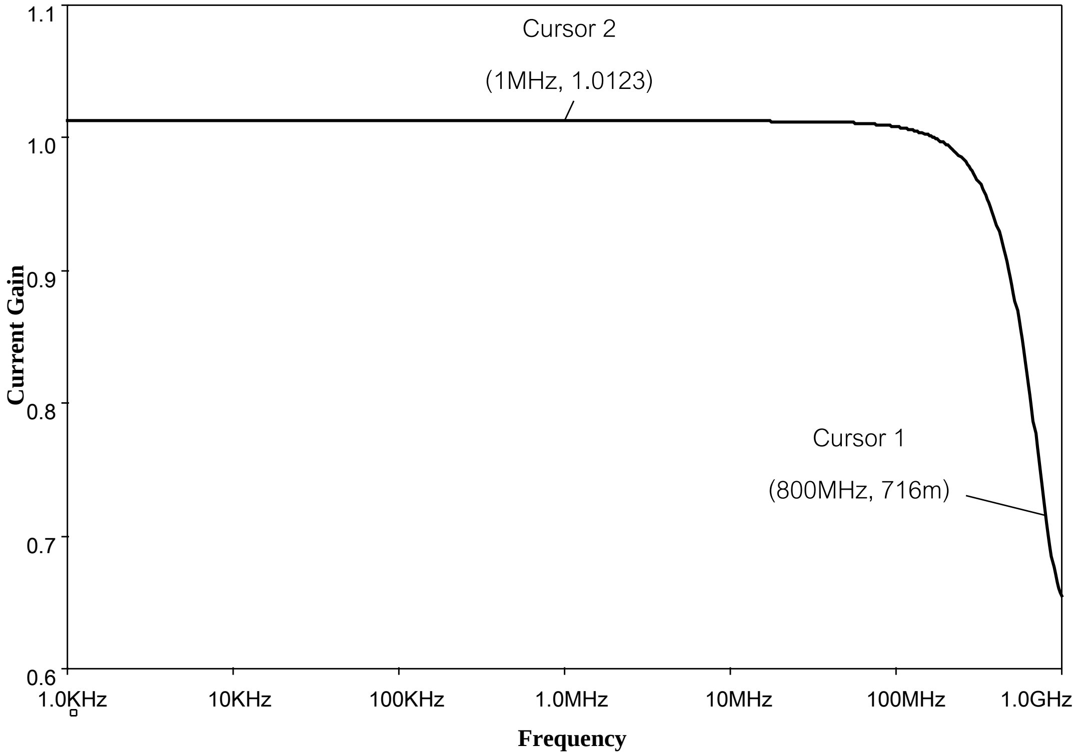


Figure 3.11 Bode plot of Current gain $|I_n / I_w|$

In the figure 3.11 the current gain for low frequency can be found as 1.0126. Since the ideal gain value is unity, the percent error between the value of simulation and theory can be found as $\varepsilon_{\alpha n} = (1-1.0126)\times 100 \approx 1.26\%$. From the figure 3.11, the corner frequency of this current gain can be found as $800MHz(\omega_{\alpha n} = 5026Mrad/s)$. The general equation for current gain in figure 3.11 can be expressed as

$$\alpha_n(s) = \omega_{\alpha n}(1-\varepsilon_{\alpha n})/(s+\omega_{\alpha n}) \tag{3.27}$$

where $\omega_{\alpha n}$ are the -3dB corner frequencies of the current between n-port and z-port. The $\varepsilon_{\alpha n}$ is current tracking errors which is the different between the ideal value of current gain for this port and the value of gain that can be acquired by simulation ($\varepsilon_{\alpha n} = 1 - Gain_{Simulation}$). In ideal case ($\varepsilon_{\alpha n} = 0$), this non-ideality parameter of current gain is unity $(\alpha_n(s) = 1)$.

Combining the general equation of non-ideal parameters (3.24, 3.25, 3.26 and 3.27), the CBTA characteristic equation 3.21 can be rewritten as

$$\begin{bmatrix} i_z \\ v_w \\ i_p \\ i_n \end{bmatrix} = \begin{bmatrix} g_m(s) & -g_m(s) & 0 & 0 \\ 0 & 0 & \mu_w(s)v_z & 0 \\ 0 & 0 & 0 & \alpha_p(s) \\ 0 & 0 & 0 & -\alpha_n(s) \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \tag{3.28}$$

The maximum operating frequency of CBTA is $f_{\max} = \min\{f_{\alpha p}, f_{\alpha n}, f_{gm}, f_{\mu}\} \approx 420$ MHz. Note that all of these responses are done without taking the load effect into consideration to let the CBTA perform in the best condition. The short explanation of load effect on CBTA on the z-port is provided here as an example. Since the z-port is realized by OTA, the frequency response of z-port will be heavily affected by the load that being connected to that port. This assumption is already described in the last chapter, which is equation 2.58 ($f_H = 1/2\pi C_L R_O$) where the load is directly affected the pole of transfer function. Note that this port is an input port that being used to setup the parameters in the other ports. The effect of load at this port will also be carried out to the other port. Since the design of circuit need the CBTA to be connected to many type of load, the investigation of load effect is important. The next section will be the simulation on the CBTA performance when the various type of loads are presented.

3.5 The effect of load on CBTA

The next chapter will be the designation of inductance simulator based on CBTA where z-port is connected to capacitor and w-port is connected to resistor. But the connecting of those loads affect the gain and the frequency response of CBTA. Thus the reasons why the investigation on the effect of load will be described in this section. The purpose of this investigation is to identify the appropriate range of load that let the CBTA perform at its fully potential. The first test is to fix the resistor R_w at w-port to a certain value and try out the different values of capacitor C_z at z-port. As for the result, the frequency response, gain and transconductace value that specified for each port will be analyzed. By doing this, the appropriate range of C_z where the

CBTA has low error can be acquired. For the second test, this time the value of capacitor C_z is being fixed and the different values of resistor R_w will be tried. Similar to the first test, the appropriate range of R_w will be acquired. As for the configuration of a testing circuit, it can be illustrated in figure 3.12.

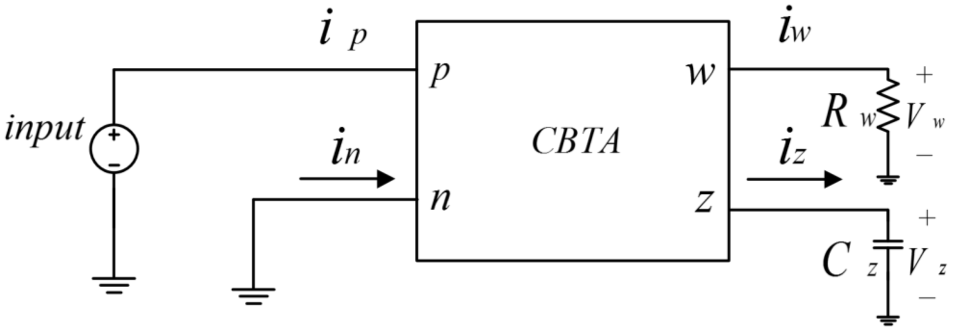


Figure 3.12 Testing circuit for determine the load effect of CBTA

To start the analysis, the biasing supply, the transistors specification and the dimension for each transistors will be the same as the previous experiment, which the transconductance to be calculated to 0.285mS. As seen from the figure 3.12, a single input signal is applied to a test circuit for this test scheme. By doing this, the responding signals will be generated at each port of CBTA and are the values that going to be analyzed. Note that the responding signals are mostly the values of gain and transconductance that should be represented the characteristic of CBTA.

As for the first test, the fixed value of resistor $R_w = 1k\Omega$ will be assigned. As for the reason, it is a common value that can be easily found and do not generate error for the test circuit. For the reason that $R_w = 1k\Omega$ provided no error, the detail about effect of R_w will be on the second test. For now, the concentration point will be on the effect of the load capacitance C_z. Start with z-port, the value that going to be analyzed here is transconductance ($g_m = I_{out}/V_{in}$). The values of capacitor C_z that going to be tried are $1pF$,$1nF$,$1\mu F$ and $1mF$. By doing the simulation, the result of the transconductance value for the different values of capacitors can be illustrated in the figure 3.13.

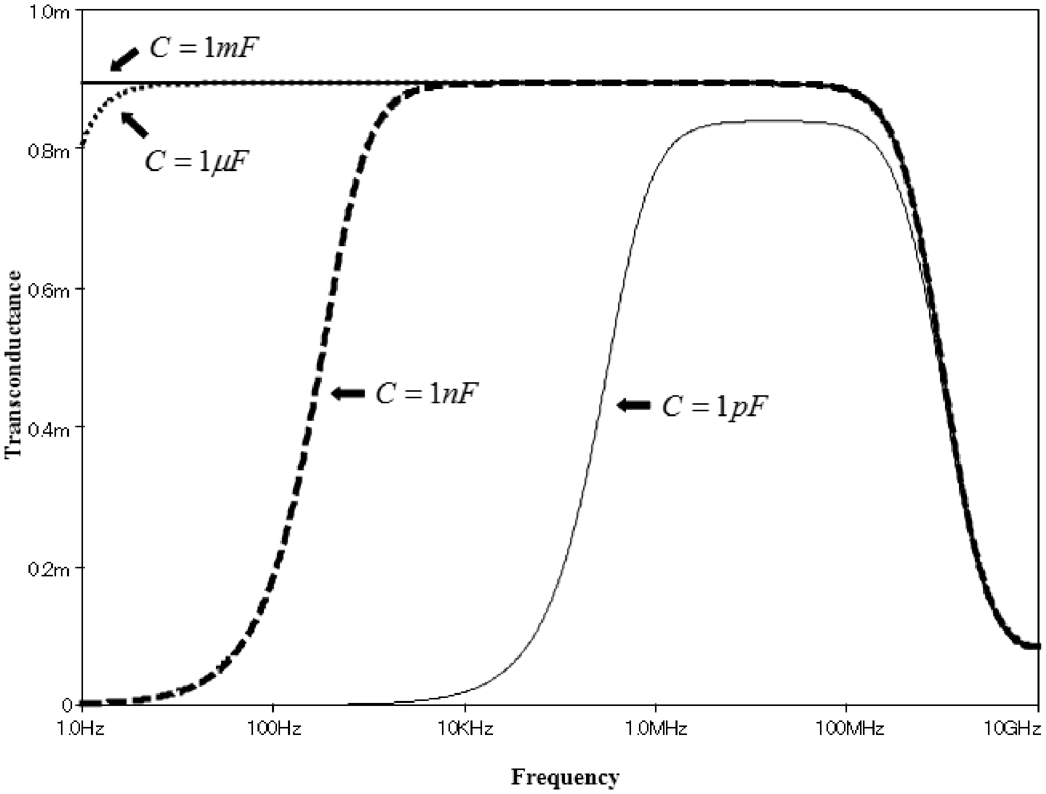


Figure 3.13 The transconductance for the different values of capacitance loads.

It can be seen from the above figure that the -3dB high-end corner frequency is not really different and can be estimated as 671 MHz. For the matter of amplitude of transconductance, it can be seen that the flat band of line for $C_z = 1pF$ in figure 3.13 has lower value while comparing to the other line. This is the transconductance error and it means that $C_z = 1pF$ is not appropriated to use for this setup. Since the amplitude the flat band of line for $C_z = 1nF$ contains no error, the appropriated lowest value of capacitor must be existed between $1pF$ and $1nF$. By slowly increasing the capacitance C_z from $1pF$, the new lowest value without the transconductance error arised from capacitor C_z can be found as $25pF$, which the result illustrated in the figure 3.14. As seen in figure 3.14, the transconductance at the flat band for both C_z are now almost identical.

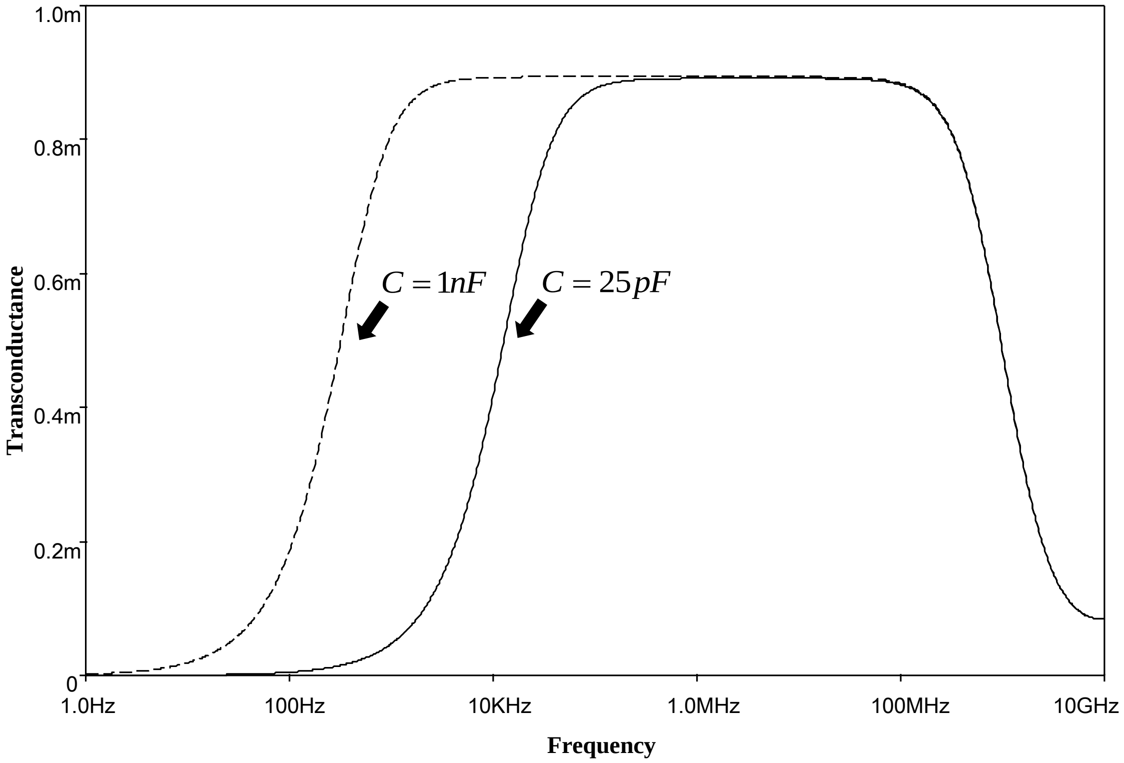


Figure 3.14 The transconductance values for load capacitor $25pF$ and $1nF$.

Since this is the load capacitance that connected to z-port, there will be no current in this port $(1/sC=\infty=open-circuit)$ for the value of capacitor that too low or the CBTA operation at low frequency. As seen from figure 3.14, the line for $C_z=25pF$ has low-end corner frequency at 100 kHz. It means that the capacitance value of $C_z=25pF$ is not appropriated to be used at the frequency lower than 100 kHz. For the increasing value of C_z, the lower frequency operation range can be extended. Note that increases in the value of capacitor resulting in the size of the capacitor and the circuit power consumption.

Now, the next test will be the effect of capacitor C_z on the relationship between the voltage of w-port and z-port ($V_w=V_z$). The analysis will be on the voltage at w-port which being influence by voltage at z-port. The values of capacitor that going to be used this time is as follow; $25pF$, $1nF$, $1\mu F$ and $1mF$. Note the capacitance $25pF$ is the value that being acquired by the last test. The simulation result of voltage at w-port can be illustrated in figure 3.15.

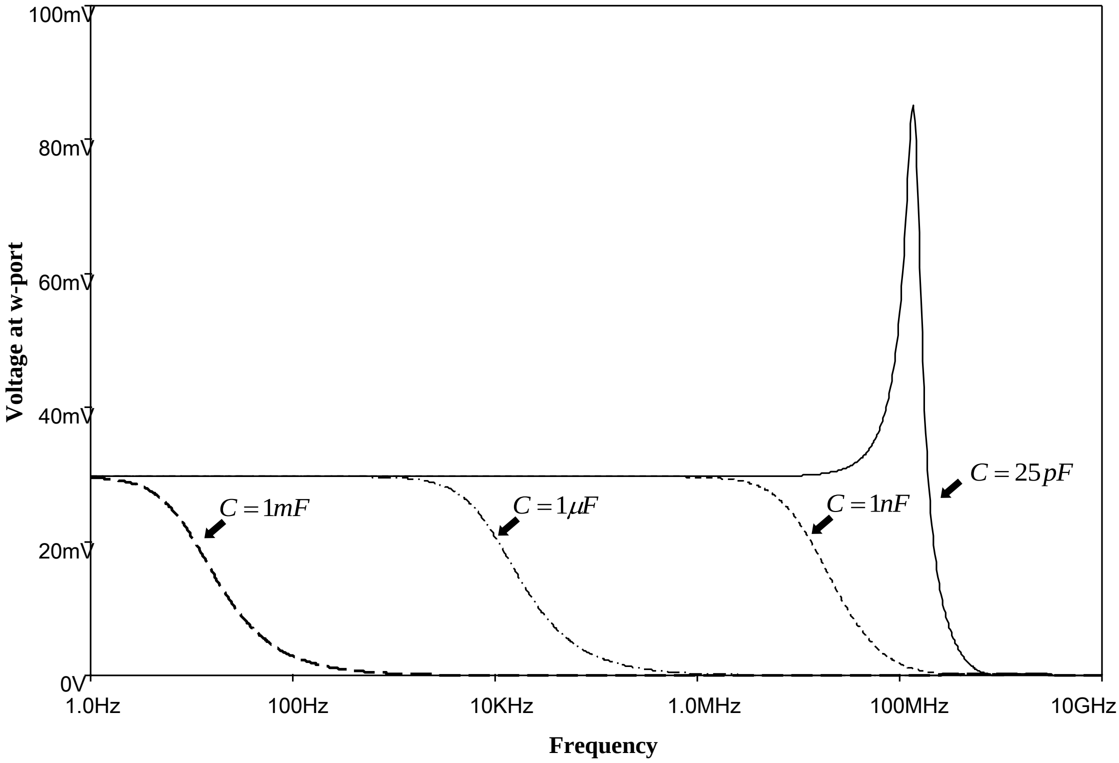


Figure 3.15 The voltage of w-port for the different values of capacitance loads.

It can be seen from the figure 3.15 that there is an overshoot for the capacitance load of $25pF$. It means this capacitance value again cannot be used. From the simulation result in figure 3.15, the line for $C_z = 1nF$ does not contain overshoot. Because of that, the lowest value of C_z that the circuit contains no error can be located between $25pF$ and $1nF$. By slowly increasing the capacitance load in the simulation program, the new lowest value without the overshoot arised from a load capacitance C_z can be found as $380pF$, which the new result can be illustrated in figure 3.16. Unlike the response from the last test, the effect of load capacitance on the corner frequency can be clearly seen. By using the cursor of simulation program, the -3dB corner frequency for the capacitance load $380pF$, $1nF$, $1\mu F$ and $1mF$ can be estimated as 43 MHz, 12 MHz, 9.6 kHz and 9 Hz respectively. It can be seen that increasing in C_z result in the decreasing of corner frequency. That why the capacitor C_z must be kept small to achieve high frequency operation.

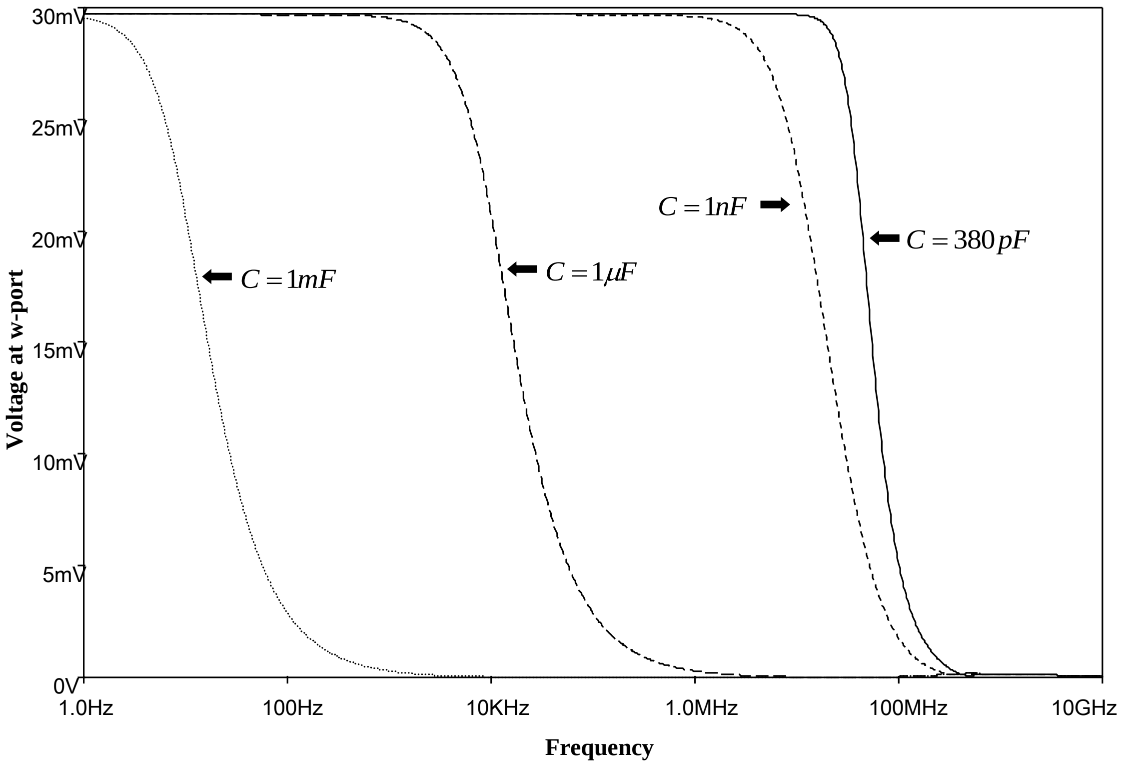


Figure 3.16 The new frequency response of voltage at w-port

The next test will be the effect of capacitor C_z on the relationship between current at w-port, p-port and n-port ($i_w = i_p = -i_n$). Since the independent current source is being connected to p-port, the analysis on the corner frequency cannot be done on this port ($f_{H-Source} \neq f_{H-(p)port}$). The investigation can be alternatively done to n-port since they share the same topology. The value that going to be analyzed in this case will be the current gain (i_n / i_w) for the different value of C_z. The values of load capacitance C_z that is going to be tested as follows; $380pF$,$1nF$,$1\mu F$ and $1mF$. Note that $380pF$ is the value of C_z that being acquired by last test. The simulation result for the current gain (i_n / i_w) can be illustrated in figure 3.17. By using the cursor of simulation program, the -3dB corner frequency for the load capacitance $380pF$,$1nF$,$1\mu F$ and $1mF$ can be estimated as 87 MHz, 50 MHz, 1.58 MHz and 49 kHz respectively. Same as the last test, increasing in C_z result in the decreasing of corner frequency.

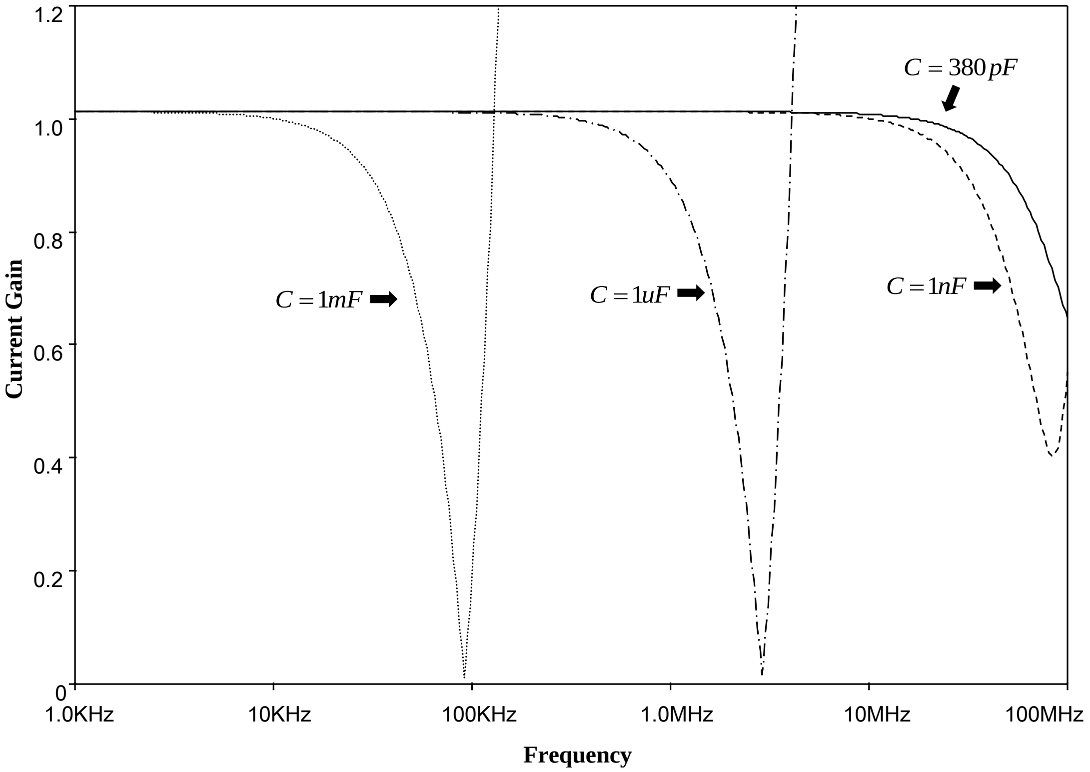


Figure 3.17 The current gain of n-port and w-port for difference value of C_z

As seen in figure 3.17, there is no error in the gain for $C_z = 380pF$ this time (Gain=1). It means that there is no need to look for the lowest value of C_z. With all the investigation has been done to all the ports of CBTA, the best possible value of load capacitance for z-port can be identified as $380pF$, where the maximum operating frequency is 43 MHz.

For the test in the second phase, the capacitance load will be fixed to $380pF$ since this is the most efficient value of C_z that being acquired by the last test. The test scheme in this phase will be similar to the first one but this time the resistor will be varied. Start with z-port, the transconductance at this port will be analyzed for the different values of R_w. The values of resistor R_w that is going to be used here will be 1Ω, $1k\Omega$ and $1M\Omega$. Same as the first phase, the simulation on transconductance value on z-port can be illustrated in the figure 3.18.

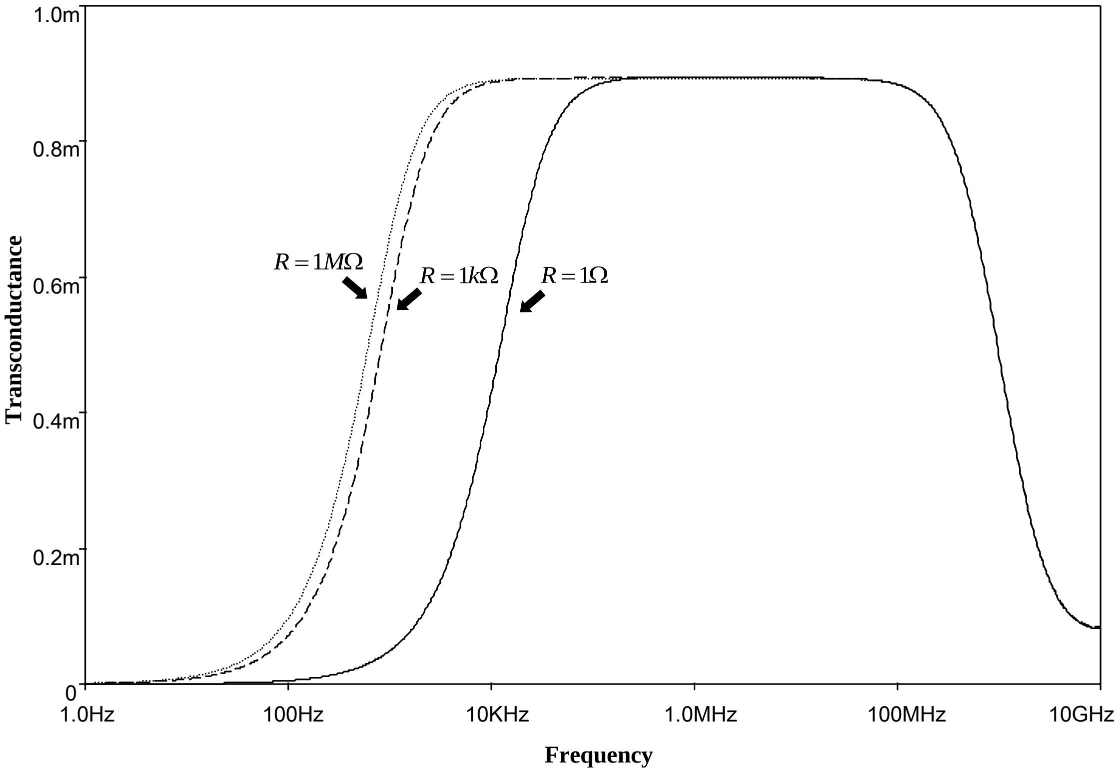


Figure 3.18 The transconductance of CBTA for the difference value of R_w

The high-end corner frequency f_H in the figure 3.18 can be estimated as 670 MHz. As seen from the figure, the corner at high frequency is not really different, which means that the investigation will be on the lower frequency. From the figure 3.18, it can be noticed that increasing in the value of resistive load can extend the corner at low frequency. Since the current trend of the integrated circuit is preferred at high frequency, the lower frequency extension through the increasing of resistive load will be ignored.

For the effect of resistor load R_w on the relationship of w-port and z-port, the analyzed value is voltage gain between w-port and z-port for the different values of R_w. The resistor load value R_w for this case will be 1Ω, $1k\Omega$ and $1M\Omega$. The simulation results of the voltage gain between w-port and z-port (V_w / V_z) can be illustrated in figure 3.19.

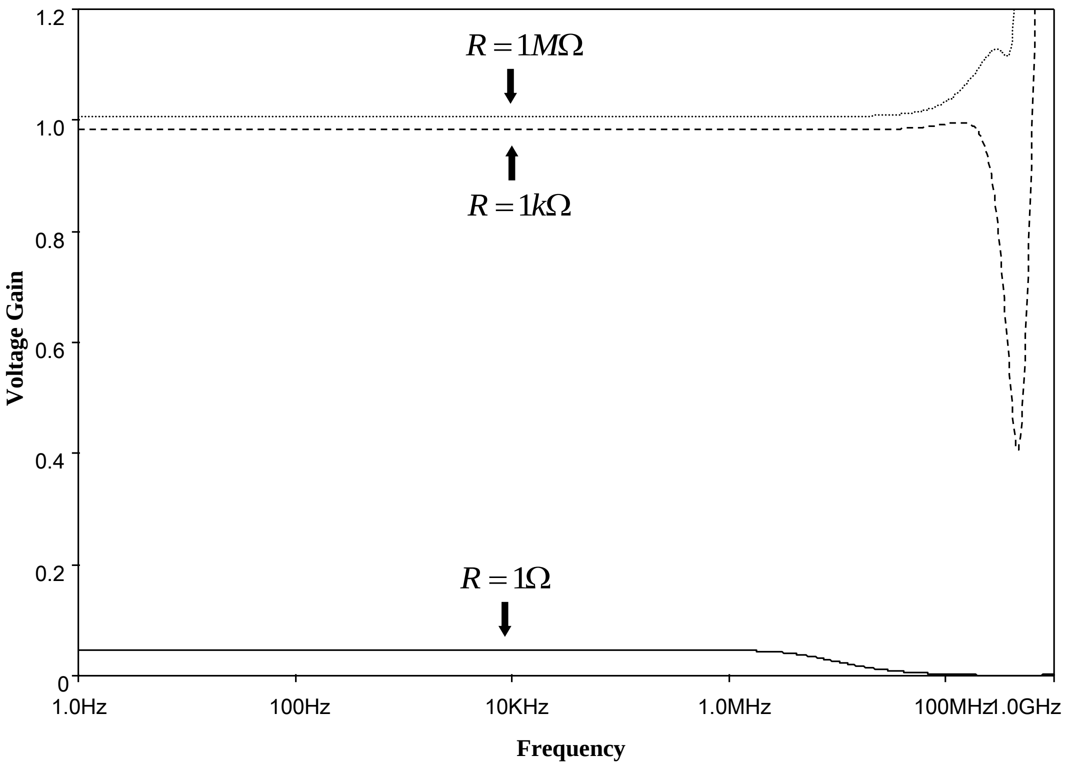


Figure 3.19 The voltage gain of z-port and w-port for the different value of R

It can be seen from the figure above that the voltage gain for $R_w = 1\Omega$ is far from unity. It means that voltage gain for $R_w = 1\Omega$ cannot be used, since the ideal value of this voltage gain should be unity ($V_w = V_z$). The lowest possible value of R_w has to be reacquired because $R_w = 1\Omega$ contains gain error. From the simulation result in figure 3.19, the line for $R_w = 1k\Omega$ does not contain error in the gain (Gain=1). Because of that, the new lowest value of resistance load R_w without gain error can be located between 1Ω and $1k\Omega$. By slowly increasing the resistance load in the simulation program, the new acceptable lowest value of R_w can be found as 400Ω, which the result can be illustrated in the figure 3.20.

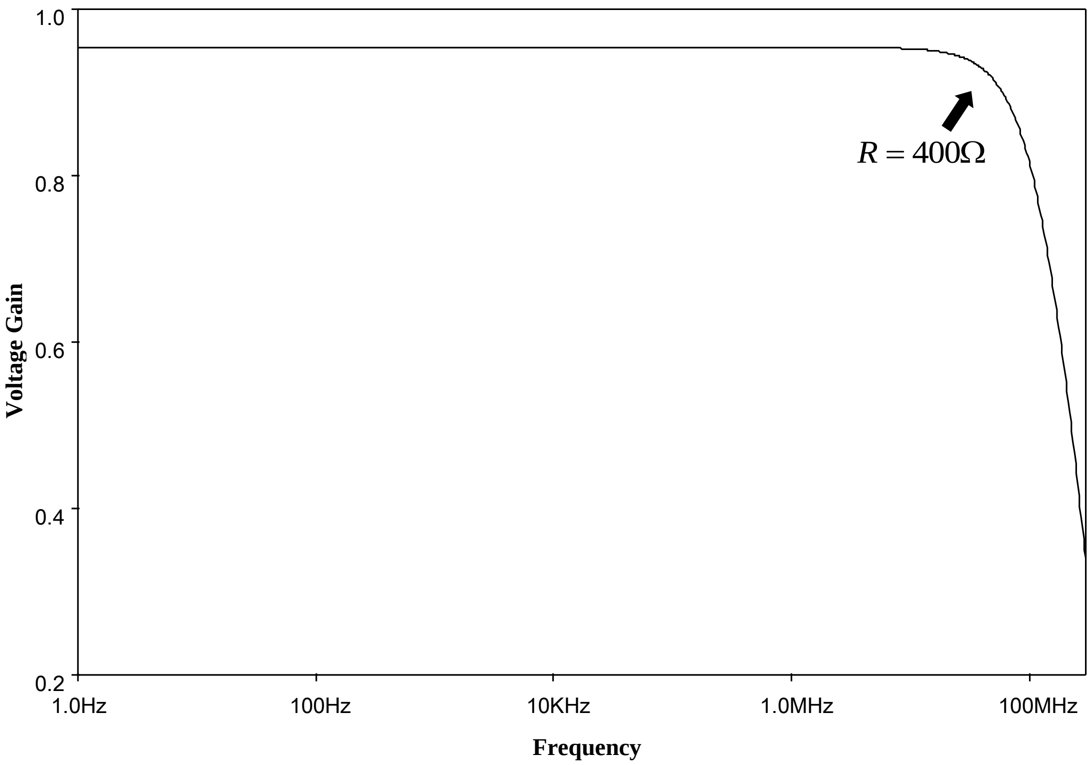


Figure 3.20 The voltage gain of z-port and w-port for the lowest possible value of R_w

It can be seen that the current gain for $R_w = 400\Omega$ now almost ideal (Gain=1). By using the cursor of simulation program, the corner frequency of voltage gain for $R_w = 400\Omega$ can be estimated as 156 MHz.

For the effect of resistor load R_w on the relationship between w-port, p-port and n-port, the current gain between n-port and w-port will be analyzed for the different value of R_w. The resistive load value for this case will be 400Ω, $1k\Omega$ and $1M\Omega$. Note that 400Ω is the new lowest value of R_w that being acquired by last test. The simulation result of the current gain between n-port and w-port (i_n / i_w) can be illustrated in figure 3.21. Since the ideal value of this case must be unity ($|i_n = i_p|$), the line for $R_w = 1M\Omega$ where the gain is around 22 cannot be used. It means that the maximum value of resistive load R_w need to be reacquired. By slowly decreasing the value of R_w through the simulation, the new highest acceptable value of R_w can be found as $3k\Omega$, which the result can be illustrated in figure 3.22. As seen in figure 3.22, the current gains for this range of resistor are now on the accurate value.

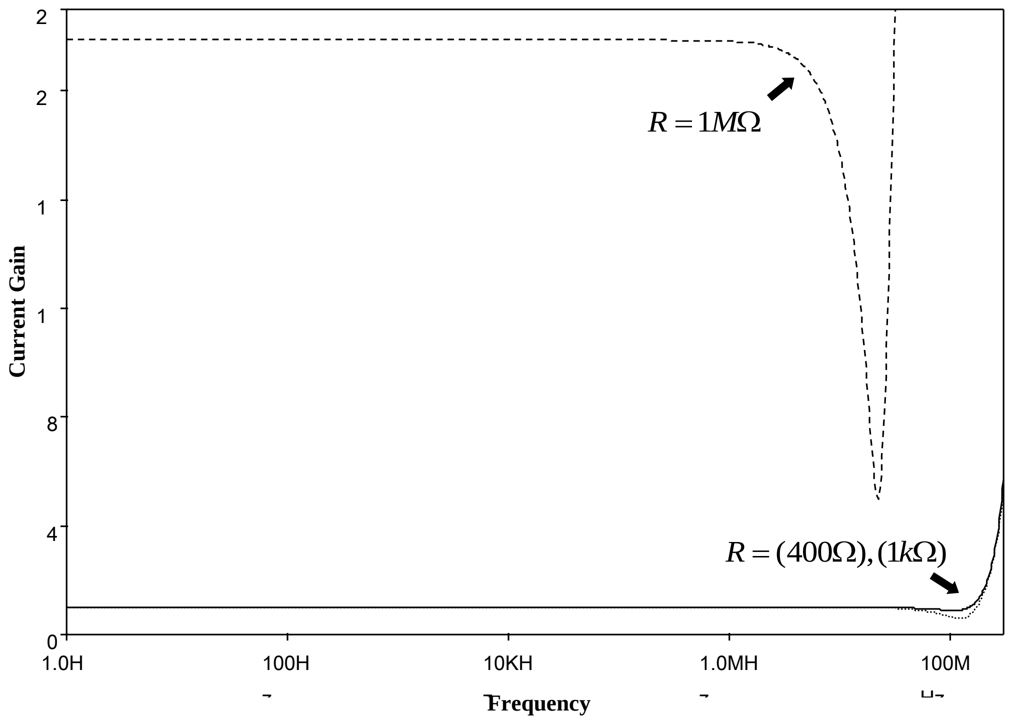


Figure 3.21 The current gain of n-port and w-port for different value of resistive load

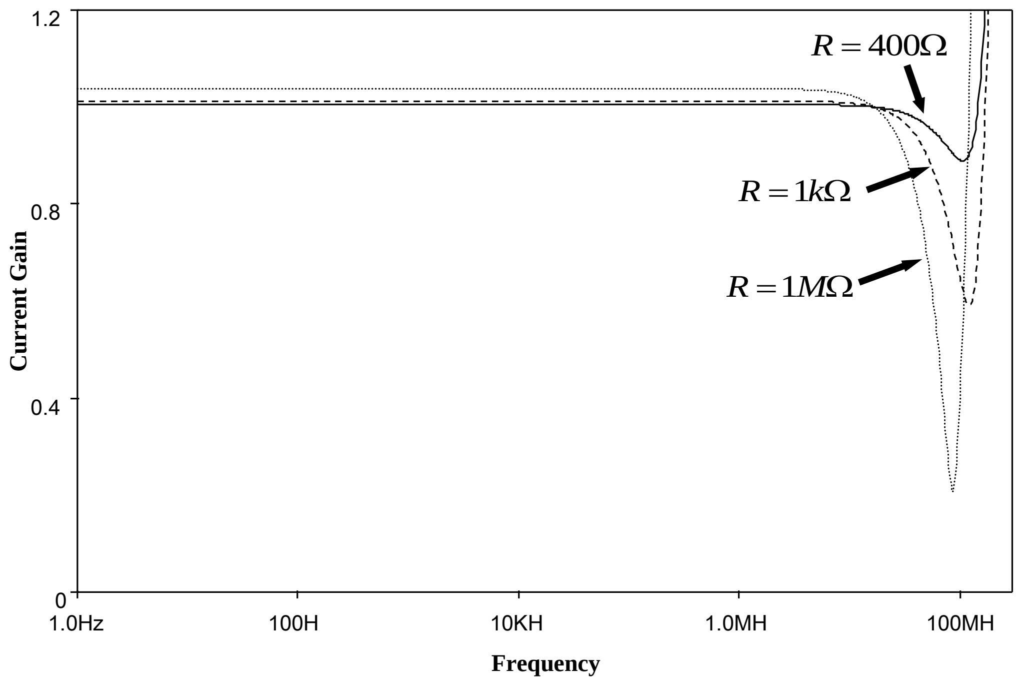


Figure 3.22 The new current gain of n-port and w-port for the different value of R_w

For the corner frequency of CBTA using $R_w = 400\Omega - 3k\Omega$, the investigation will be done separately. For the lowest resistor value $R_w = 400\Omega$ the current that being produced at n-port and w-port can be shown in figure 3.23.

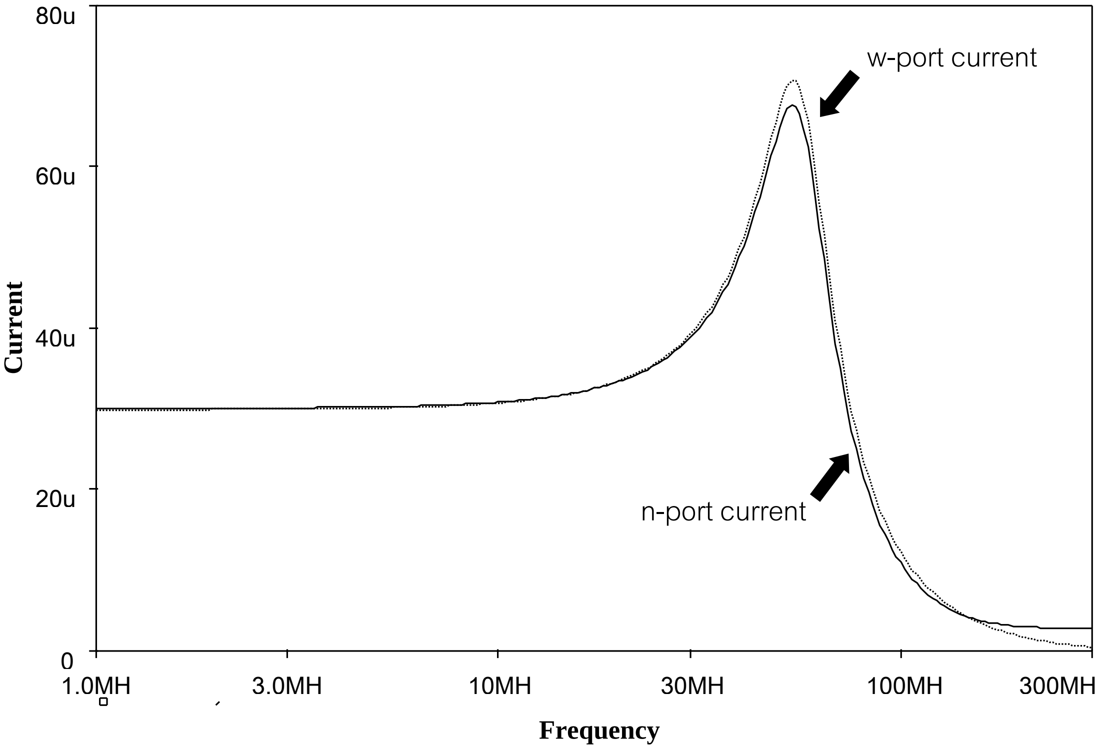


Figure 3.23 n-port and w-port current for $R_w = 400\Omega$

As seen in figure 3.23, an overshoot being occurred for this resistor value. This overshoot is not appeared in figure 3.22 (which represent the gain of I_n / I_w) because the current values of these two ports are closed to each other. In order to eliminate this overshoot, the lowest value of resistor R_w has to be reacquired. By slowly increasing the R_w from 400Ω, the lowest resistor value can be found as $R_w = 900\Omega$ and can be illustrated in figure 3.24. As seen in figure 3.24, the overshoot is eliminated. By using the cursor in simulation program, the corner frequency of the currents relationship between n-port and w-port in figure 3.24 can be estimated as 44 MHz.

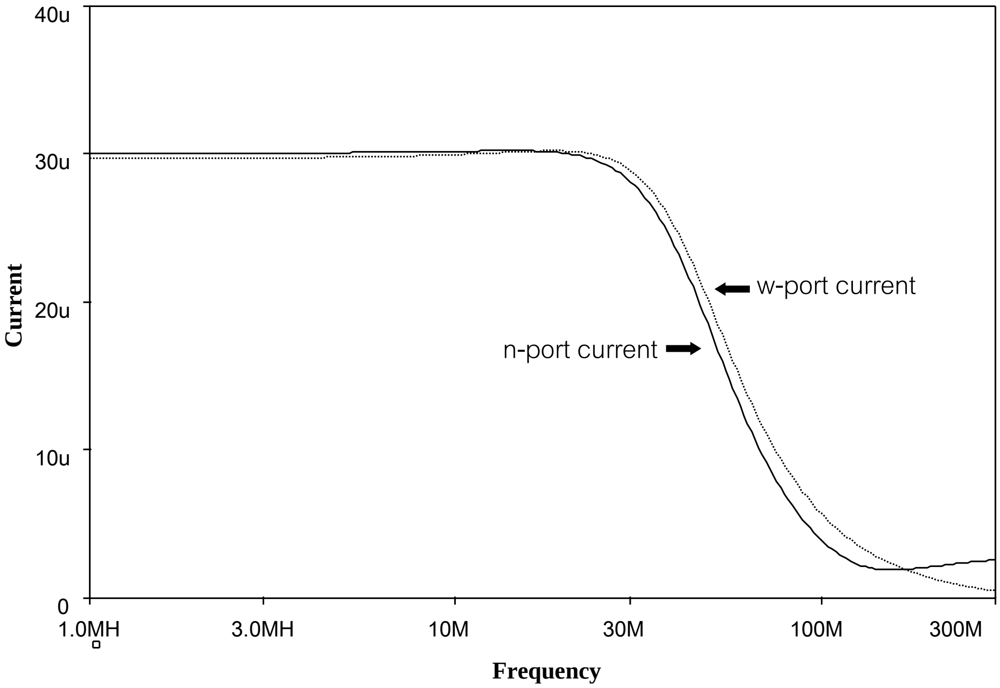


Figure 3.24 n-port and w-port current for $R_w = 900\Omega$

For the highest resistor value $R_w = 3k\Omega$, the current that being produced at n-port and w-port can be shown in figure 3.25.

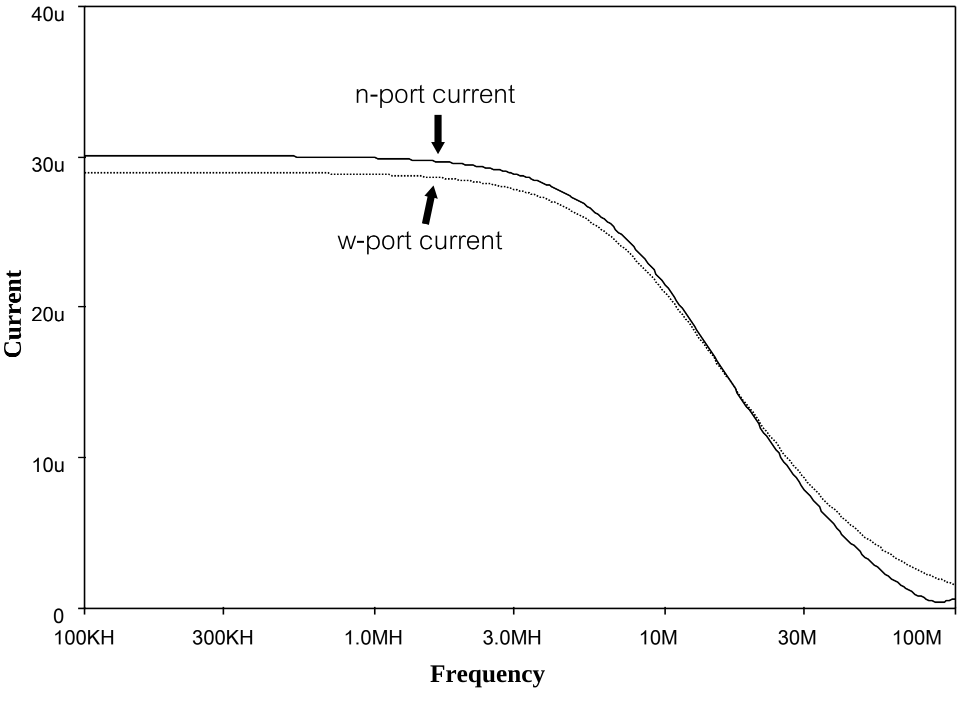


Figure 3.25 n-port and w-port current for $R_w = 3k\Omega$

As seen in figure 3.25, no overshoot being found for this case. The corner frequency of the currents in figure 3.25 can be estimated as 10.4 MHz.

With this testing, the appropriated range of R_w for figure 3.13 will be $R_w = 900\Omega - 3k\Omega$ and the appropriated lowest of C_z will be $C_z = 380pF$. Remember that the maximum operating frequency for $C_z = 380pF$ is 43 MHz for $R_w = 1k\Omega$. From the figure 3.25, $R_w = 900\Omega$ offered the highest operating frequency of 44 MHz. Since the $C_z = 380pF$ already connected to the z-port where $R_w = 900\Omega$ is being test, the maximum operating frequency for $C_z = 380pF$ will also be extended to 44 MHz. With this, it can be assumed that the maximum operating frequency for the most efficient load $R_w = 900\Omega$ and $C_z = 380pF$ is 44 MHz.

3.6 Summary

This chapter explains the realization of CBTA starting from the root of the circuit which is the OTA and the CCII. The derivation of CBTA is done step by step using the information provided by last chapter. To describe the overall image of the CBTA, its structure, schematic symbol, equivalent circuit and characteristic matrix equation are analyzed. The simulation in this chapter is provided in order to verify the characteristic of CBTA and its frequency response when the parasitic components taking effect.

CHAPTER IV
INDUCTANCE SIMULATOR USING CBTA

4.1 Introduction

Several circuits were developed by CBTA [14-17]. In this chapter, the realization concept of inductance simulator using CBTA will be introduced. The detail are about the derivation of the proposed circuit. In addition, the simulation results of the proposed circuit will be presented. The results are as follow; frequency response, tunability and linearity. Moreover, these results are compared to the ideal inductor and the other inductance simulator that being recently introduced. For the application of the proposed circuit, the second order band-pass filter is being chosen as an example. For the investigation method, filter circuit will be analyzed in three cases. The first case is where the proposed circuit replaced an inductor in the filter circuit. The second case is the original filter circuit using the ideal inductor. The final case is the recently introduced inductance simulator using ZC-CFTA. Comparing the quality factor and power consumption from these three cases, the performance of the filter using the proposed circuit can be acquired.

4.2 Realization of Inductance Simulator using CBTA

To begin the realization of inductance simulator, the basic information of ideal inductor need to be acquired. The symbol of an ideal inductor can be illustrated in figure 4.1. The impedance value of the figure 4.1 can be acquired by dividing the voltage across the ideal inductor with the current that going through it. The impedance of ideal inductor can be expressed in this equation.

$$Z_L = sL_{eq} = \frac{V_1 - V_2}{I_{in}} \tag{4.1}$$

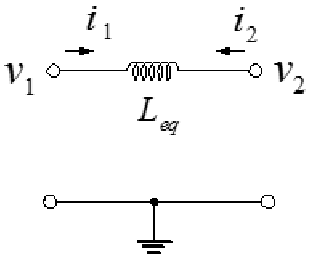


Figure 4.1 Electronic symbol of a passive inductor

For the concept of inductance simulator realization, the input impedance of a designed circuit must be in the same format as equation 4.1. For the better understanding, this realization concept can be illustrated in figure 4.2.

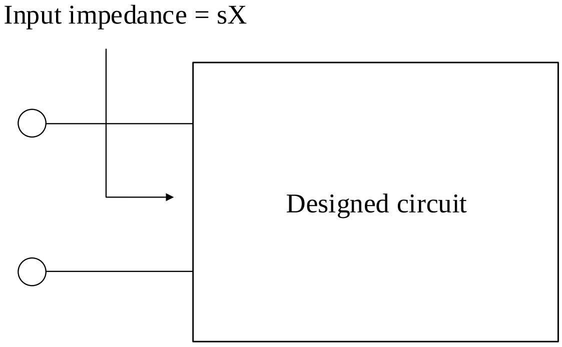


Figure 4.2 Realization concept of inductance simulator

Now, the CBTA test circuit in the last chapter will be illustrated again in figure 4.3. In fact, this circuit is already an inductance simulator. As for the reason, the derivation of this circuit will be explained here. In this case, the derivation will be focused on the input impedance. For this derivation, the CBTA configuration will use figure 3.5 which the transistors dimension are given in table 3.1.

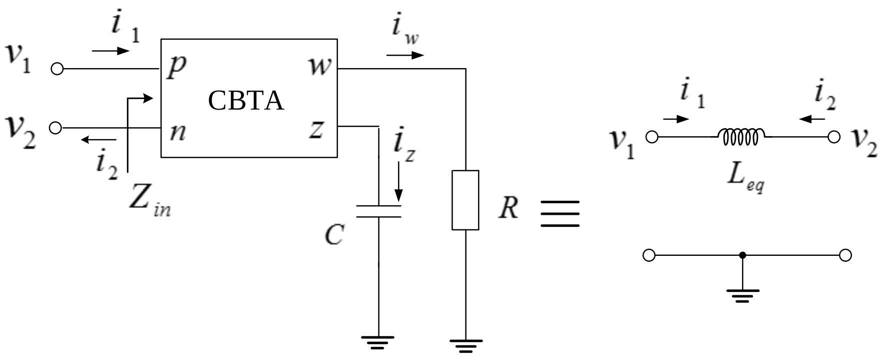


Figure 4.3 Inductance simulator using CBTA

Normally, the output current at z-port should follow the first characteristic of CBTA ($i_z = g_m(v_p - v_n)$). However, the transistors dimension for some of the current mirror are not identical. The output current at z-port has to be recalculated. In figure 3.5, the transistors M_{28} and M_{30} have 4 times higher dimension comparing to transistors M_{27} and M_{29}. The transistors M_{33} and M_{34} have 4.4 time higher dimension comparing to transistors M_{31} and M_{32}. Because the dimension of the transistors in current mirror pair are not identical, the current at z-port can be rewritten as this equation.

$$i_z = 4.2 g_m (v_p - v_n) \tag{4.2}$$

Because of that, the voltage at z-port in figure 4.3 can be expressed in this equation.

$$v_z = \frac{4.2 g_m (v_p - v_n)}{sC} \tag{4.3}$$

The voltage that being generated at z-port will influence the voltage at w-port according to the characteristic of CBTA ($v_w = v_z$). Because of that, the current that being generated at w-port can be expressed in this equation.

$$i_w = \frac{4.2 g_m (v_p - v_n)}{sCR} \tag{4.4}$$

The current that being generated at w-port will be carried out to p-port and n-port according to the characteristic of CBTA ($i_w = i_p = -i_n$). Assumed that the p-port and n-port are the input port of the inductance simulator, the current i_w can be treated as the input current I_{in}. Consideration the equation 4.4, the voltage $(v_p - v_n)$ can be treated as voltage across the component in figure 4.3 (V_{in}). Combining all the derivation, the input impedance of figure 4.3 can be expressed in this equation.

$$\frac{V_{in}}{I_{in}} = \frac{sCR}{4.2 g_m} = sL \tag{4.5}$$

From equation 4.5, it can be seen that figure 4.3 now becomes an inductance simulator. In order to test the inductance simulator in figure 4.3, the results from simulation program will be provided. With $\pm 1.5V$ voltage supplies and $50\mu A$ bias current, the transconductance g_m can be calculated as $0.285mS$ by hand. Since the hand calculation value contains error, the more accurate value of g_m can be alternatively acquired by simulation, which in this case is $0.242mS$. From the previous chapter, the most efficient loads for figure 4.3 can be found as follows; $C = 380pF$ and $R = 900\Omega$. The maximum operating frequency in this case should be $44MHz$. Substituting these values in equation 4.5, the inductance value of figure 4.3 can be found as $0.336mH$. By applying the test current source to the circuit in figure 4.3, the input impedance of the proposed circuit can be acquired. The frequency response of input impedance in figure 4.3 comparing to ideal inductor at $0.336mH$ can be illustrated in the figure 4.4.

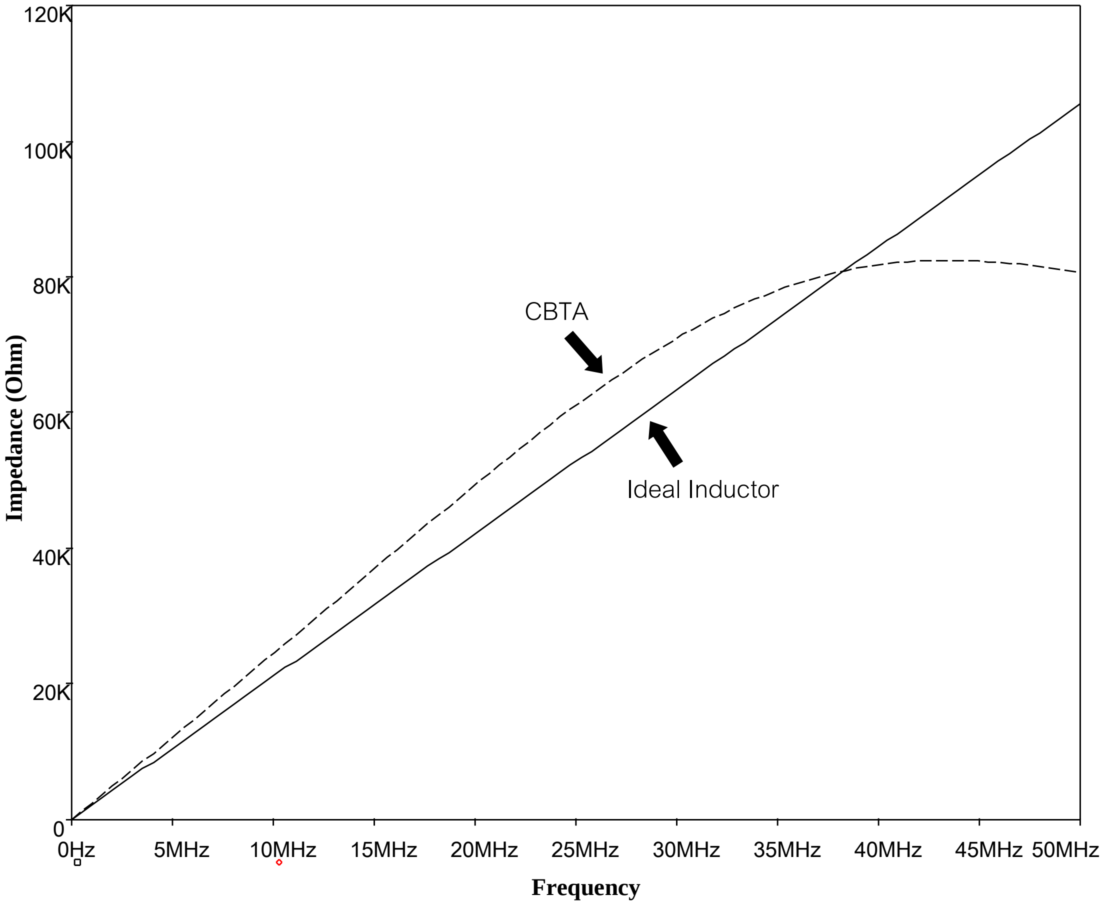


Figure 4.4 The impedance of proposed circuit and the ideal inductor at $0.336mH$

As seen in figure 4.4, the frequency response of input impedance of the proposed circuit is a little higher than an ideal inductor. The source of this error is from the non-ideality of each port of CBTA that being explained in the last chapter. By adding the non-ideal parameter of each port, equation 4.5 can be expressed as equation 4.6.

$$\frac{V_{in}}{I_{in}} = \frac{sCR}{4.2g_m(s)\times(\mu_w)\times(\alpha_{p,n})} = sL \qquad (4.6)$$

Using the value of non-ideal parameter that being found from the previous chapter, the inductance value of the proposed circuit can be recalculated as $0.392mH$. The frequency response of introduce circuit comparing to the ideal inductor at $0.392mH$ can be illustrated in figure 4.5.

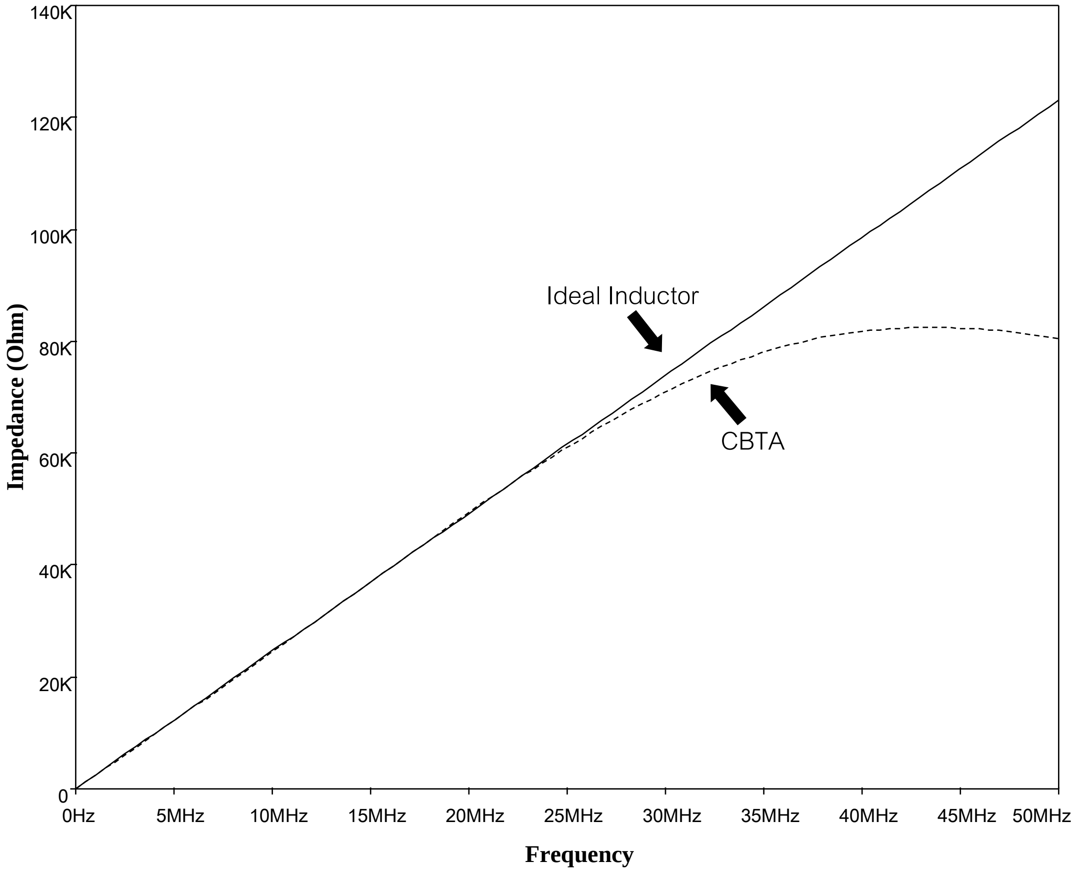


Figure 4.5 The impedance of proposed circuit and the ideal inductor at $0.392mH$

On the frequency of $25MHz$, the impedance of the proposed circuit starting to drift apart from the ideal inductor. Moreover, the impedance of the proposed circuit stop increasing at $44MHz$. The source of these errors arise from the effect of loads of CBTA that being explained in the previous chapter.

As seen in equation 4.1, the impedance of ideal inductor is linear equation. The derivative of equation 4.1 should be in a constant value for all frequency ranges. For the linearity of the proposed circuit, it sketch as the dash line in figure 4.5. It can be seen that the inductance value is increased consistently until the frequency of $25MHz$. Because of that, the derivative of the inductance value for this frequency range should be in a constant value. By normalizing this value, the percentage of linearity for the proposed circuit can be acquired. The normalized value of derivative of impedance versus frequency can be illustrated in figure 4.6. As seen in the figure 4.6, the frequency that the derivative value decreased to 0.99 is about $20MHz$. Because of that, the frequency $0MHz$ to $20MHz$ is the frequency range that the proposed circuit can be linearly performed with 1% variation error.

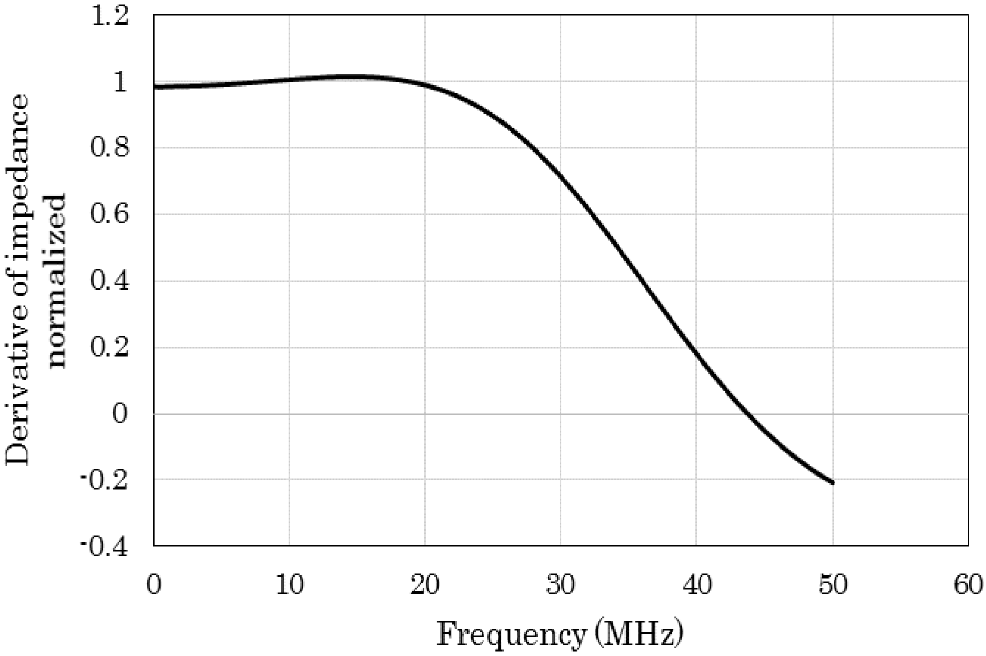


Figure 4.6 The derivative of impedance of the proposed circuit.

The next investigation will be about the tunability of the proposed circuit. From the equation of inductance value of the proposed circuit (which is equation 4.5), it can be seen that the equation contains the transconductance parameter g_m. According to equation 2.4 ($g_m = 2\sqrt{KI_D}$), this value is depended on the biasing current of CBTA (I_D). Because of that, the inductance value of the proposed circuit (equation 4.5) can be controlled by the value of g_m. As for the simulation result, the plot of the impedance value versus the biasing current of the proposed circuit can be illustrated in figure 4.7. From the figure 4.7, it can be seen that the increasing in the biasing current decrease the impedance value of the proposed circuit.

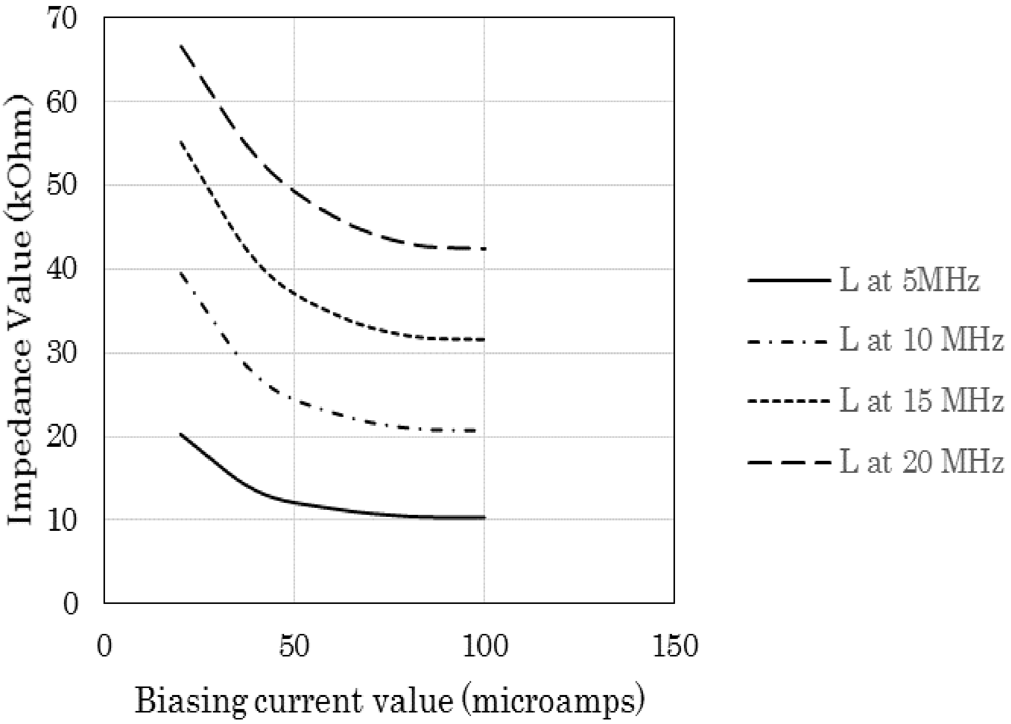


Figure 4.7 The tune ability of the proposed circuit at varios frequencies

For the quality factor of the proposed circuit, it can be found by using this equation.

$$Q = \frac{\omega L}{R} \tag{4.6}$$

In order to find the resistance of the proposed circuit, a dependent DC current source will be used instead of AC current source. With this, the imaginary part of the proposed circuit will not interfere with its impedance value. The impedance value of the proposed circuit with DC source can be illustrated in figure 4.8. From the figure 4.8, the resistance of the proposed circuit can be approximately calculated as 217Ω. Substituting the resistance value $R = 217\Omega$ and the inductance value $L = 0.392mH$ in the equation 4.6, the quality factor of proposed circuit can be acquired. Since the equation 4.6 contains the parameter ω, the quality factor will not be a constant value for every frequency. For example, the quality factor of the proposed circuit at $20MHz$ will be 227.

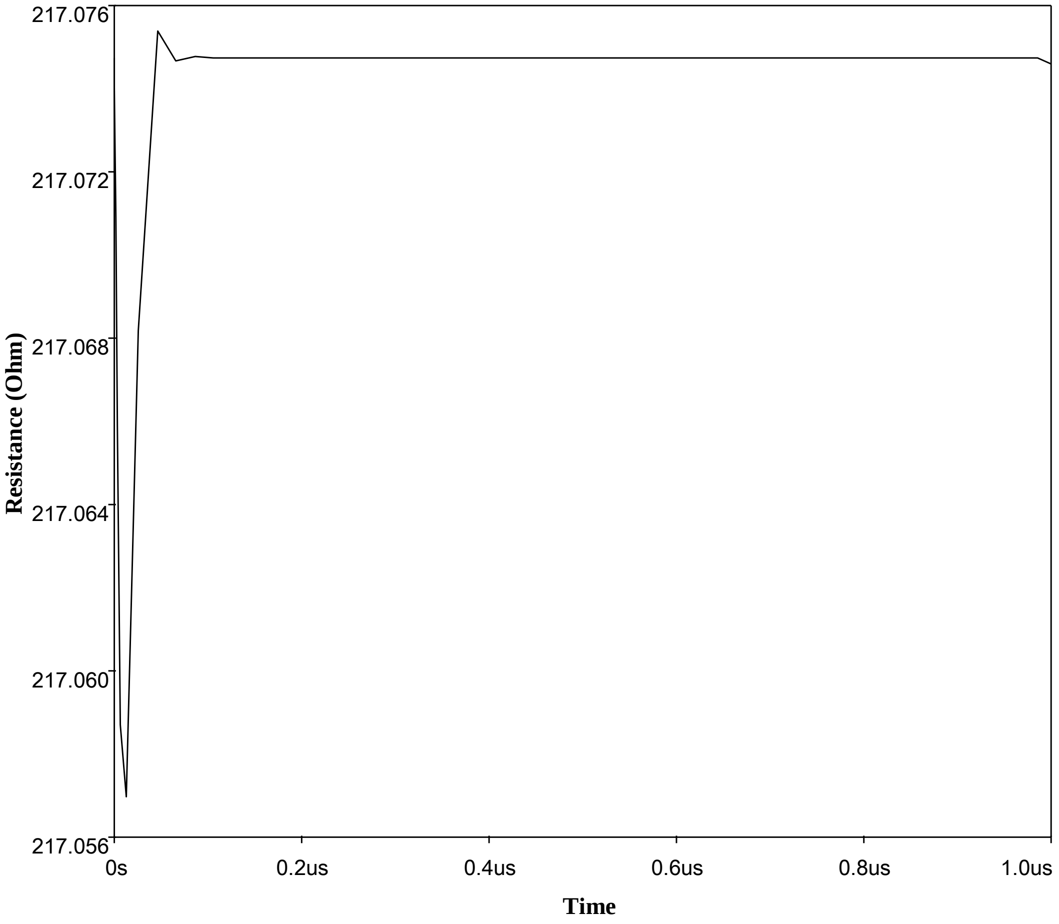


Figure 4.8 The resistance of the proposed circuit

For the power consumption of proposed circuit, it can be measured by the simulation program. For the biasing voltage of $\pm 1.5V$, the power consumption of the proposed circuit is $6.29mW$.

4.3 Application of Inductance Simulator using CBTA

In this section, the investigation will be on the applications of inductance simulator based on CBTA with common electronic circuits such as filter and oscillator. In this investigation, a second order band pass filter (BP) is being chosen as an application circuit. It is a passive circuit that contains passive component such as capacitors, inductors, and resistors. Filter circuits have a role to eliminate unwanted frequencies from output signal of circuits that the filters are being attached to. The simulation result for this section will be the voltage gain of the filter circuit. In order to investigate the performance of the proposed circuit, the result of the filter using the proposed circuit will be compared with an ideal inductor and the other introduced inductance simulator. The second order band pass filter circuit that is going to be used in this investigation can be illustrated in figure 4.9.

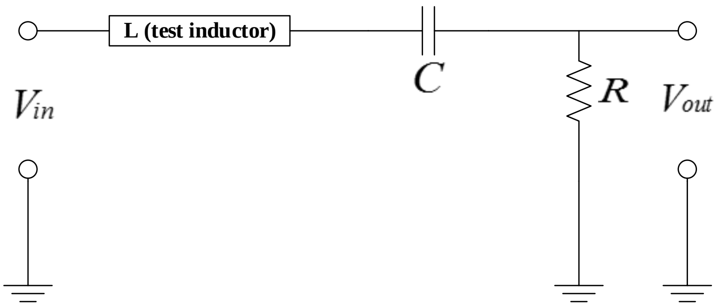


Figure 4.9 Second order band-pass notch filter [18]

In the figure 4.9, the test inductor will be replaced with the various kind of inductors. For an ideal inductor, the transfer function of this band pass filter can be expressed as this equation.

$$\frac{V_{out}}{V_{in}} = \frac{s(R/L)}{s^2 + s(R/L) + (1/LC)} \tag{4.7}$$

For the other introduced circuit that going be used in comparison, the inductance simulator using z-copy current follower transconductance amplifiers (ZC-CFTA) is being chosen [18]. This circuit can be illustrated in figure 4.10.

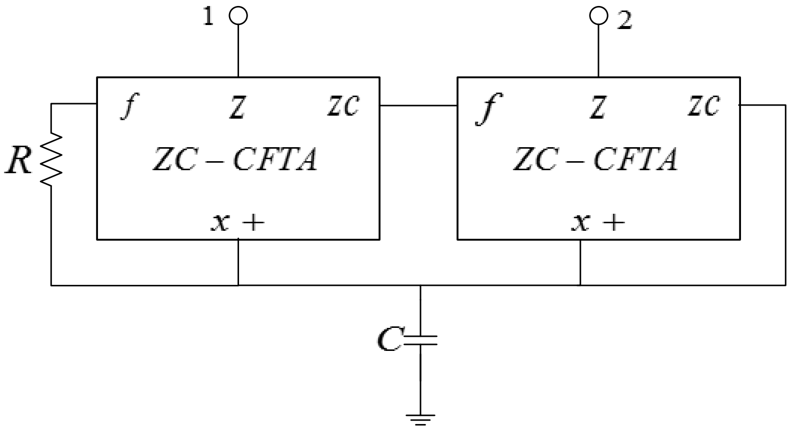


Figure 4.10 Inductance simulator based on ZC-CFTA [18]

This inductance simulator also used the same technology as the proposed circuit (TSMC $0.25\mu m$) and the operating frequency is closed to the proposed circuit. Because of that, it is a good inductance simulator to be used in comparison with the proposed circuit. Since the circuit configuration in [18] specified for the inductance value to be $1mH$, the investigation on this section also have to do on the same inductance value. Now, set the values of capacitors and resistors of figure 4.9 to $1nF$ and $1k\Omega$ respectively. Also setting the inductance values of the proposed circuit, the inductance simulator using ZC-CFTA and the ideal inductor to $1mH$. Applying a independent voltage source at the input port of the filter then analyze the value of voltage at the output port. A Bode plot of the band pass filter can be illustrate in figure 4.11.

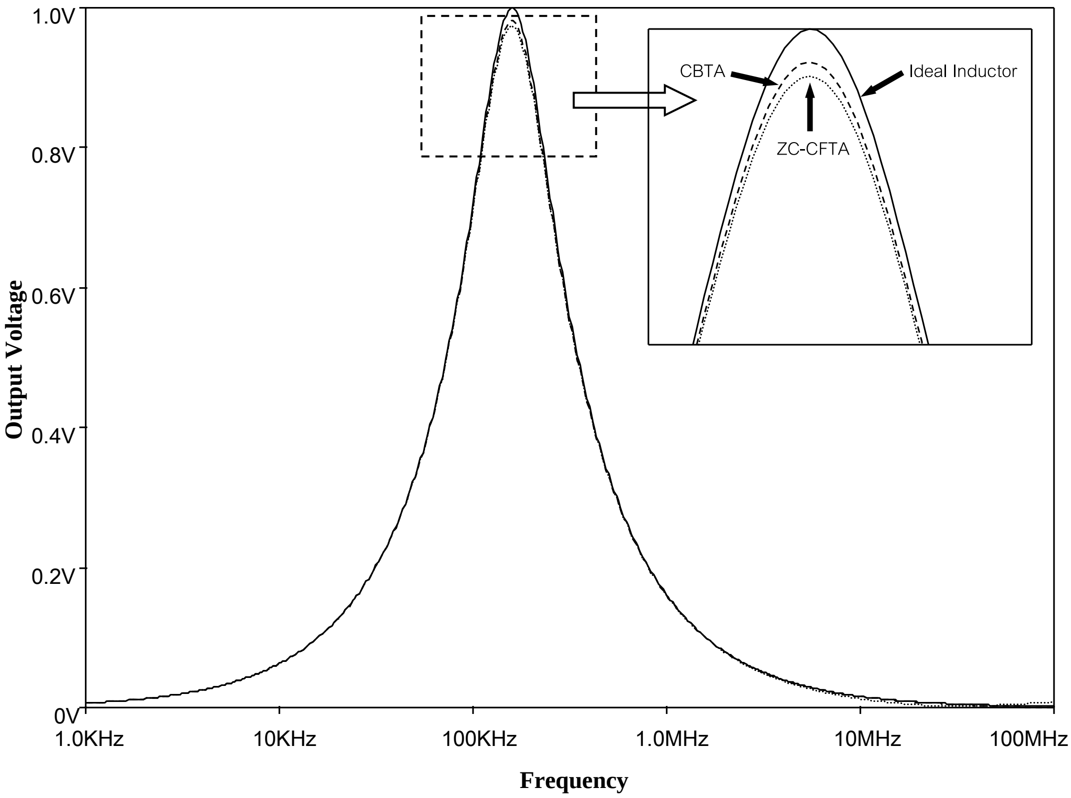


Figure 4.11 Magnitude Plot of BP filter with three different inductors.

From the result, the filter quality factor for ideal inductor, proposed circuit and ZC-CFTA can be found as 0.996, 0.99 and 0.967 respectively. The quality factor of proposed circuit and the referenced circuit may not be really different, but the power consumption does. Because the inductance simulator using ZC-CFTA need about twice transistors amount compared the proposed circuit, it consumed more power. By using the power dissipation function in the simulation program, the power consumption of the proposed circuit and the referenced circuit can be found as $6.29mW$ and $11.6mW$ respectively. As seen from the result, the referenced circuit consumes almost twice amount of power comparing to the proposed circuit. Finally, the summarize of the characteristic of the proposed circuit can be shown in table 4.1

Technology	Maximum frequency	Quality factor at $20MHz$	Linearity range for 1% variation error	Power
TSMC $0.25\mu m$	$25MHz$	227	$(0-20)MHz$	$6.29mW$

Table 4.1 The characteristic of inductance simulator using CBTA

4.4 Summary

This chapter explained the realization of inductance simulator using CBTA. The circuit derivation starting from a single CBTA to a completed circuit is also provided. To verify the precision of the proposed circuit, the simulation process is provided. For the investigation on the accuracy of inductance value, the proposed circuit is compared with the ideal passive inductor. As for the linearity of the proposed circuit, the simulation on the derivative of impedance and the frequency is provided. The tunability of the proposed circuit is shown by the plot of the impedance value and the increasing of the biasing current. For the application of the proposed circuit, the simulation on the BP filter is provided. The investigation focusing on the BP filter using three different inductor which are the proposed circuit, an ideal inductor and the other introduced inductor. The magnitude plot of filter and the power consumption are given as results.

CHAPTER V

CONCLUSION

An inductance simulator using current backward transconductance amplifier (CBTA) is proposed and simulated. It consists of a single CBTA, a capacitor and a resistor. The CBTA structure is being realized by the transistor model MOSIS TSMC level 7 $0.25\mu m$. The proposed circuit capable of simulating inductor at the bandwidth of $0Hz$ to $20MHz$ for an inductance value of $0.392mH$. The proposed circuit is also proved to contain less than 1% linearity error for $0Hz$ to $20MHz$ frequency range. The proposed circuit power dissipation is $6.29mW$. By adjusting the biasing current of the proposed circuit, the inductance value can be tuned. The quality factor of the proposed circuit is 227 for the maximum operating frequency of $20MHz$. The applications of the proposed circuit are focusing on the designation of integrated circuits that working on the radio frequency such as filter, oscillator and phase shifter. The proposed circuit will replace the lump inductor that normally not appropriated to be used on the integrated circuit. As an example, the simulation on the BP filter is provided. The BP filter using the proposed circuit is proved to consume less power than the ZC-CFTA inductor.

REFERENCES

1 D.S. Jayalalitha, D.Susan, “Grounded Simulated Inductor - A review” Middle-east journal of scientific research 15, 2013, pp.278-286.

2 Sedra, K.C. Smith, “A second generation current-conveyor and its applications”, IEEE Transaction on Circuit Theory, 1970, pp.132-133.

3 A.N. Pual, D. Patranabis, “Active simulation of grounded inductors using a single current conveyor”, IEEE Transaction on Circuits and Systems, vol. cas-28, no. 2, 1981, pp. 164-165.

4 K. Pal, “Novel floating inductance using current conveyors”, Electronic Letters, vol.17, no. 18, 1981, pp. 638.

5 W. Kiranon, P. Pawarangkoon, “Floating inductance simulation based on current conveyors”, Electronic Letters, vol. 33, no. 21,1997, pp. 1748-1749.

6 S. Konglamphan, A. Chantakun, M. Sripruchyanun, “Floating positive and negative inductance simulators based on CC-DVCCs” International conference on science, Technology and innovation for sustainable well-being, 2009, pp. 294-300.

7 Jantakun, M. Sripruchyanun, “Single Element Based Electronically tunable Floating positive and negative inductance simulators and its applications” JICTEE, 2010, pp. 321-325.

8 R.S. Winton, “Essentials of Circuits, Devices, Networks and Microelectronics” Amazon publications, pp.255-264, 307-325.

9 A.S. Sedra, K.C. Smith, “Microelectronic circuit 6th edition” Oxford 2010, pp.302-305, 588-612, 637-641.

10 T.C. Carusone, D.A. Johns, K.W. Martin, “Analog Integrated Circuit Design 2nd edition” John Wiley & Sons 2012, pp.193-197.

11 U.E. Ayten, M. Sagbas, N. Herencsar, J. Koton, “Novel Floating General Element Simulator Using CBTA” Radioengineering vol. 21, 2012, pp.11-19.

12 K.C. Smith, A. Sedra, "The Current Conveyor A New Circuit Building Block" Proceeding of the IEEE, 1968, pp.1368-1369.

13 E. Yuce, O. Cicekoglu, S. Minaei, "CCII-Based Grounded to Floating Immittance Converter and a Floating Inductance Simulator", Analog Integrated Circuits and Signal Processing, 2006, pp.287-291.

14 U.E. Ayten, M. Sagbas, H. Sedef, "Current mode leapfrog ladder filters using a new active block", International Journal of Electronics and Communication, 2010, pp.503-511.

15 U.E. Ayten, M. Sagbas, H. Sedef, "Current and voltage transfer function filters using a single active device", IET Circuits Device and System Volume 4, 2010, pp.78-86.

16 N. Herencsar, J. Koton, K. Vrba, A. Lahiri, U. E. Ayten, M. Sagbas, "A New Compact CMOS Realization of Sinusoidal Oscillator Using a Single Modified CBTA" Radioelektronika 21st International Conference, 2011, pp.1-4.

17 M. Koksal, "Realization of general all-pole current transfer function by using CBTA", International Journal of Circuit Theory and Application, 2011, pp.319-329

18 N. Herenscar, A. Lahiri, J. Koton, K. VRBA, R. Sotner, "New Floating Lossless Inductance Simulator Using Z-copy Current follower Transconductance amplifiers", 22nd International Conference Radioelektronika, 2012, pp.1-4.

19 S. Lertwicha, D. Wilairat, A New Tunable Floating Inductance Using Current Backward Transconductance Amplifier, Tokyo International Conference on Engineering and Applied Science, 2014, pp.819-827.

APPENDICES

APPENDIX A

PARAMETERS OF TSMC 0.25 NMOS TRANSISTOR MODEL

```
.MODEL CMOSN NMOS (                                LEVEL   = 5
+VERSION = 3.1            TNOM    = 27             TOX     = 5.7E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.4057065
+K1      = 0.4812565      K2      = -2.143234E-6   K3      = 1E-3
+K3B     = 1.739064       W0      = 1E-7           NLX     = 2.07014E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.853855       DVT1    = 0.5269796      DVT2    = -0.1516398
+U0      = 336.1142488    UA      = -9.13972E-10   UB      = 2.29739E-18
+UC      = 4.595948E-11   VSAT    = 1.231309E5     A0      = 1.8852603
+AGS     = 0.3741845      B0      = -5.05764E-10   B1      = 1.304868E-8
+KETA    = -0.010292      A1      = 4.842526E-4    A2      = 0.5918155
+RDSW    = 200            PRWG    = 0.5            PRWB    = -0.1215943
+WR      = 1              WINT    = 0              LINT    = 0
+XL      = 0              XW      = -4E-8          DWG     = -8.398692E-9
+DWB     = 6.989789E-9    VOFF    = -0.110589      NFACTOR = 1.5456108
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 6.186036E-3    ETAB    = 4.072635E-4
+DSUB    = 0.0454263      PCLM    = 1.6180211      PDIBLC1 = 0.960617
+PDIBLC2 = 2.756532E-3    PDIBLCB = 0.0632399      DROUT   = 1
+PSCBE1  = 6.835886E8     PSCBE2  = 2.321947E-4    PVAG    = 9.588376E-3
+DELTA   = 0.01           RSH     = 4.8            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 3.97E-10       CGSO    = 3.97E-10       CGBO    = 1E-12
+CJ      = 1.693231E-3    PB      = 0.99           MJ      = 0.4659089
+CJSW    = 4.010534E-10   PBSW    = 0.8            MJSW    = 0.3105251
+CJSWG   = 3.29E-10       PBSWG   = 0.8            MJSWG   = 0.3105251
+CF      = 0              PVTH0   = -4.987453E-3   PRDSW   = -10
+PK2     = 2.35067E-3     WKETA   = 5.026193E-3    LKETA   = 3.095218E-
3     )
```

APPENDIX B

PARAMETERS OF TSMC 0.25 PMOS TRANSISTOR MODEL

```
.MODEL CMOSP PMOS (                                LEVEL   = 5
+VERSION = 3.1            TNOM    = 27             TOX     = 5.7E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.5914264
+K1      = 0.6633444      K2      = -2.559301E-3   K3      = 0.096591
+K3B     = 5.9878122      W0      = 1E-6           NLX     = 1.230011E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 4.5107722      DVT1    = 0.8938246      DVT2    = -0.0791488
+U0      = 105.4362828    UA      = 1.14213E-9     UB      = 1E-21
+UC      = -1E-10         VSAT    = 1.633945E5     A0      = 1.1356848
+AGS     = 0.1867493      B0      = 6.319402E-7    B1      = 5E-6
+KETA    = 0.0159733      A1      = 0.0407986      A2      = 0.3
+RDSW    = 1.45126E3      PRWG    = 0.0371558      PRWB    = -0.1304058
+WR      = 1              WINT    = 0              LINT    = 3.235579E-8
+XL      = 0              XW      = -4E-8          DWG     = -3.103962E-8
+DWB     = -8.779821E-9   VOFF    = -0.1299825     NFACTOR = 0.9968441
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.2991485      ETAB    = -0.0484912
+DSUB    = 1.00379        PCLM    = 1.2655502      PDIBLC1 = 3.48145E-3
+PDIBLC2 = -4.550334E-6   PDIBLCB = -1E-3          DROUT   = 0.0495568
+PSCBE1  = 7.295808E9     PSCBE2  = 1.690202E-9    PVAG    = 0
+DELTA   = 0.01           RSH     = 3.3            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 5.11E-10       CGSO    = 5.11E-10       CGBO    = 1E-12
+CJ      = 1.893734E-3    PB      = 0.9889579      MJ      = 0.4705132
+CJSW    = 3.124347E-10   PBSW    = 0.8            MJSW    = 0.2786992
+CJSWG   = 2.5E-10        PBSWG   = 0.8            MJSWG   = 0.2786992
+CF      = 0              PVTH0   = 3.006772E-3    PRDSW   = 11.8252609
+PK2     = 1.675914E-3    WKETA   = 0.0130859      LKETA   = -5.842819E-
3    )
```

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