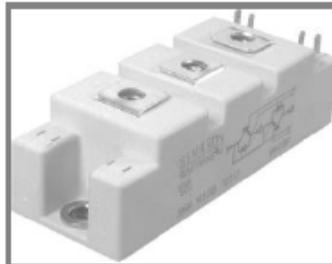




## SKM 75GB063D



SEMITRANS® 2

### Superfast NPT-IGBT Modules

SKM 75GB063D

SKM 75GAR063D

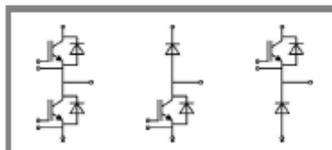
SKM 75GAL063D

#### Features

- N channel, homogeneous Si-structure (NPT-Non punch-through IGBT)
- Low tail current with low temperature dependence
- High short circuit capability, self limiting if term. G is clamped to E
- Pos. temp.-coeff. of  $V_{CEsat}$
- Very low  $C_{ies}$ ,  $C_{oes}$ ,  $C_{res}$
- Latch-up free
- Fast & soft inverse CAL diodes
- Isolated copper baseplate using DBC Direct Copper Bonding Technology without hard mould
- Large clearance (10 mm) and creepage distances (20 mm)

#### Typical Applications\*

- Switching (not for linear use)
- Switched mode power supplies
- UPS
- Three phase inverters for servo / AC motor speed control
- Pulse frequencies also > 10kHz



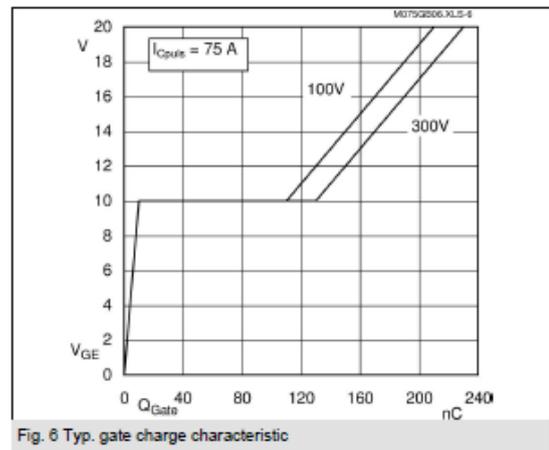
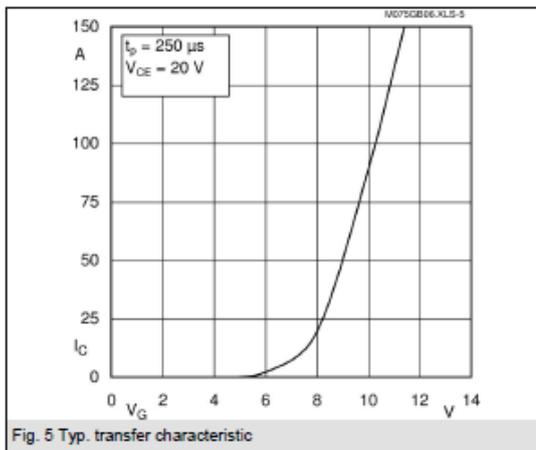
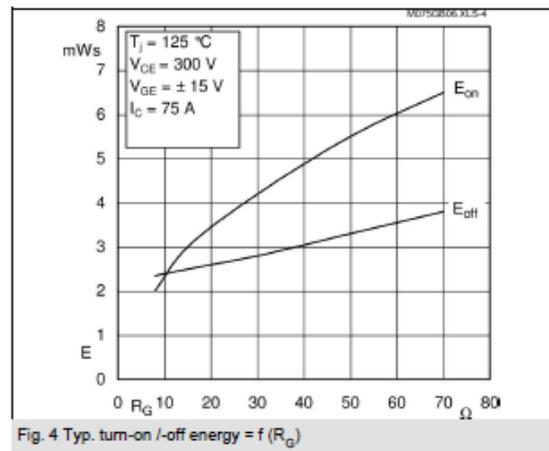
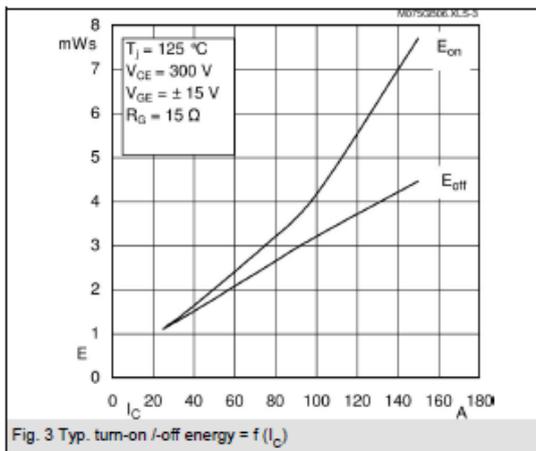
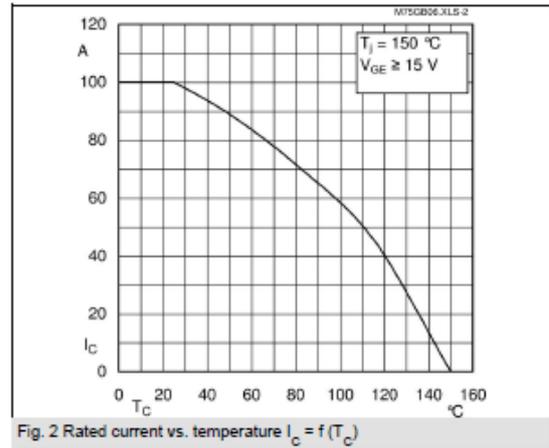
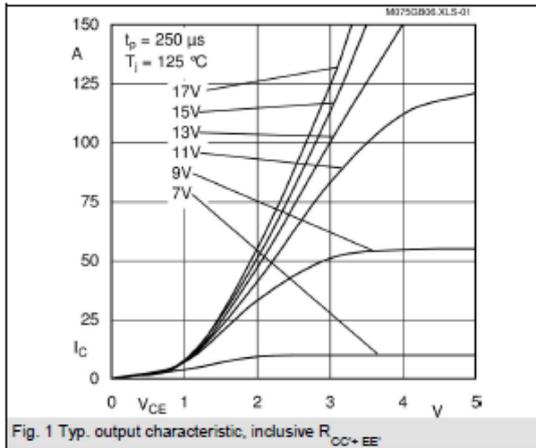
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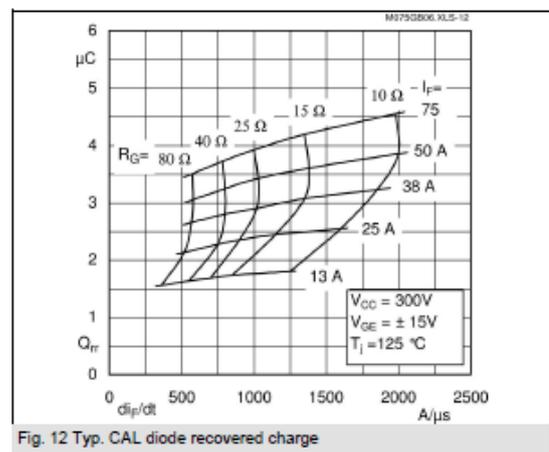
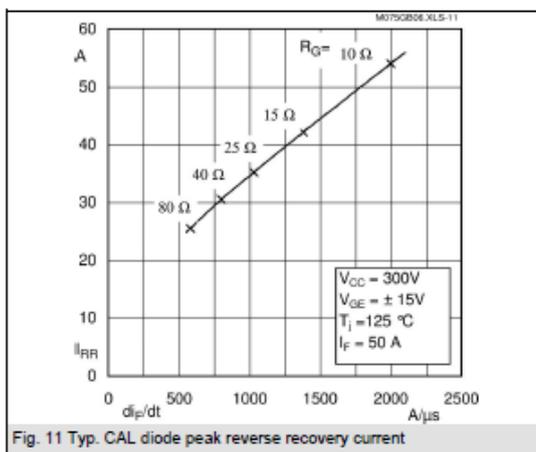
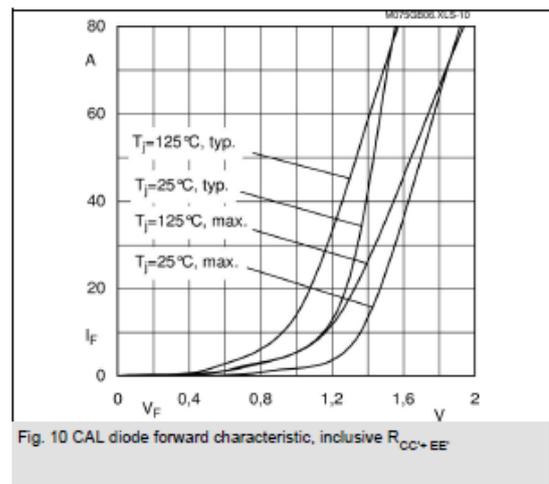
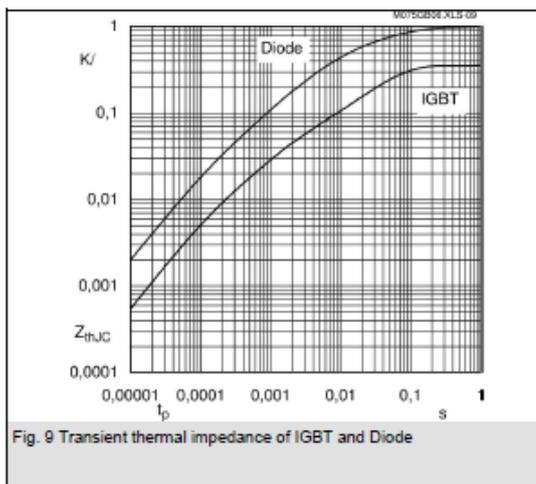
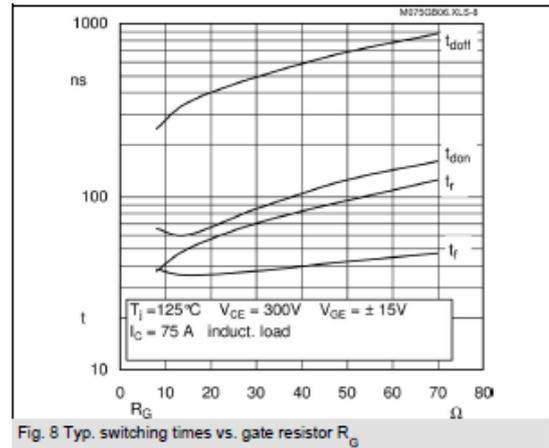
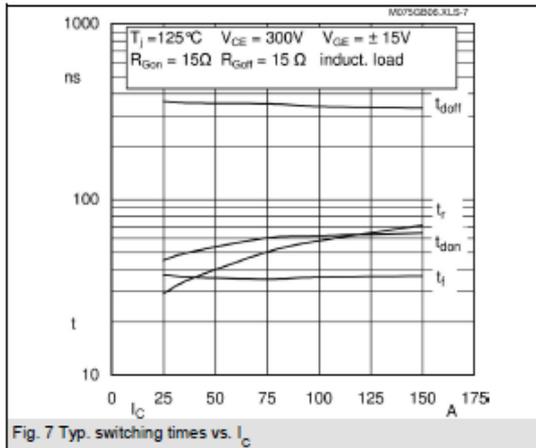
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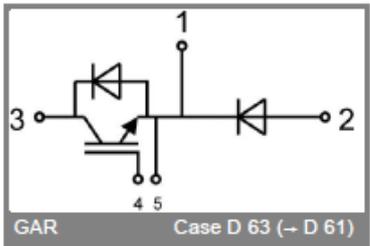
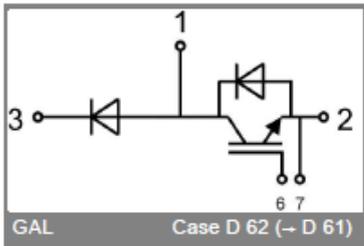
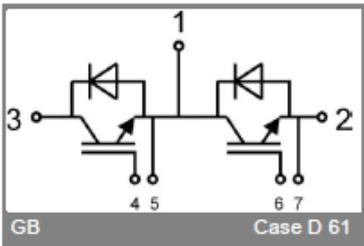
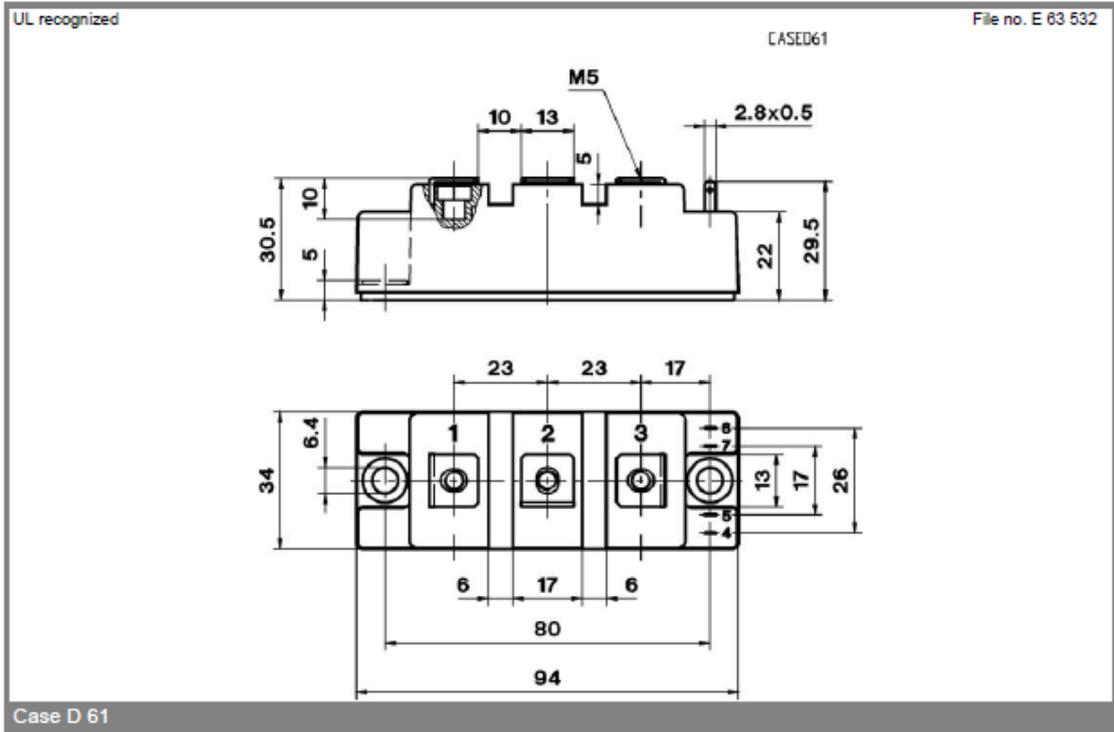
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Absolute Maximum Ratings		$T_c = 25^\circ\text{C}$ , unless otherwise specified		
Symbol	Conditions	Values	Units	
<b>IGBT</b>				
$V_{CES}$	$T_j = 25^\circ\text{C}$	600	V	
$I_C$	$T_j = 150^\circ\text{C}$	$T_{case} = 25^\circ\text{C}$	100	A
		$T_{case} = 75^\circ\text{C}$	75	A
$I_{CRM}$	$I_{CRM} = 2 \times I_{Cnom}$	150	A	
$V_{GES}$		$\pm 20$	V	
$t_{\mu s}$	$V_{CC} = 300\text{ V}; V_{GE} \leq 20\text{ V}; T_j = 125^\circ\text{C}$ $V_{CES} < 600\text{ V}$	10	$\mu\text{s}$	
<b>Inverse Diode</b>				
$I_F$	$T_j = 150^\circ\text{C}$	$T_{case} = 25^\circ\text{C}$	75	A
		$T_{case} = 80^\circ\text{C}$	50	A
$I_{FRM}$	$I_{FRM} = 2 \times I_{Fnom}$	150	A	
$I_{FSM}$	$t_p = 10\text{ ms}; \text{sin.}$	$T_j = 150^\circ\text{C}$	440	A
<b>Freewheeling Diode</b>				
$I_F$	$T_j = 150^\circ\text{C}$	$T_c = 25^\circ\text{C}$	100	A
		$T_c = 80^\circ\text{C}$	75	A
$I_{FRM}$	$I_{FRM} = 2 \times I_{Fnom}$	200	A	
$I_{FSM}$	$t_p = 10\text{ ms}; \text{sin}$	$T_j = 150^\circ\text{C}$	720	A
<b>Module</b>				
$I_{T(RMS)}$		200	A	
$T_{vj}$		- 40 ... + 150	$^\circ\text{C}$	
$T_{stg}$		- 40 ... + 125	$^\circ\text{C}$	
$V_{isol}$	AC, 1 min.	2500	V	

Characteristics		$T_c = 25^\circ\text{C}$ , unless otherwise specified			
Symbol	Conditions	min.	typ.	max.	Units
<b>IGBT</b>					
$V_{GE(th)}$	$V_{GE} = V_{CE}; I_C = 1\text{ mA}$	4,5	5,5	6,5	V
$I_{CES}$	$V_{GE} = 0\text{ V}; V_{CE} = V_{CES}$		0,1	0,3	mA
$V_{CE0}$		$T_j = 25^\circ\text{C}$	1,05		V
		$T_j = 125^\circ\text{C}$	1		V
$r_{CE}$	$V_{GE} = 15\text{ V}$	$T_j = 25^\circ\text{C}$	14		m $\Omega$
		$T_j = 125^\circ\text{C}$	18,7		m $\Omega$
$V_{CE(sat)}$	$I_{Cnom} = 75\text{ A}; V_{GE} = 15\text{ V}$	$T_j = 25^\circ\text{C}_{chiplev.}$	2,1	2,5	V
		$T_j = 125^\circ\text{C}_{chiplev.}$	2,4	2,8	V
$C_{ies}$	$V_{CE} = 25\text{ V}; V_{GE} = 0\text{ V}$	$f = 1\text{ MHz}$	4,2		nF
$C_{oes}$			0,5		nF
$C_{res}$			0,3		nF
$Q_G$	$V_{GE} = 0\text{ V} \dots +15\text{ V}$		180		nC
$R_{Gint}$	$T_j = ^\circ\text{C}$		0		$\Omega$
$t_{d(on)}$	$R_{Gon} = 15\ \Omega$	$V_{CC} = 300\text{ V}$ $I_C = 75\text{ A}$	60		ns
			50		ns
$t_r$	$R_{Goff} = 15\ \Omega$	$T_j = 125^\circ\text{C}$ $V_{GE} = \pm 15\text{ V}$	3		mJ
			350		ns
$t_{d(off)}$			35		ns
			2,5		mJ
$R_{th(j-c)}$	per IGBT		0,35		K/W

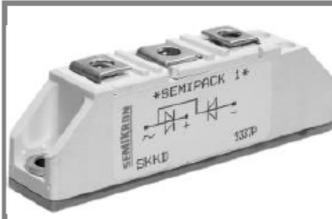








## SKKD 40F, SKMD 40F



SEMIPACK® 1

### Fast Diode Modules

SKKD 40F  
SKMD 40F

#### Features

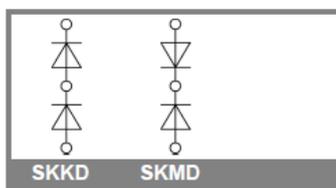
- Heat transfer through ceramic isolated metal baseplate
- Hard soldered joints for high reliability
- SKKD half bridge connection; SKMD centre tap connection, common cathode
- UL recognized, file no. E 63 532

#### Typical Applications\*

- Self-commutated inverters
- DC choppers
- AC motor speed control
- Inductive heating
- Uninterruptible power supplies
- Electronic welders
- General power switching application

$V_{RSM}$ V	$V_{RRM}$ V	$I_{FRMS} = 110$ A (maximum value for continuous operation) $I_{FAV} = 40$ A (sin. 180°; 50Hz; $T_c = 80$ °C)	
400	400	SKKD 40F04	SKMD 40F04
600	600	SKKD 40F06	SKMD 40F06
800	800	SKKD 40F08	SKMD 40F08
1000	1000	SKKD 40F10	SKMD 40F10

Symbol	Conditions	Values	Units
$I_{FAV}$	sin. 180; $T_c = 85$ (100) °C	37 (25)	A
$I_{FSM}$	$T_{vj} = 25$ °C; 10 ms $T_{vj} = 125$ °C; 10 ms	1100 940	A
$t_t$	$T_{vj} = 25$ °C; 8,3 ... 10 ms $T_{vj} = 125$ °C; 8,3 ... 10 ms	6000 4400	A*s A*s
$V_F$	$T_{vj} = 25$ °C; $I_F = 150$ A	max. 2	V
$V_{(TO)}$	$T_{vj} = 125$ °C	max. 1,2	V
$r_T$	$T_{vj} = 125$ °C	max. 4	mΩ
$I_{RD}$	$T_{vj} = 25$ °C; $V_{RD} = V_{RRM}$	max. 0,5	mA
$I_{RD}$	$T_{vj} = 125$ °C; $V_{RD} = V_{RRM}$	max. 50	mA
$Q_{tr}$	$T_{vj} = 125$ °C; $I_F = 100$ A, $-di/dt = 30$ A/μs, $V_R = 30$ V	3 10	μC A
$t_{tr}$		600	ns
$E_{tr}$		0,05	mJ
$R_{th(j-c)}$	per diode / per module	0,7 / 0,35	K/W
$R_{th(c-s)}$	per diode / per module	0,2 / 0,1	K/W
$T_{vj}$		- 40 ... + 125	°C
$T_{stg}$		- 40 ... + 125	°C
$V_{isol}$	a. c. 50 Hz; r.m.s.; 1 s / 1 min.	3600 / 3000	V~
$M_s$	to heatsink	5 ± 15 %	Nm
$M_t$	to terminals	3 ± 15%	Nm
a		5 * 9,81	m/s <sup>2</sup>
m	approx.	120	g
Case	SKKD SKMD	A 10 A 11	



SKKD

SKMD

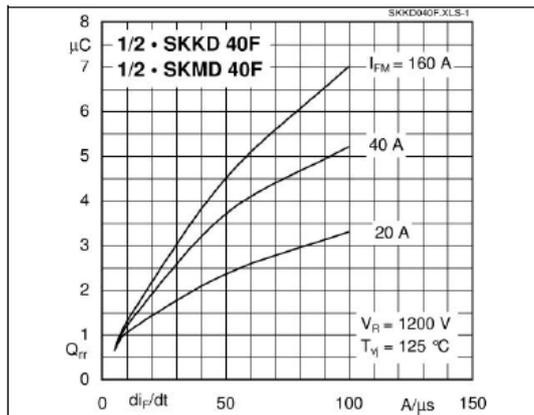


Fig. 1 Typ. recovery charge vs. current decrease

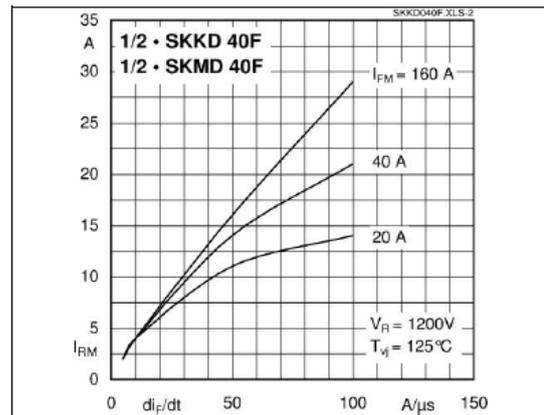


Fig. 2 Peak recovery current vs. current decrease

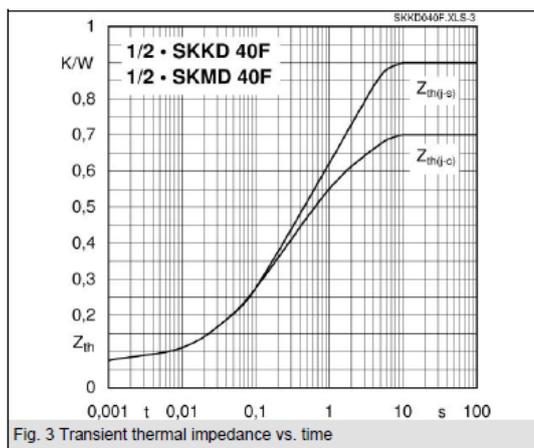


Fig. 3 Transient thermal impedance vs. time

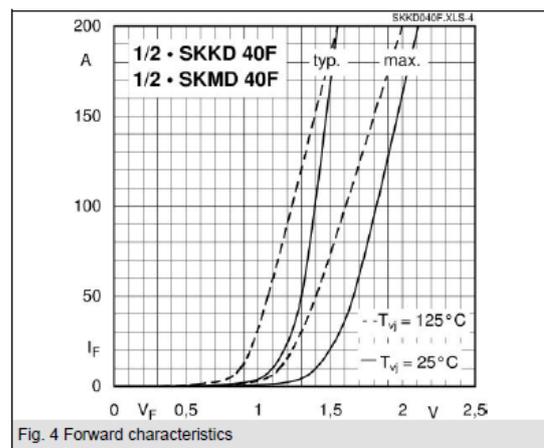


Fig. 4 Forward characteristics

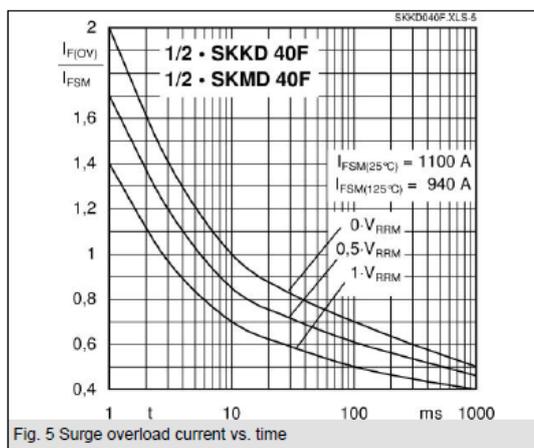
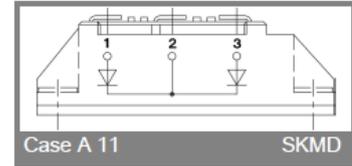
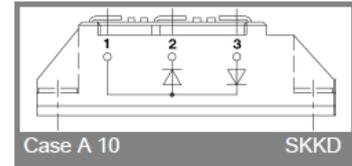
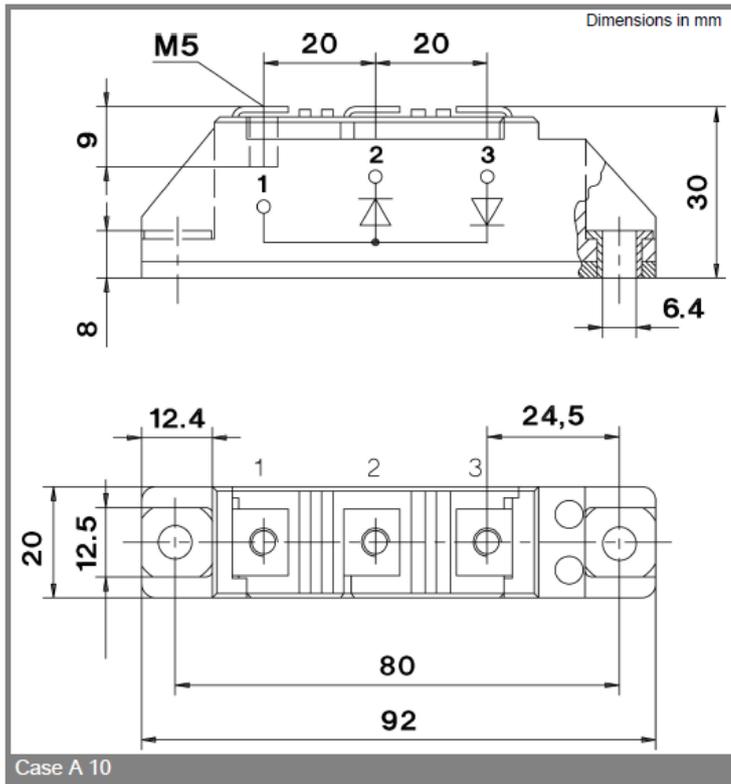


Fig. 5 Surge overload current vs. time





## SKHI 22 A / B (R) ...



**SEMIDRIVER™**

Hybrid Dual IGBT Driver

SKHI 22 A / B (R)

### Features

- Double driver for halfbridge IGBT modules
- SKHI 22A is compatible to old SKHI 22
- SKHI 22B has additional functionality
- CMOS compatible inputs
- Short circuit protection by  $V_{CE}$  monitoring and switch off
- Drive interlock top / bottom
- Isolation by transformers
- Supply undervoltage protection (13 V)
- Error latch / output

### Typical Applications

- Driver for IGBT modules in bridge circuits in industrial applications

1) see fig. 6

2) At  $R_{CE} = 18 \text{ k}\Omega$ ,  $C_{CE} = 330 \text{ pF}$

### Absolute Maximum Ratings

Symbol	Conditions	Values	Units
$V_S$	Supply voltage prim.	18	V
$V_{IH}$	Input signal volt. (High) SKHI 22A	$V_S + 0,3$	V
	SKHI 22B	$5 + 0,3$	V
$I_{outPEAK}$	Output peak current	8	A
$I_{outAVmax}$	Output average current	40	mA
$f_{max}$	max. switching frequency	50	kHz
$V_{CE}$	Collector emitter voltage sense across the IGBT	1200	V
$dv/dt$	Rate of rise and fall of voltage secondary to primary side	50	kV/ $\mu$ s
$V_{isolIO}$	Isolation test voltage input - output (2 sec. AC)	2500	Vac
$V_{isol12}$	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
$R_{Gonmin}$	Minimum rating for $R_{Gon}$	3	$\Omega$
$R_{Goffmin}$	Minimum rating for $R_{Goff}$	3	$\Omega$
$Q_{out/pulse}$	Max. rating for output charge per pulse	4 <sup>1)</sup>	$\mu$ C
$T_{op}$	Operating temperature	- 40 ... + 85	$^{\circ}$ C
$T_{stg}$	Storage temperature	- 40 ... + 85	$^{\circ}$ C

### Characteristics

$T_a = 25^{\circ}\text{C}$ , unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
$V_S$	Supply voltage primary side	14,4	15	15,6	V
$I_{SO}$	Supply current primary side (no load)		80		mA
	Supply current primary side (max.)			290	mA
$V_i$	Input signal voltage SKHI 22A on/off		15 / 0		V
	SKHI 22B on/off		5 / 0		V
$V_{IT+}$	Input threshold voltage (High) SKHI 22A			12,5	V
	SKHI 22B			3,9	V
$V_{IT-}$	Input threshold voltage (Low) SKHI 22A	4,5			V
	SKHI 22B	1,5			V
$R_{in}$	Input resistance SKHI 22A		10		k $\Omega$
	SKHI 22B		3,3		k $\Omega$
$V_{G(on)}$	Turn on gate voltage output		+ 15		V
$V_{G(off)}$	Turn off gate voltage output		- 7		V
$R_{GE}$	Internal gate-emitter resistance		22		k $\Omega$
$f_{ASIC}$	Asic system switching frequency		8		MHz
$t_{d(on)IO}$	Input-output turn-on propagation time	0,85	1	1,15	$\mu$ s
$t_{d(off)IO}$	Input-output turn-off propagation time	0,85	1	1,15	$\mu$ s
$t_{d(ert)}$	Error input-output propagation time		0,6		$\mu$ s
$t_{pERRRESET}$	Error reset time		9		$\mu$ s
$t_{TD}$	Top-Bot Interlock Dead Time SKHI 22A		4,3		$\mu$ s
	SKHI 22B	no interlock		4,7	$\mu$ s
$V_{CEsat}$	Reference voltage for $V_{CE}$ -monitoring		5 <sup>2)</sup>	10	V
$C_{ps}$	Coupling capacitance primary secondary		12		pF
MTBF	Mean Time Between Failure $T_a = 40^{\circ}\text{C}$		2,0		$10^6$ h
w	weight		45		g



Component	Function	Recommended Value
$R_{CE}$	Reference voltage for $V_{CE}$ -monitoring $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1,4 \quad (1)$ with $R_{VCE} = 1k\Omega$ (1700V IGBT): $V_{CEstat}(V) = \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} - 1,8 \quad (1.1)$	$10k\Omega < R_{CE} < 100k\Omega$ 18k $\Omega$ for SKM XX 123 (1200V) 36k $\Omega$ for SKM XX 173 (1700V)
$C_{CE}$	Inhibit time for $V_{CE}$ - monitoring $t_{min} = \tau_{CE} \cdot \ln \left[ \frac{15 - V_{CEstat}(V)}{10 - V_{CEstat}(V)} \right] \quad (2)$ $\tau_{CE}(\mu s) = C_{CE}(nF) \cdot \frac{10 \cdot R_{CE}(k\Omega)}{10 + R_{CE}(k\Omega)} \quad (3)$	$C_{CE} < 2,7nF$ 0,33nF for SKM XX 123 (1200V) 0,47nF for SKM XX 173 (1700V) 0,5 $\mu s < t_{min} < 10\mu s$
$R_{VCE}$	Collector series resistance for 1700V IGBT-operation	1k $\Omega$ / 0,4W
$R_{ERROR}$	Pull-up resistance at error output $\frac{U_{Pull-Up} < 15mA}{R_{ERROR}}$	$1k\Omega < R_{ERROR} < 10k\Omega$
$R_{GON}$	Turn-on speed of the IGBT <sup>4)</sup>	$R_{GON} > 3\Omega$
$R_{GOFF}$	Turn-off speed of the IGBT <sup>5)</sup>	$R_{GOFF} > 3\Omega$

<sup>4)</sup> Higher resistance reduces free-wheeling diode peak recovery current, increases IGBT turn-on time.

<sup>5)</sup> Higher resistance reduces turn-off peak voltage, increases turn-off time and turn-off power dissipation



## PIN array

Fig. 2 shows the pin arrays. The input side (primary side) comprises 10 inputs (SKHI 22A / 21A 8 inputs), forming the interface to the control circuit (see fig.1).

The output side (secondary side) of the hybrid driver shows two symmetrical groups of pins with 4 outputs, each forming the interface to the power module. All pins are designed for a grid of 2,54 mm.

### Primary side PIN array

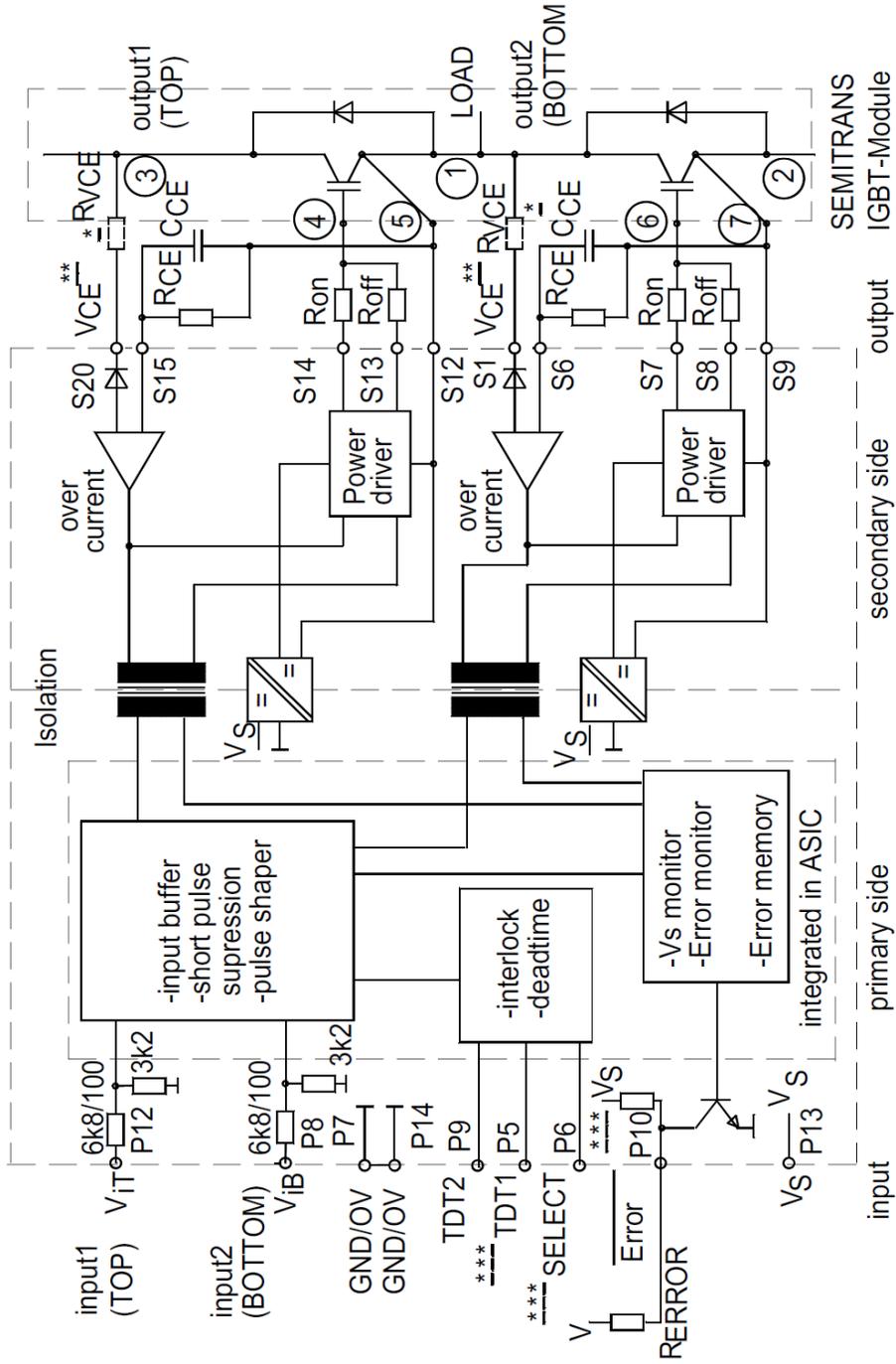
PIN No.	Designation	Explanation
P14	GND / 0V	related earth connection for input signals
P13	V <sub>S</sub>	+ 15V ± 4% voltage supply
P12	V <sub>IN1</sub>	switching signal input 1 (TOP switch) positive 5V logic (for SKHI22A /21A, 15V logic)
P11	free	not wired
P10	/ERROR	error output, low = error; open collector output; max 30V / 15mA (for SKHI22A /21A, internal 10kΩ pull-up resistor versus V <sub>S</sub> )
P9	TDT2	signal input for digital adjustment of interlocking time; <b>SKHI22B: to be switched by bridge to GND (see fig. 3)</b> <b>SKHI22A /21A: to be switched by bridge to V<sub>S</sub></b>
P8	V <sub>IN2</sub>	switching signal input 2 (BOTTOM switch); positive 5V logic (for SKHI22A /21A, 15V logic)
P7	GND / 0V	related earth connection for input signals
P6	SELECT	signal input for neutralizing locking function; to be switched by bridge to GND
P5	TDT1	signal input for digital adjustment of locking time; to be switched by bridge to GND

**ATTENTION:** Inputs P6 and P5 are not existing for SKHI 22A/ 21A. The contactor tracks of the digital input signals P5/ P6/ P9 must not be longer than 20 mm to avoid interferences, if no bridges are connected.

### Secondary side PIN array

PIN No.	Designation	Explanation
S20	V <sub>CE1</sub>	collector output IGBT 1 (TOP switch)
S15	C <sub>CE1</sub>	reference voltage adjustment with R <sub>CE</sub> and C <sub>CE</sub>
S14	G <sub>ON1</sub>	gate 1 R <sub>ON</sub> output
S13	G <sub>OFF1</sub>	gate 1 R <sub>OFF</sub> output
S12	E1	emitter output IGBT 1 (TOP switch)
S1	V <sub>CE2</sub>	collector output IGBT 2 (BOTTOM switch)
S6	C <sub>CE2</sub>	reference voltage adjustment with R <sub>CE</sub> and C <sub>CE</sub>
S7	G <sub>ON2</sub>	gate 2 R <sub>ON</sub> output
S8	G <sub>OFF2</sub>	gate 2 R <sub>OFF</sub> output
S9	E2	emitter output IGBT 2 (BOTTOM switch)

**ATTENTION:** The connector leads to the power module should be as short as possible.



\* When SKHI22B is driving 1700V IGBTs, a 1kΩ / 0.4W R<sub>VCE</sub>-resistor must be connected in series to the V<sub>CE</sub> input.  
 \*\* The V<sub>CE</sub>-terminal is to be connected to the IGBT collector C. If the V<sub>CE</sub>-monitoring is not used, connect S1 to S9 or S20 to S12 respectively.  
 \*\*\* Terminals P5 and P6 are not existing for SKHI22A/21A; internal pull-up resistor exists in SKHI22A/21A only.  
 1-7 Connections to SEMISTRANS GB-module

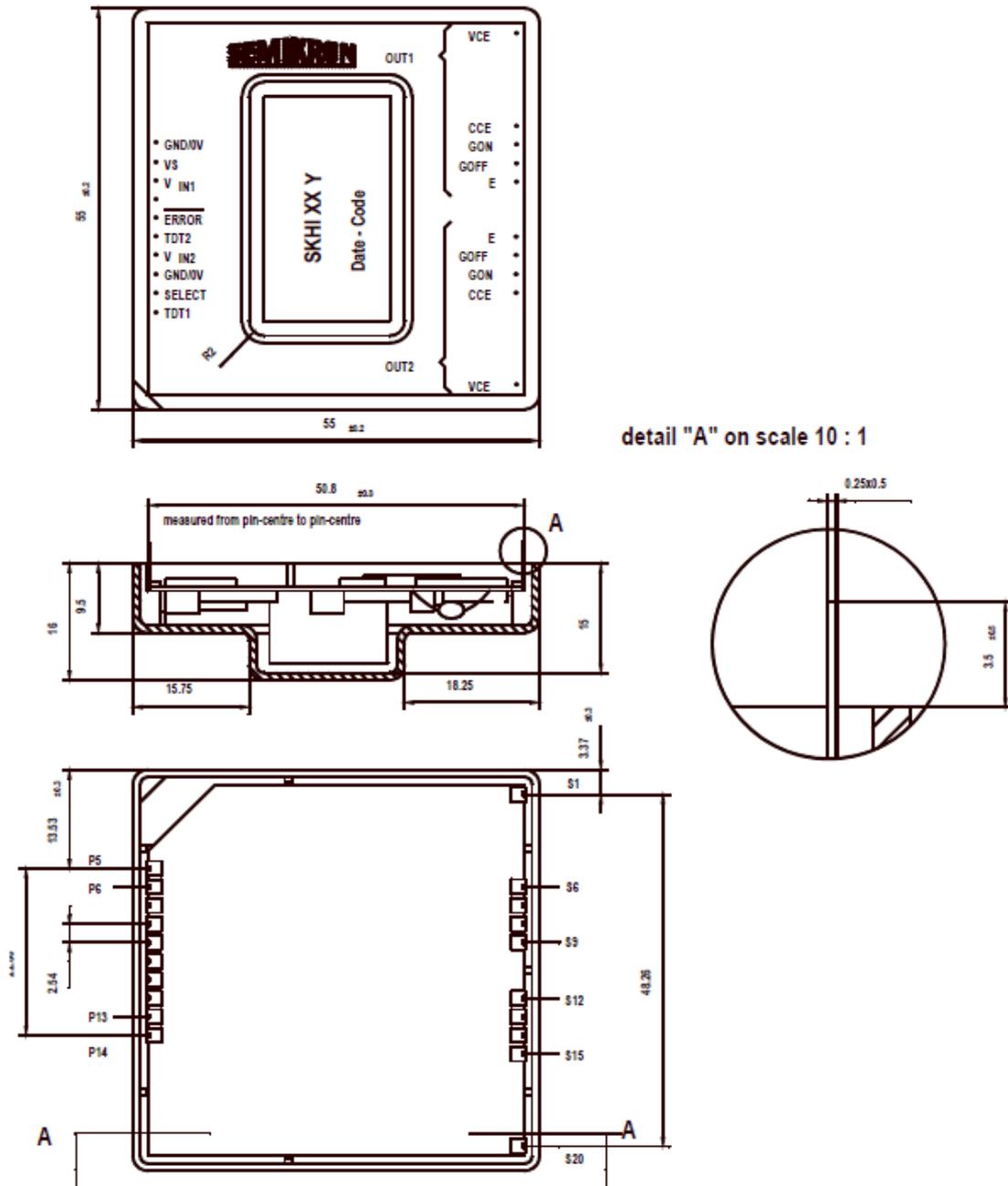


Fig. 2 Dimension drawing and PIN array (P5 and P6 are not existing for SKHI22A/21A)



## SEMIDRIVER™

### SKHI 22A / 22B und SKHI 21A

#### Hybrid dual drivers

The driver generation SKHI 22A/B and SKHI 21A will replace the hybrid drivers SKHI 21/22 and is suitable for all available low and medium power range IGBT and MOSFETs.

The SKHI 22A (SKHI 21A) is a form-, fit- and mostly function-compatible replacement to its predecessor, the SKHI 22 (SKHI 21).

The SKHI 22B is recommended for any new development. It has two additional signal pins on the primary side with which further functions may be utilized.

The SKHI 22A and SKHI 22B are available with standard isolation (isolation testing voltage 2500 VAC, 2sec.) as well as with an increased isolation voltage (type "H4") (isolation testing voltage 4000 VAC, 2sec.). The SKHI 21A is only offered with standard isolation features.

#### Differences SKHI 22-22A (SKHI 21-21A)

Compared to the old SKHI 22/21 the new driver SKHI 22A / 21A is absolutely compatible with regards to pins and mostly with regards to functions. It may be equivalently used in existing PCBs.

The following points have to be considered when exchanging the drivers:

- Leave out the two resistors RTD for interlocking dead time adjustment at pin 11 and pin 9.
- The interlocking time of the driver stages in halfbridge applications is adjusted to 3,25 µs. It may be increased up to 4,25 µs by applying a 15 V (VS) supply voltage at Pin 9 (TDT2) (wire bridge)
- The error reset time is typically 9µs.
- The input resistance is 10 kΩ.

As far as the SKHI 22A is concerned, the negative gate voltage required for turn-off of the IGBT is no longer -15V, but -7V.

#### General description

The new driver generation SKHI 22A/B, SKHI 21A consists of a hybrid component which may directly be mounted to the PCB.

All devices necessary for driving, voltage supply, error monitoring and potential separation are integrated in the driver. In order to adapt the driver to the used power module, only very few additional wiring may be necessary.

The forward voltage of the IGBT is detected by an integrated short-circuit protection, which will turn off the module when a certain threshold is exceeded.

In case of short-circuit or too low supply voltage the integrated error memory is set and an error signal is generated.

The driver is connected to a controlled + 15 V-supply voltage. The input signal level is 0/15 V for the SKHI 22A/ 21A and 0/5 V for the SKHI 22B.

In the following explanations the whole driver family will be designated as SKHI 22B. If a special type is referred to, the concerned driver version will explicitly be named.

### Technical explanations<sup>1</sup>

#### Description of the circuit block diagram and the functions of the driver

The block diagram (fig.1) shows the inputs of the driver (primary side) on the left side and the outputs (secondary side) on the right.

The following functions are allocated to the primary side:

**Input-Schmitt-trigger**, CMOS compatible, positive logic (input high = IGBT on)

#### Interlock circuit and deadtime generation of the IGBT

If one IGBT is turned on, the other IGBT of a halfbridge cannot be switched. Additionally, a digitally adjustable interlocking time is generated by the driver (see fig. 3), which has to be longer than the turn-off delay time of the IGBT. This is to avoid that one IGBT is turned on before the other one is not completely discharged. This protection-function may be neutralized by switching the select input (pin6) (see fig. 3). fig. 3 documents possible interlock-times. "High" value can be achieved with no connection and connection to 5 V as well.

P6 ; SELECT	P5 ; TDT1	P9 ; TDT2	interlock time t <sub>TD</sub> /µs
open / 5V	GND	GND	1,3
open / 5V	GND	open / 5V	2,3
open / 5V	open / 5V	GND	3,3
open / 5V	open / 5V	open / 5V	4,3
GND	X	X	no interlock

Fig. 3 SKHI 22B - Selection of interlock-times: „High“-level can be achieved by no connection or connecting to 5 V

#### Short pulse suppression

The integrated short pulse suppression avoids very short switching pulses at the power semiconductor caused by high-frequency interference pulses at the driver input signals. Switching pulses shorter than 500 ns are suppressed and not transmitted to the IGBT.

#### Power supply monitoring (VS)

A controlled 15 V-supply voltage is applied to the driver. If it falls below 13 V, an error is monitored and the error output signal switches to low level.

<sup>1</sup>The following descriptions apply to the use of the hybrid driver for IGBTs as well as for power MOSFETs. For the reason of shortness, only IGBTs will be mentioned in the following. The designations "collector" and "emitter" will refer to IGBTs, whereas for the MOSFETs "drain" and "source" are to be read instead.



### Error monitoring and error memory

The error memory is set in case of under-voltage or short-circuit of the IGBTs. In case of short-circuit, an error signal is transmitted by the  $V_{CE}$ -input via the pulse transformers to the error memory. The error memory will lock all switching pulses to the IGBTs and trigger the error output (P10) of the driver. The error output consists of an open collector transistor, which directs the signal to earth in case of error. SEMIKRON recommends the user to provide for a pull-up resistor directly connected to the error evaluation board and to adapt the error level to the desired signal voltage this way. The open collector transistor may be connected to max. 30 V / 15 mA. If several SKHI 22Bs are used in one device, the error terminals may also be paralleled.

**ATTENTION:** Only the SKHI 22A / 21A is equipped with an internal pull-up resistor of 10 k $\Omega$  versus  $V_G$ . The SKHI 22B does not contain an internal pull-up resistor.

The error memory may only be reset, if no error is pending and both cycle signal inputs are set to low for > 9  $\mu$ s at the same time.

### Pulse transformer set

The transformer set consists of two pulse transformers one is used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between primary and secondary side, the other one for the DC/DC-converter. The DC/DC-converter serves as potential-separation and power supply for the two secondary sides of the driver. The isolation voltage for the "H4"-type is 4000  $V_{AC}$  and 2500  $V_{AC}$  for all other types.

The secondary side consists of two symmetrical driver switches integrating the following components:

### Supply voltage

The voltage supply consists of a rectifier, a capacitor, a voltage controller for - 7 V and + 15 V and a + 10 V reference voltage.

### Gate driver

The output transistors of the power drivers are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed by the external resistors  $R_{ON}$  and  $R_{OFF}$ . Do not connect the terminals S7 with S8 and S13 with S14, respectively. The IGBT is turned on by the driver at + 15 V by  $R_{ON}$  and turned off at - 7 V by  $R_{OFF}$ .  $R_{ON}$  and  $R_{OFF}$  may not be chosen below 3  $\Omega$ . In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a 22 k $\Omega$ -resistor versus the emitter output (E) has been integrated at output  $G_{OFF}$ .

### $V_{CE}$ -monitoring

The  $V_{CE}$ -monitoring controls the collector-emitter voltage  $V_{CE}$  of the IGBT during its on-state.  $V_{CE}$  is internally limited to 10 V. If the reference voltage  $V_{CEref}$  is exceeded, the IGBT will be switched off and an error is indicated. The reference voltage  $V_{CEref}$  may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in the steady state. This value will, however, be reset, when the

IGBT is turned off.  $V_{CEstat}$  is the steady-state value of  $V_{CEref}$  and is adjusted to the required maximum value for each IGBT by an external resistor  $R_{CE}$  to be connected between the terminals  $C_{CE}$  (S6/S15) and E (S9/S12). It may not exceed 10 V. The time constant for the delay of  $V_{CEref}$  may be increased by an external capacitor  $C_{CE}$ , which is connected in parallel to  $R_{CE}$ . It controls the time  $t_{min}$  which passes after turn-on of the IGBT before the  $V_{CE}$ -monitoring is activated. This makes possible any adaptation to the switching behavior of any of the IGBTs. After  $t_{min}$  has passed, the  $V_{CE}$ -monitoring will be triggered as soon as  $V_{CE} > V_{CEref}$  and will turn off the IGBT.

### External components and possible adjustments of the hybrid driver

Fig. 1 shows the required external components for adjustment and adaptation to the power module.

### $V_{CE}$ - monitoring adjustment

The external components  $R_{CE}$  and  $C_{CE}$  are applied for adjusting the steady-state threshold and the short-circuit monitoring dynamic.  $R_{CE}$  and  $C_{CE}$  are connected in parallel to the terminals  $C_{CE}$  (S15/ S6) and E (S12/ S9).

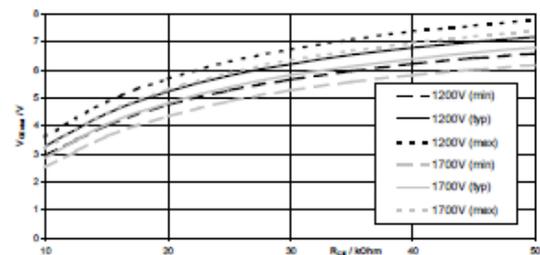


Fig. 4  $V_{CEstat}$  in dependence of  $R_{CE}$  ( $T_{amb} = 25^{\circ}C$ )

Dimensioning of  $R_{CE}$  and  $C_{CE}$  can be done in three steps:

1. Calculate the maximum forward voltage from the datasheet of the used IGBT and determine  $V_{CEstat}$
2. Calculate approximate value of  $R_{CE}$  according to equation (1) or (1.1) from  $V_{CEstat}$  or determine  $R_{CE}$  by using fig.4.
3. Determine  $t_{min}$  and calculate  $C_{CE}$  according to equations (2) and (3).

Typical values are

for 1200 V IGBT:  $V_{CEstat} = 5$  V;  $t_{min} = 1,45$   $\mu$ s,  
 $R_{CE} = 18$  k $\Omega$ ,  $C_{CE} = 330$  pF

for 1700 V IGBT:  $V_{CEstat} = 6$  V;  $t_{min} = 3$   $\mu$ s,  
 $R_{CE} = 36$  k $\Omega$ ,  $C_{CE} = 470$  pF

### Adaptation to 1700 V IGBT

When using 1700 V IGBTs it is necessary to connect a 1 k $\Omega$  / 0,4 W adaptation resistor between the  $V_{CE}$ -terminal (S20/ S1) and the respective collector.



### Error monitoring and error memory

The error memory is set in case of under-voltage or short-circuit of the IGBTs. In case of short-circuit, an error signal is transmitted by the  $V_{CE}$ -input via the pulse transformers to the error memory. The error memory will lock all switching pulses to the IGBTs and trigger the error output (P10) of the driver. The error output consists of an open collector transistor, which directs the signal to earth in case of error. SEMIKRON recommends the user to provide for a pull-up resistor directly connected to the error evaluation board and to adapt the error level to the desired signal voltage this way. The open collector transistor may be connected to max. 30 V / 15 mA. If several SKHI 22Bs are used in one device, the error terminals may also be paralleled.

**ATTENTION:** Only the SKHI 22A / 21A is equipped with an internal pull-up resistor of 10 k $\Omega$  versus  $V_G$ . The SKHI 22B does not contain an internal pull-up resistor.

The error memory may only be reset, if no error is pending and both cycle signal inputs are set to low for > 9  $\mu$ s at the same time.

### Pulse transformer set

The transformer set consists of two pulse transformers one is used bidirectional for turn-on and turn-off signals of the IGBT and the error feedback between primary and secondary side, the other one for the DC/DC-converter. The DC/DC-converter serves as potential-separation and power supply for the two secondary sides of the driver. The isolation voltage for the "H4"-type is 4000  $V_{AC}$  and 2500  $V_{AC}$  for all other types.

The secondary side consists of two symmetrical driver switches integrating the following components:

### Supply voltage

The voltage supply consists of a rectifier, a capacitor, a voltage controller for - 7 V and + 15 V and a + 10 V reference voltage.

### Gate driver

The output transistors of the power drivers are MOSFETs. The sources of the MOSFETs are separately connected to external terminals in order to provide setting of the turn-on and turn-off speed by the external resistors  $R_{ON}$  and  $R_{OFF}$ . Do not connect the terminals S7 with S8 and S13 with S14, respectively. The IGBT is turned on by the driver at + 15 V by  $R_{ON}$  and turned off at - 7 V by  $R_{OFF}$ .  $R_{ON}$  and  $R_{OFF}$  may not be chosen below 3  $\Omega$ . In order to ensure locking of the IGBT even when the driver supply voltage is turned off, a 22 k $\Omega$ -resistor versus the emitter output (E) has been integrated at output  $G_{OFF}$ .

### $V_{CE}$ -monitoring

The  $V_{CE}$ -monitoring controls the collector-emitter voltage  $V_{CE}$  of the IGBT during its on-state.  $V_{CE}$  is internally limited to 10 V. If the reference voltage  $V_{CEref}$  is exceeded, the IGBT will be switched off and an error is indicated. The reference voltage  $V_{CEref}$  may dynamically be adapted to the IGBTs switching behaviour. Immediately after turn-on of the IGBT, a higher value is effective than in the steady state. This value will, however, be reset, when the

IGBT is turned off.  $V_{CEstat}$  is the steady-state value of  $V_{CEref}$  and is adjusted to the required maximum value for each IGBT by an external resistor  $R_{CE}$  to be connected between the terminals  $C_{CE}$  (S6/S15) and E (S9/S12). It may not exceed 10 V. The time constant for the delay of  $V_{CEref}$  may be increased by an external capacitor  $C_{CE}$ , which is connected in parallel to  $R_{CE}$ . It controls the time  $t_{min}$  which passes after turn-on of the IGBT before the  $V_{CE}$ -monitoring is activated. This makes possible any adaptation to the switching behavior of any of the IGBTs. After  $t_{min}$  has passed, the  $V_{CE}$ -monitoring will be triggered as soon as  $V_{CE} > V_{CEref}$  and will turn off the IGBT.

### External components and possible adjustments of the hybrid driver

Fig. 1 shows the required external components for adjustment and adaptation to the power module.

### $V_{CE}$ - monitoring adjustment

The external components  $R_{CE}$  and  $C_{CE}$  are applied for adjusting the steady-state threshold and the short-circuit monitoring dynamic.  $R_{CE}$  and  $C_{CE}$  are connected in parallel to the terminals  $C_{CE}$  (S15/ S6) and E (S12/ S9) .

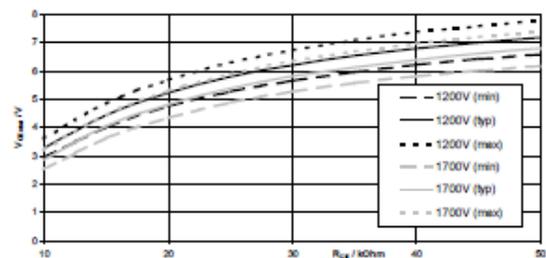


Fig. 4  $V_{CEstat}$  in dependence of  $R_{CE}$  ( $T_{amb} = 25^{\circ}C$ )

Dimensioning of  $R_{CE}$  and  $C_{CE}$  can be done in three steps:

1. Calculate the maximum forward voltage from the datasheet of the used IGBT and determine  $V_{CEstat}$
2. Calculate approximate value of  $R_{CE}$  according to equation (1) or (1.1) from  $V_{CEstat}$  or determine  $R_{CE}$  by using fig.4.
3. Determine  $t_{min}$  and calculate  $C_{CE}$  according to equations (2) and (3).

Typical values are

for 1200 V IGBT:  $V_{CEstat} = 5$  V;  $t_{min} = 1,45$   $\mu$ s,  
 $R_{CE} = 18$  k $\Omega$ ,  $C_{CE} = 330$  pF

for 1700 V IGBT:  $V_{CEstat} = 6$  V;  $t_{min} = 3$   $\mu$ s,  
 $R_{CE} = 36$  k $\Omega$ ,  $C_{CE} = 470$  pF

### Adaptation to 1700 V IGBT

When using 1700 V IGBTs it is necessary to connect a 1 k $\Omega$  / 0,4 W adaptation resistor between the  $V_{CE}$ -terminal (S20/ S1) and the respective collector.



### Adaptation to error signal level

An open collector transistor is used as error terminal, which, in case of error, leads the signal to earth. The signal has to be adapted to the evaluation circuit's voltage level by means of an externally connected pull-up resistor. The maximum load applied to the transistor shall be 30 V / 15 mA.

As for the SKHI 22A / 21A a 10 kΩ pull-up resistor versus V<sub>S</sub> (P13) has already been integrated in the driver.

### IGBT switching speed adjustment

The IGBT switching speed may be adjusted by the resistors R<sub>ON</sub> and R<sub>OFF</sub>. By increasing R<sub>ON</sub> the turn-on speed will decrease. The reverse peak current of the free-wheeling diode will diminish. SEMIKRON recommends to adjust R<sub>ON</sub> to a level that will keep the turn-on delay time t<sub>d(on)</sub> of the IGBT < 1 μs.

By increasing R<sub>OFF</sub> the turn-off speed of the IGBT will decrease. The inductive peak overvoltage during turn-off will diminish.

The minimum gate resistor value for R<sub>OFF</sub> and R<sub>ON</sub> is 3 Ω. Typical values for R<sub>ON</sub> and R<sub>OFF</sub> recommended by SEMIKRON are given in fig. 5

SK-IGBT-Modul	R <sub>Gon</sub> Ω	R <sub>Goff</sub> Ω	C <sub>CE</sub> pF	R <sub>CE</sub> kΩ	R <sub>VCE</sub> kΩ
SKM 50GB123D	22	22	330	18	0
SKM 75GB123D	22	22	330	18	0
SKM 100GB123D	15	15	330	18	0
SKM 145GB123D	12	12	330	18	0
SKM 150GB123D	12	12	330	18	0
SKM 200GB123D	10	10	330	18	0
SKM 300GB123D	8,2	8,2	330	18	0
SKM 400GA123D	6,8	6,8	330	18	0
SKM 75GB173D	15	15	470	36	1
SKM 100GB173D	12	12	470	36	1
SKM 150GB173D	10	10	470	36	1
SKM 200GB173D	8,2	8,2	470	36	1

Fig. 5 Typical values for external components

### Interlocking time adjustment

Fig. 3 shows the possible interlocking times between output1 and output2. Interlocking times are adjusted by connecting the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) either to earth/ GND (P7 and P14) according to the required function or by leaving them open.

A typical interlocking time value is 3,25 μs (P9 = GND; P5 and P6 open). For SKHI 22A / 21A the terminals TDT1 (P5) and SELECT (P6) are not existing. The interlocking time has been fixed to 3,25 μs and may only be increased to 4,25 μs by connecting TDT2 (P9) to V<sub>S</sub> (P13).

**ATTENTION:** If the terminals TDT1 (P5), TDT2 (P9) and SELECT (P6) are not connected, eventually connected track on PC-board may not be longer than 20 mm in order to avoid interferences.

SEMIKRON recommends to start-up operation using the values recommended by SEMIKRON and to optimize the values gradually according to the IGBT switching behaviour and overvoltage peaks within the specific circuitry.

### Driver performance and application limits

The drivers are designed for application with halfbridges and single modules with a maximum gate charge Q<sub>GE</sub> < 4 μC (see fig. 6).

The charge necessary to switch the IGBT is mainly depending on the IGBT's chip size, the DC-link voltage and the gate voltage.

This correlation is also shown in the corresponding module datasheet curves.

It should, however, be considered that the SKHI 22B is turned on at + 15 V and turned off at - 7 V. Therefore, the gate voltage will change by 22 V during every switching procedure.

Unfortunately, most datasheets do not indicate negative gate voltages. In order to determine the required charge, the upper leg of the charge curve may be prolonged to + 22 V for determination of approximate charge per switch.

The medium output current of the driver is determined by the switching frequency and the gate charge. For the SKHI 22B the maximum medium output current is I<sub>out,AVmax</sub> < ± 40 mA.

The maximum switching frequency f<sub>MAX</sub> may be calculated with the following formula, the maximum value however being 50 kHz due to switching reasons:

$$f_{MAX}(\text{kHz}) = \frac{4 \cdot 10^4}{Q_{GE}(\text{nC})}$$

Fig. 6 shows the maximum rating for the output charge per pulse for different gate resistors.

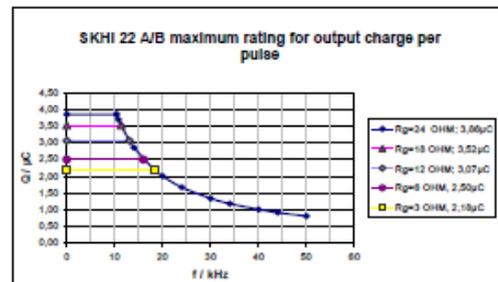


Fig. 6 Maximum rating for output charge per pulse

### Further application notes

The CMOS-inputs of the hybrid driver are extremely sensitive to over-voltage. Voltages higher than V<sub>S</sub> + 0,3 V or below - 0,3 V may destroy these inputs. Therefore, control signal over-voltages exceeding the above values have to be avoided.

Please provide for static discharge protection during handling. As long as the hybrid driver is not completely assembled, the input terminals have to be short-circuited.



Persons working with CMOS-devices have to wear a grounded bracelet. Any synthetic floor coverings must not be statically chargeable. Even during transportation the input terminals have to be short-circuited using, for example, conductive rubber. Worktables have to be grounded. The same safety requirements apply to MOSFET- and IGBT-modules!

The connecting leads between hybrid driver and the power module should be as short as possible, the driver leads should be twisted.

Any parasitic inductances within the DC-link have to be minimized. Over-voltages may be absorbed by C- or RCD-snubbers between the main terminals for PLUS and MINUS of the power module.

When first operating a newly developed circuit, SEMIKRON recommends to apply low collector voltage and load current in the beginning and to increase these values gradually, observing the turn-off behaviour of the free-wheeling diode and the turn-off voltage spikes generated across the IGBT. An oscillographic control will be necessary. In addition to that the case temperature of the module has to be monitored. When the circuit works correctly under rated operation conditions, short-circuit testing may be done, starting again with low collector voltage.

It is important to feed any errors back to the control circuit and to switch off the device immediately in such events. Repeated turn-on of the IGBT into a short circuit with a high frequency may destroy the device.

#### Mechanical fixing on PCB:

In applications with mechanical vibrations do not use a ty-rap for fixing the driver, but - after soldering and testing - apply special glue. Recommended types: CIBA GEIGY XP 5090 + 5091; PACTAN 5011; WACKER A33 (ivory) or N199 (transparent), applied around the case edge (forms a concave mould). The housing may not be pressed on the PCB; do not twist the PCB with the driver soldered on, otherwise the internal ceramics may crack. The driver is not suitable for big PCBs.

Proven, within the scope of the product qualification, was the use of the driver with the printed circuit board SKPC 2006 (L x B x H = 97,0 x 67,5 x 1,5 mm). During the test, the driver was stuck with glue on the printed circuit board. Based on this information the technical conclusion arises, that in an application with big printed circuit boards, this board must be supported and reinforced in the area of the driver.

If a PCB is directly plugged to IGBT modules, the PCB has to be fixed to the heat sink by thread bolts.

The temperature of the solder must not exceed 265°C, and solder time must not exceed 4 seconds. The ambient temperature must not exceed the specified maximum storage temperature of the driver.

The driver is not suited for hot air reflow or infrared reflow soldering processes.

#### Storage hints

- Store driver only in original packaging.
- Avoid contamination of driver's surface during storage, handling and processing.
- Please use the driver within one year after driver manufacturing date. The manufacturing date is marked on the driver. Usage of the driver beyond this shelf life could compromise product long term reliability.
- Further storage conditions are indicated in the data sheet

#### Environmental conditions

The driver is type tested under the environmental conditions below.

Thermal cycling test:

- 100 cycle -40°C ... +85°C

Vibration test according DIN IEC 68-2-6:

- Sinusoidal sweep: 10 Hz ... 100 Hz
- 1 Octave / min.
- Acceleration: 1,5 g
- Axes: 3 (x, y, z)
- 26 sweeps per axis
- Driver soldered on board SKPC 2006 (L x B x H = 97,0 x 67,5 x 1,5mm)
- Driver stuck with glue on printed circuit board (see application notes)

Shock test according DIN IEC 68-2-27:

- Half-sinusoidal pulse
- Peak acceleration: 5 g
- Shock width: 18ms
- 3 shocks in each direction ( $\pm x$ ,  $\pm y$  und  $\pm z$ )
- 18 shocks in total
- Driver soldered on board SKPC 2006 (L x B x H = 97,0 x 67,5 x 1,5mm)
- Driver stuck with glue on printed circuit board (see application notes)
- 40/085/56 (40°C, 85% RH, 56h)
- No condensation, no dripping water, non- corrosive
- Climate class 3K3

All electrical and mechanical parameters should be validated by user's technical experts for each application.

For further details please contact SEMIKRON.



## CD4049UB, CD4050B

Data sheet acquired from Harris Semiconductor  
SCHS046A

August 1998 - Revised May 1999

### CMOS Hex Buffer/Converters

The CD4049UB and CD4050B devices are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage ( $V_{CC}$ ). The input-signal high level ( $V_{IH}$ ) can exceed the  $V_{CC}$  supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. ( $V_{CC} = 5V$ ,  $V_{OL} \leq 0.4V$ , and  $I_{OL} \geq 3.3mA$ .)

The CD4049UB and CD4050B are designated as replacements for CD4009UB and CD4010B, respectively. Because the CD4049UB and CD4050B require only one power supply, they are preferred over the CD4009UB and CD4010B and should be used in place of the CD4009UB and CD4010B in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049UB and CD4050B are pin compatible with the CD4009UB and CD4010B respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049UB or CD4050B, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069UB Hex Inverter is recommended.

### Features

- CD4049UB Inverting
- CD4050B Non-Inverting
- High Sink Current for Driving 2 TTL Loads
- High-To-Low Level Logic Conversion
- 100% Tested for Quiescent Current at 20V
- Maximum Input Current of  $1\mu A$  at 18V Over Full Package Temperature Range; 100nA at 18V and 25°C
- 5V, 10V and 15V Parametric Ratings

### Applications

- CMOS to DTL/TTL Hex Converter
- CMOS Current "Sink" or "Source" Driver
- CMOS High-To-Low Logic Level Converter

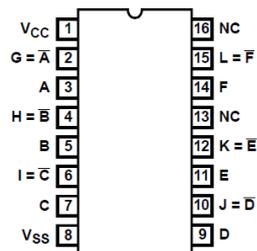
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD4049UBE	-55 to 125	16 Ld PDIP	E16.3
CD4050BE	-55 to 125	16 Ld PDIP	E16.3
CD4049UBF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BF	-55 to 125	16 Ld CERDIP	F16.3
CD4050BM	-55 to 125	16 Ld SOIC	M16.3

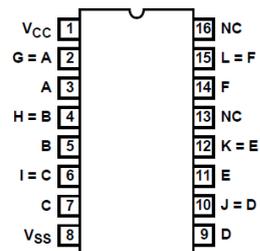
NOTE: Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or customer service for ordering information.

### Pinouts

CD4049UB (PDIP, CERDIP)  
TOP VIEW



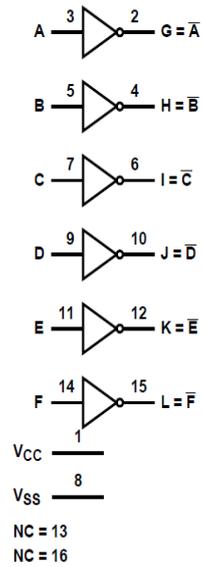
CD4050B (PDIP, CERDIP, SOIC)  
TOP VIEW



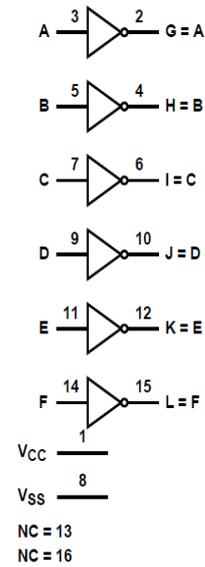


### Functional Block Diagrams

CD4049UB



CD4050B



### Schematic Diagrams

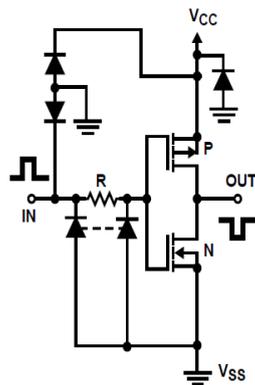


FIGURE 1A. SCHEMATIC DIAGRAM OF CD4049UB, 1 OF 6 IDENTICAL UNITS

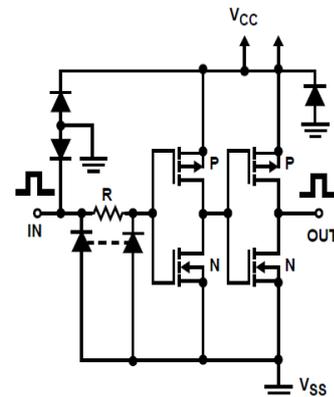


FIGURE 1B. SCHEMATIC DIAGRAM OF CD4050B, 1 OF 6 IDENTICAL UNITS



### Absolute Maximum Ratings

Supply Voltage (V+ to V-) ..... -0.5V to 20V  
 DC Input Current, Any One Input .....  $\pm 10\text{mA}$

### Operating Conditions

Temperature Range .....  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$

### Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  ( $^{\circ}\text{C}/\text{W}$ )  $\theta_{JC}$  ( $^{\circ}\text{C}/\text{W}$ )  
 PDIP Package ..... 90 N/A  
 CERDIP Package ..... 130 55  
 SOIC Package ..... 100 N/A  
 Maximum Junction Temperature (Plastic Package) .....  $150^{\circ}\text{C}$   
 Maximum Storage Temperature Range .....  $-65^{\circ}\text{C}$  to  $150^{\circ}\text{C}$   
 Maximum Lead Temperature (Soldering 10s) .....  $265^{\circ}\text{C}$   
 (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE ( $^{\circ}\text{C}$ )							UNITS
								25			
	$V_O$ (V)	$V_{IN}$ (V)	$V_{CC}$ (V)	-55	-40	85	125	MIN	TYP	MAX	
Quiescent Device Current $I_{DD}$ (Max)	-	0.5	5	1	1	30	30	-	0.02	1	$\mu\text{A}$
	-	0.10	10	2	2	60	60	-	0.02	2	$\mu\text{A}$
	-	0.15	15	4	4	120	120	-	0.02	4	$\mu\text{A}$
	-	0.20	20	20	20	600	600	-	0.04	20	$\mu\text{A}$
Output Low (Sink) Current $I_{OL}$ (Min)	0.4	0.5	4.5	3.3	3.1	2.1	1.8	2.6	5.2	-	mA
	0.4	0.5	5	4	3.8	2.9	2.4	3.2	6.4	-	mA
	0.5	0.10	10	10	9.6	6.6	5.6	8	16	-	mA
	1.5	0.15	15	26	25	20	18	24	48	-	mA
Output High (Source) Current $I_{OH}$ (Min)	4.6	0.5	5	-0.81	-0.73	-0.58	-0.48	-0.65	-1.2	-	mA
	2.5	0.5	5	-2.6	-2.4	-1.9	-1.55	-2.1	-3.9	-	mA
	9.5	0.10	10	-2.0	-1.8	-1.35	-1.18	-1.65	-3.0	-	mA
	13.5	0.15	15	-5.2	-4.8	-3.5	-3.1	-4.3	-8.0	-	mA
Out Voltage Low Level $V_{OL}$ (Max)	-	0.5	5	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0.10	10	0.05	0.05	0.05	0.05	-	0	0.05	V
	-	0.15	5	0.05	0.05	0.05	0.05	-	0	0.05	V
Output Voltage High Level $V_{OH}$ (Min)	-	0.5	5	4.95	4.95	4.95	4.95	4.95	5	-	V
	-	0.10	10	9.95	9.95	9.95	9.95	9.95	10	-	V
	-	0.15	15	14.95	14.95	14.95	14.95	14.95	15	-	V
Input Low Voltage, $V_{IL}$ (Max) CD4049UB	4.5	-	5	1	1	1	1	-	-	1	V
	9	-	10	2	2	2	2	-	-	2	V
	13.5	-	15	2.5	2.5	2.5	2.5	-	-	2.5	V
Input Low Voltage, $V_{IL}$ (Max) CD4050B	0.5	-	5	1.5	1.5	1.5	1.5	-	-	1.5	V
	1	-	10	3	3	3	3	-	-	3	V
	1.5	-	15	4	4	4	4	-	-	4	V
Input High Voltage, $V_{IH}$ Min CD4049UB	0.5	-	5	4	4	4	4	4	-	-	V
	1	-	10	8	8	8	8	8	-	-	V
	1.5	-	15	12.5	12.5	12.5	12.5	12.5	-	-	V



**DC Electrical Specifications** (Continued)

PARAMETER	TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURE (°C)							UNITS
				25							
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>CC</sub> (V)	-55	-40	85	125	MIN	TYP	MAX	
Input High Voltage, V <sub>IH</sub> Min CD4050B	4.5	-	5	3.5	3.5	3.5	3.5	3.5	-	-	V
	9	-	10	7	7	7	7	7	-	-	V
	13.5	-	15	11	11	11	11	11	-	-	V
Input Current, I <sub>IN</sub> Max	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA

**AC Electrical Specifications** T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 20ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 200kΩ

PARAMETER	TEST CONDITIONS		LIMITS (ALL PACKAGES)		UNITS
	V <sub>IN</sub>	V <sub>CC</sub>	TYP	MAX	
Propagation Delay Time Low to High, t <sub>PLH</sub> CD4049UB	5	5	60	120	ns
	10	10	32	65	ns
	10	5	45	90	ns
	15	15	25	50	ns
	15	5	45	90	ns
Propagation Delay Time Low to High, t <sub>PLH</sub> CD4050B	5	5	70	140	ns
	10	10	40	80	ns
	10	5	45	90	ns
	15	15	30	60	ns
	15	5	40	80	ns
Propagation Delay Time High to Low, t <sub>PHL</sub> CD4049UB	5	5	32	65	ns
	10	10	20	40	ns
	10	5	15	30	ns
	15	15	15	30	ns
	15	5	10	20	ns
Propagation Delay Time High to Low, t <sub>PHL</sub> CD4050B	5	5	55	110	ns
	10	10	22	55	ns
	10	5	50	100	ns
	15	15	15	30	ns
	15	5	50	100	ns
Transition Time, Low to High, t <sub>TLH</sub>	5	5	80	160	ns
	10	10	40	80	ns
	15	15	30	60	ns
Transition Time, High to Low, t <sub>THL</sub>	5	5	30	60	ns
	10	10	20	40	ns
	15	15	15	30	ns
Input Capacitance, C <sub>IN</sub> CD4049UB	-	-	15	22.5	pF
Input Capacitance, C <sub>IN</sub> CD4050B	-	-	5	7.5	pF



### Typical Performance Curves

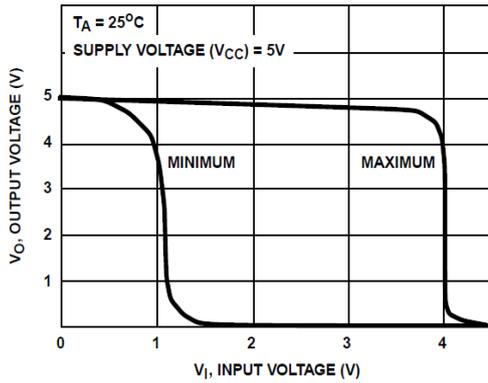


FIGURE 2. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4049UB

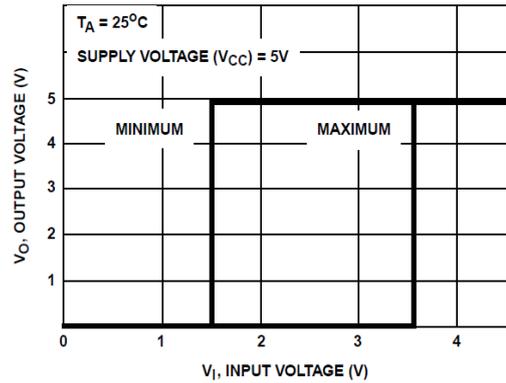


FIGURE 3. MINIMUM AND MAXIMUM VOLTAGE TRANSFER CHARACTERISTICS FOR CD4050B

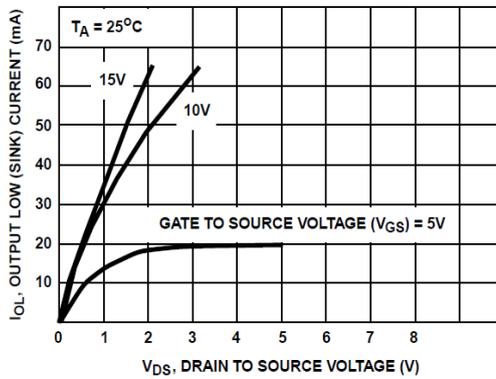


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

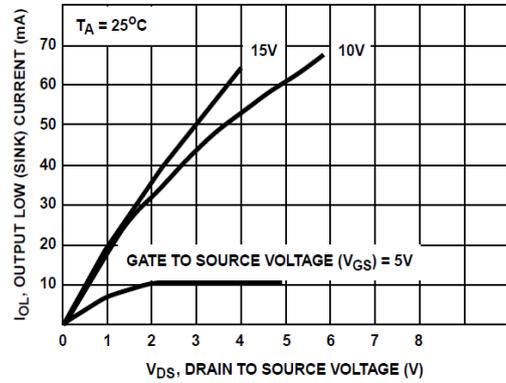


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT DRAIN CHARACTERISTICS

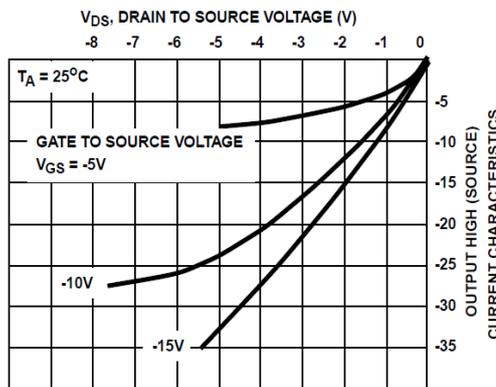


FIGURE 6. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

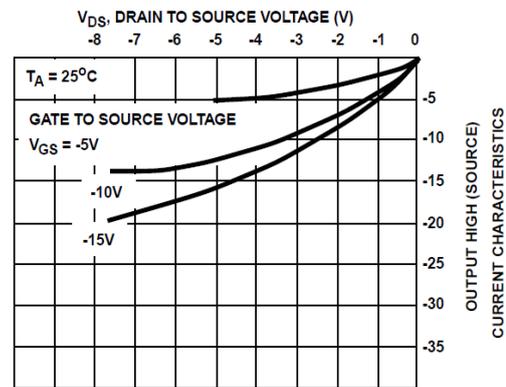


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS



**Typical Performance Curves** (Continued)

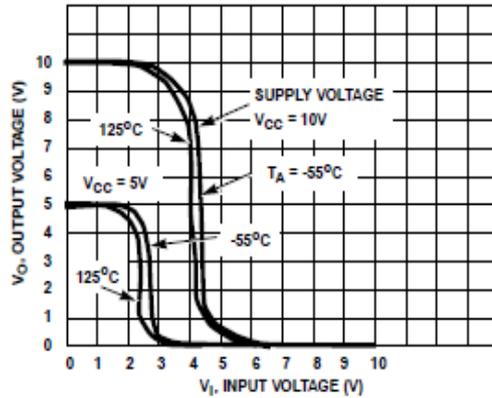


FIGURE 8. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4049UB

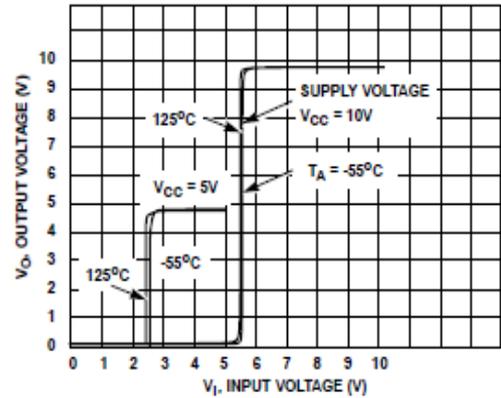


FIGURE 9. TYPICAL VOLTAGE TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE FOR CD4050B

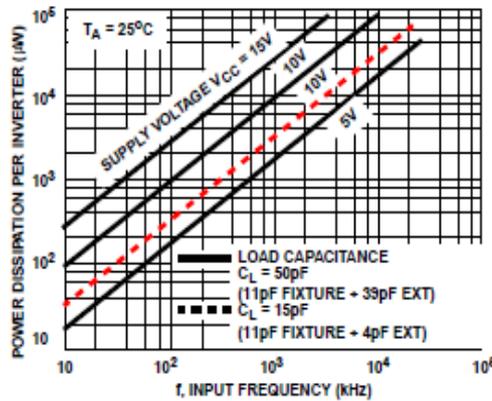


FIGURE 10. TYPICAL POWER DISSIPATION vs FREQUENCY CHARACTERISTICS

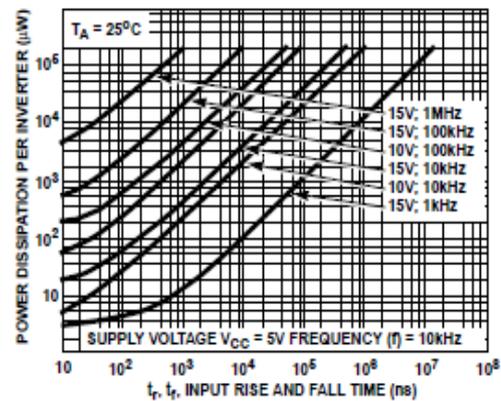


FIGURE 11. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4049UB

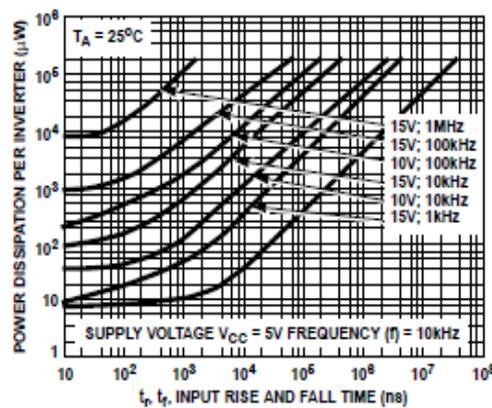


FIGURE 12. TYPICAL POWER DISSIPATION vs INPUT RISE AND FALL TIMES PER INVERTER FOR CD4050B



### Test Circuits

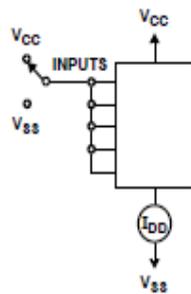
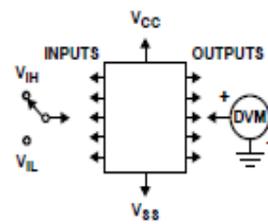
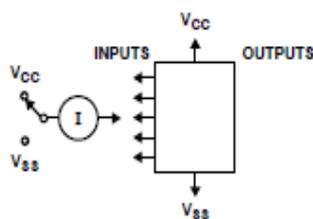


FIGURE 13. QUIESCENT DEVICE CURRENT TEST CIRCUIT

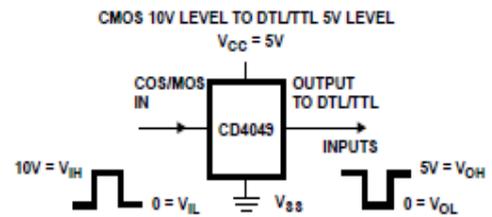


NOTE: Test any one input with other inputs at  $V_{CC}$  or  $V_{SS}$ .  
FIGURE 14. INPUT VOLTAGE TEST CIRCUIT



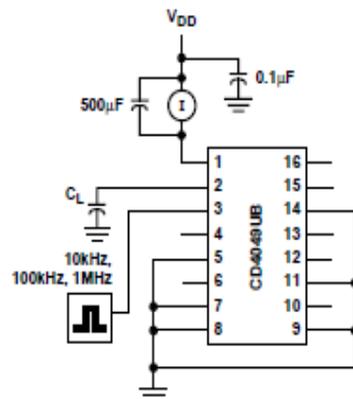
NOTE: Measure inputs sequentially, to both  $V_{CC}$  and  $V_{SS}$  connect all unused inputs to either  $V_{CC}$  or  $V_{SS}$ .

FIGURE 15. INPUT CURRENT TEST CIRCUIT



In Terminal - 3, 5, 7, 9, 11, or 14  
Out Terminal - 2, 4, 6, 10, 12 or 15  
 $V_{CC}$  Terminal - 1  
 $V_{SS}$  Terminal - 8

FIGURE 16. LOGIC LEVEL CONVERSION APPLICATION

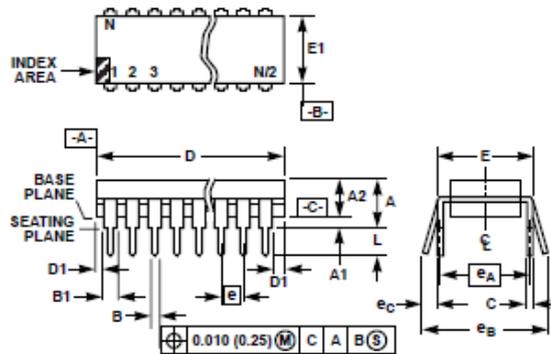


$C_L$  INCLUDES FIXTURE CAPACITANCE

FIGURE 17. DYNAMIC POWER DISSIPATION TEST CIRCUITS



### Dual-In-Line Plastic Packages (PDIP)



**NOTES:**

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and e<sub>A</sub> are measured with the leads constrained to be perpendicular to datum -C-.
- e<sub>B</sub> and e<sub>C</sub> are measured at the lead tips with the leads unconstrained. e<sub>C</sub> must be zero or greater.
- e<sub>B</sub> maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

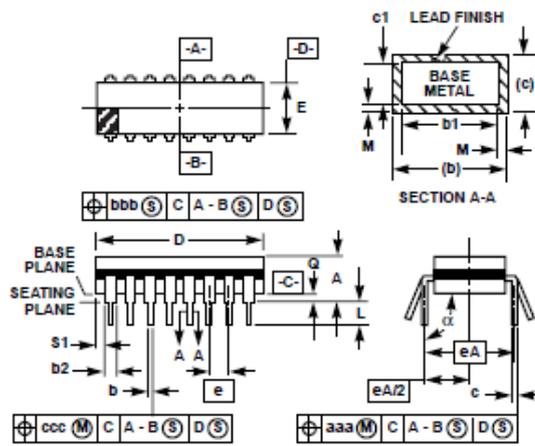
### E16.3 (JEDEC MS-001-BB ISSUE D) 16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e <sub>A</sub>	0.300 BSC		7.62 BSC		6
e <sub>B</sub>	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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### Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



**NOTES:**

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

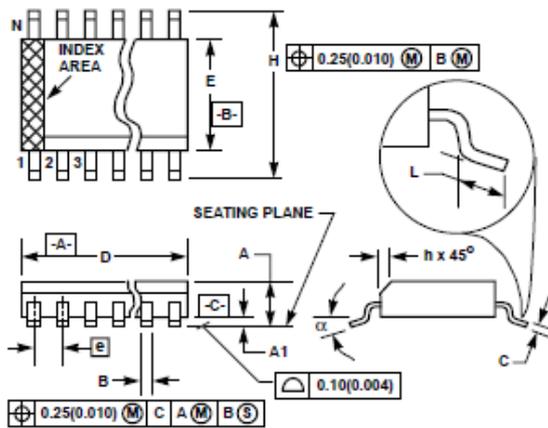
### F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A) 16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
$\alpha$	$90^\circ$	$105^\circ$	$90^\circ$	$105^\circ$	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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### Small Outline Plastic Packages (SOIC)



**NOTES:**

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.38mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

### M16.3 (JEDEC MS-013-AA ISSUE C) 16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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