Thesis Title	The CMOS Four-Quadrant Analogue Voltage Divider
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ABSTRACT

This thesis presents design method of five analogue voltage divider circuits where each circuit has been improved step by step. The first one is a basic analogue voltage divider circuit which consists of current mirror circuits and MOS transistors biased in nonsaturation region or triode region for synthesizing analogue division function. The second, in which current mirror circuits were substituted by a second generation current conveyor circuit (CCII), is developed from the first circuit. With higher frequency response, the third circuit replaces the voltage follower or buffer circuit from operational amplifier buffer to CMOS buffer. Four-Quadrant Analogue Voltage Divider Circuit, the fourth circuit composes of two Two-Quadrant Analogue Voltage Divider Circuits from the third circuit and can be operated at all quadrants. The last one utilizes a common Y second generation current conveyor circuit that can be implemented by a positive and negative current conveyor while both Y ports are commonly used. Also included less transistors. All circuits emphasize on design methods using MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) as main active elements. The CMOS-based circuits give more advantage than bipolar-based circuits in that they require less silicon chip area and more suitable for constructing in monolithic Integrated Circuit (IC).

From implementing the circuits with MC14007UB and PSpice simulation, experimental results are given to verify the theoretical analysis. The results illustrate that the circuits have wide bandwidth and good accuracy.