

Thesis Title	Design and Performance Analysis of MFSK System
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ABSTRACT

In this thesis an analysis of Minimum Frequency Shift Keying (MFSK) and implementation in digital domain are presented. Continuity of phase and modulation index of 0.5 are maintained by novel modulator structure. New modulator structure is based on Infinite Impulse Response (IIR) technique. Carrier frequency is changed directly by data bit. The presented scheme is less complicate than conventional MFSK modulator. The coherent demodulator using Fast Frequency Shift Keying (FFSK) is described. The proposed carrier recovery implementation utilizes Digital Voltage Control Oscillator (DVCO). Loop filter design using bilinear transformation from analog domain is presented. Clock synchronization, correlator, decoder and differential encoder/decoder are described in detail. The system performance is verified by MATLAB, which calculation limit to 12 bit and sampling rate of 20 times of bit rate. The proposed system gives lower $\frac{Eb}{No}$ than conventional coherent FSK receivers. At bit error rate 10^{-3} to 10^{-4} its gives $3dB$ lower. Moreover, the system responds to phase and frequency step faster than direct digital approach system. Modification for drastic doppler proplem is mentioned.