Thesis Title Low Voltage CMOS Analogue Four-Quadrant Multiplier

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ABSTRACT

This thesis proposes low voltage CMOS analogue four-quadrant multiplier. Differential active attenuators are used at input of the multiplier circuits to increase signal swing capabilities. For biasing purposes, a level shifter is needed for coupling the attenuator into the multiplier circuits. The multiplier is based on the Gilbert cell of MOS transistor operation in the triode region and in the saturation region. The proposes of CMOS analogue four-quadrant multiplier have a wide dynamic range, low voltage supply and good linearity. Simulation results from HSPICE programe are shown a Total Harmonic Distortion (THD) less than 2% and the power consumption is as low as $90\mu W$.