ALL DIFFERENTIAL-PAIR CMOS CURRENT-CONTROLLED CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (CCCDTA)

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ABSTRACT

A novel structure based on balanced differential-pair current controlled current differencing transconductance amplifier (CCCDTA) is proposed. The AMS's 0.35µm CMOS process is used to realize in CMOS technology. The performance of the structure is measured by HSPICE simulation under the ±1.5V supply voltages. The characteristics are compared to the characteristics obtained from translinear CCCDTA. The proposed CCCDTA has better characteristics such as wide-band current gain, less power consumption and wider conductance value.

1. INTRODUCTION

The current differencing transconductance amplifier (CDTA) [1] was proposed as an option to the famous current differencing buffered amplifier (CDBA) suitable to current-mode applications [1]. However, the CDTA-based circuits require external passive resistor because it has no internal resistance or transconductance. Therefore, recently, an improved version of CDTA was proposed by modeling and controlling the intrinsic parasitic resistance of CDTA's input stage via the bias current which is resulted in the current controlled current differencing transconductance amplifier (CCCDTA) [2].

The internal structure of CCCDTA is composed of two current controlled second generation current conveyors (CCCII) and operational transconductance amplifier (OTA). The translinear loop of CCCII is used to implement the input terminal because it's simple structure. However, the translinear-loop can suffers large offset voltage and poor voltage following [3, 4].

Recently, the CMOS CCCII based only on balanced differential-pair was proposed in [5], which requires less number of MOSFET than the translinear-based CCCII. In addition, its performance still serves better the operation of CCCII in applications [5]. Therefore, to provide an option in synthesizing the CCCDTA, the balanced differential-pair structure is targeted to replace the present translinear structure. It requires less number of MOSFETs which is needed low voltage and size of area is smaller. Moreover, the structure provides higher current bandwidth at the output which is an appropriate structure of CCCDTA.

2. THE PRINCIPLE OF CCCDTA

The structure of CCCDTA is quite similar to CDTA but the input resistances of CCCDTA are not zero. The resistance of CCCDTA at input ports which are R_p and R_n at p and n terminals. The parasitic resistances are equally and can be adjusted via controlled bias currents (I_{B11} and I_{B12}). The input currents are at port p and port n. The output current at port z which is conveyed from difference of the input currents causes the output current at port x which is the CCCDTA output. The R_p, R_n and g_m are intrinsic resistances and transconductance.

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \quad (1)$$

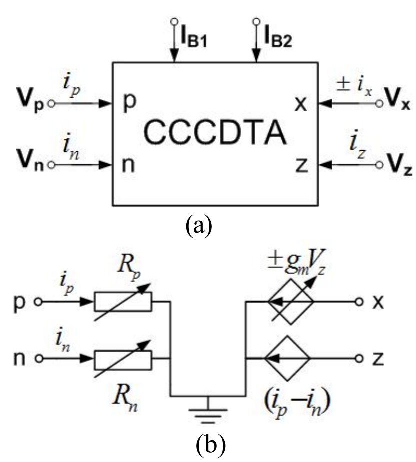

Fig. 1 CCCDTA (a) Symbol (b) Equivalent Circuit

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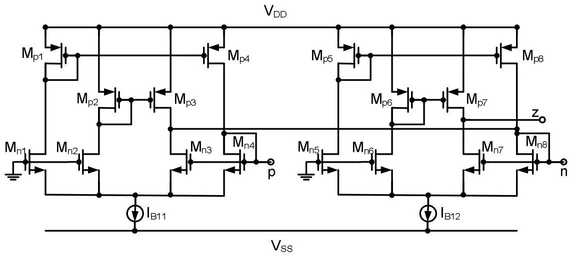

Fig. 2 Current-controlled current differencing amplifier

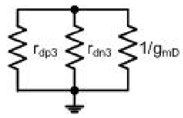

Fig. 3 Equivalent circuit of R_n

3. THE CMOS CCCDTA

3.1 Current-controlled current differencing amplifier

Fig. 2 shows the input stage of two balanced differential-pair structure. Assume identical PMOS active load and NMOS differential-pair [5].

$$g_{mp1} \cong g_{mp2} \cong g_{mp3} \cong g_{mp4} \cong g_{mM} \quad (1)$$

$$g_{mn1} \cong g_{mn2} \cong g_{mn3} \cong g_{mn4} \cong g_{mD} \quad (2)$$

$$g_{dsp1} \cong g_{dsp2} \cong g_{dsp3} \cong g_{dsp4} \cong g_{dsM} \quad (3)$$

$$g_{dsm1} \cong g_{dsm2} \cong g_{dsm3} \cong g_{dsm4} \cong g_{dsD} \quad (4)$$

The input resistance at p terminal is given by

$$R_p = \frac{1}{g_{mD}} = \frac{1}{\sqrt{I_{B11}\mu_n Cox \frac{W_D}{L_D}}}$$

(5)

The input resistance at n terminal is given by

$$R_n = \frac{1}{g_{mD}} // r_{dp3} // r_{dn3} \quad (6)$$

The output resistance at Z terminal is given by

$$R_z = \frac{1}{g_{dsD} + g_{dsM}} \quad (7)$$

3.2 Transconductance amplifier

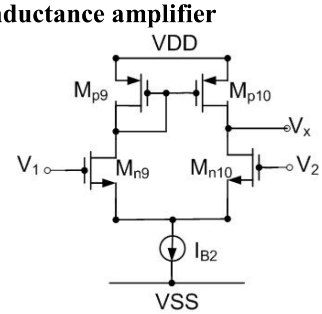

Fig. 4 Transconductance amplifier

Fig. 4 presents a simple differential pair amplifier with active load [6]. The MOSFETs M_{p9} and M_{p10} are current-mirror, the function of M_{n9} and M_{n10} is differential-pair and I_{B2} is bias current.

If $g_{mn9} \cong g_{mn10} \cong g_{mD}$ and $g_{mp9} \cong g_{mp10} \cong g_{mM}$ the relationship of I_x and V_{in} is given by

$$I_x = g_{mD} V_{in} \quad (8)$$

Where

$$V_{in} = V_1 - V_2 \quad (9)$$

And

$$g_{mD} = \sqrt{I_{B2}\mu_n Cox \frac{W_D}{L_D}} \quad (10)$$

Therefore, the transconductance is

$$g_{mD} = \frac{I_x}{V_{in}} \quad (11)$$

The output resistance at output terminal is

$$R_x = \frac{1}{g_{mD} + g_{mM}} \quad (12)$$

3.3 Novel current-controlled current differencing transconductance amplifier

The novel CMOS CCCDTA consists of two balanced differential-pair CCCII+ and one operational transconductance amplifier (OTA) that shown in Fig 5. Following the CDTA – Building block [1] the function of two balanced differential-pair CCCII+ are input state and operational transconductance amplifier is output state. The function of first balanced differential-pair CCCII+ is as input terminal p and output of the first one is connected to input state of the second CCCII+ at terminal n. The output of the second one is input of OTA. The MOSFETs M_{p1}-M_{p8} and M_{n1}-M_{n8} are constructed as the CCCD amplifier and MOSFETs M_{p9}-M_{p10} and M_{n9}-M_{n10} are constructed as operational transconductance amplifier.

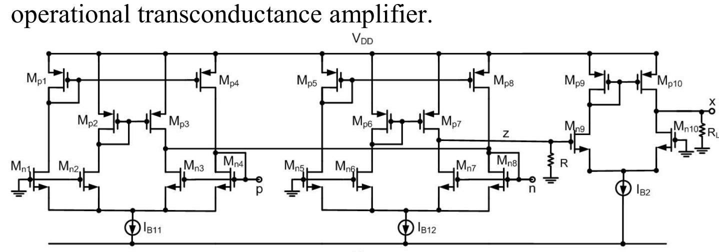

Fig. 5 Proposed Current-controlled current differencing transconductance amplifier

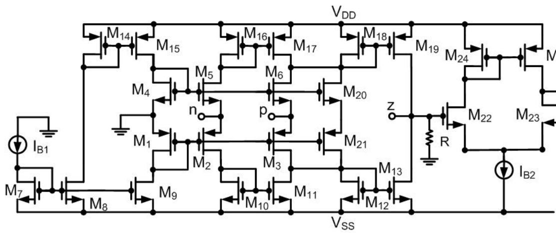

Fig. 6 Original Current-controlled current differencing transconductance amplifier

4. SIMULATION RESULT

To observe the performance of CCCDTA, the element was simulated with HSPICE simulation program under ±1.5 supply voltages base on the AMS's 0.35µm CMOS model. The Fig. 6 is the original CCCDTA that is compared with the proposed CCCDTA. The channel length of the proposed CCCDTA and the original CCCDTA are 0.7µm and aspect ratios of CMOS are listed in Table I.

TABLE I
DIMENSION OF MOS TRANSISTORS

CMOS Transistor	W(µm)/L(µm)
Proposed CCCDTA	
Mp1-Mp10	20
Mn1-Mn10	30
Original CCCDTA	
Mp1-Mp3,Mp21	30
Mn4-Mn6,Mn20	9.29
Mn7-Mn9	28.57
Mn10-Mn13	20
Mp14-Mp19	51.4
Mp22-Mp23	20
Mp24-Mp25	30

Fig. 7 presents the comparison of the parasitic resistance at p and n input terminals between the proposed CCCDTA and the original CCCDTA when I_{B1} is vary. The I_{B1} current is adjusted for controlling the parasitic resistances. The bias current that is more than 300µA will difficult to control the input parasitic resistances. Fig. 8 presents the comparison of DC transfer characteristics between the proposed CCCDTA and the original CCCDTA when I_{B1} = -25, -10, 0, 10 and 25µA. The linearity of DC transfer characteristics is limited by I_{B1}. The transconductance values are compared between the proposed CCCDTA and the original CCCDTA when I_{B2} is vary from 0 to 600 µA and maximum transconductance is at 1mA in Fig. 9. Fig. 10 presents the comparison of the -3dB bandwidth of the current gains between the proposed CCCDTA and the original CCCDTA, the proposed are I_z/I_n, I_z/I_p, I_x/I_n and I_x/I_p, located at 155.51 MHz, 228.82 MHz, 323.31 MHz and 320.89 MHz, when I_{B1} = 50µA, I_{B2} = 100µA. The original are I_z/I_n, Iz/I_p, I_x/I_n and I_x/I_p, located at 282 MHz, 311 MHz, 50 MHz and 142 MHz, when I_{B1} = 50µA, I_{B2} = 100µA. Fig. 11 presents the frequency response of g_m. Fig 12 presents loading effects at z and x terminals. From the Table II, the values of R_z and R_x of the proposed structure are 307.52kΩ and 302.71kΩ, respectively. The original CCCDTA has the values 190kΩ and 301.43kΩ for R_z and R_x, respectively. The frequency response simulations I_z/I_p, I_z/I_n, I_x/I_p and I_x/I_n of the proposed CCCDTA can be used with values of R and R_L lie between 10Ω and 1kΩ. Therefore, the proposed element works well when $R_z \geq 300R$ and $R_x \geq 300R_L$. From the simulations of the original structure, the values of R and R_L lie between 10Ω and 1kΩ. So, it works well when $R_z \geq 200R$ and $R_x \geq 300R_L$ [7].

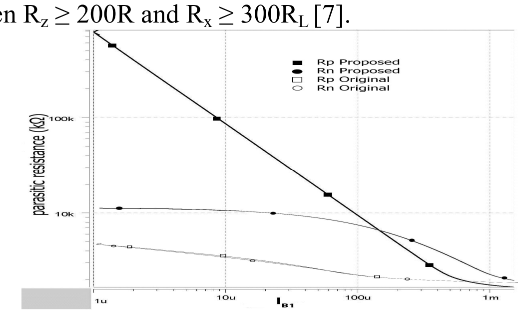

Fig. 7 Parasitic resistances at input terminals

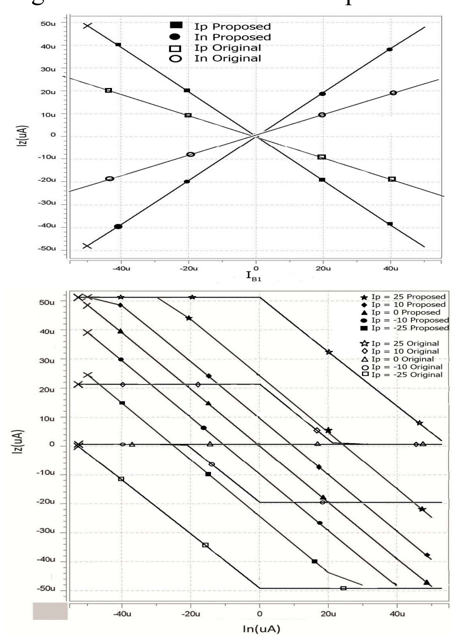

Fig. 8 DC transfer characteristic of the CCCDTA

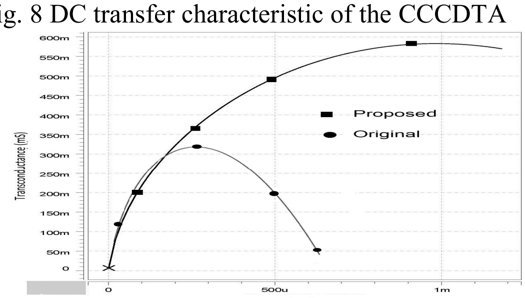

Fig. 9 Transconductance value relative to I_{B2}

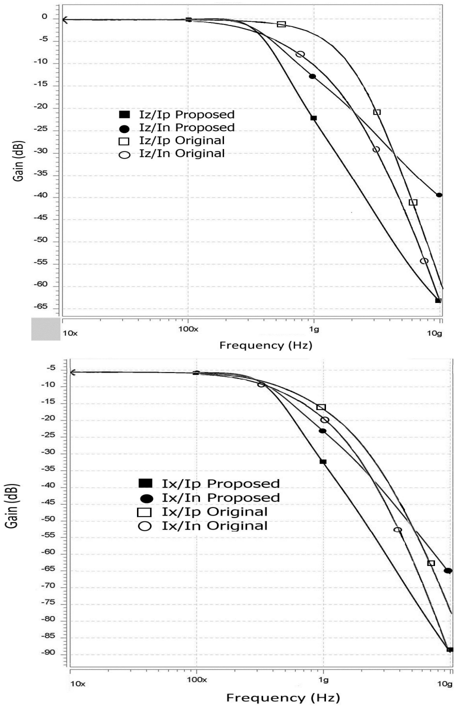

Fig. 10 Frequency responses at output

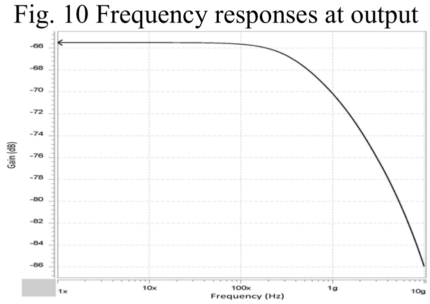

Fig. 11 Frequency responses of g_m

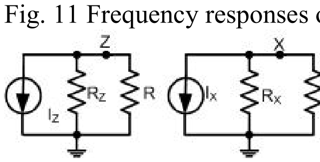

Fig. 12 Loading effects at z and x terminals

5. CONCLUSION

The differential-pair CMOS CCCDTA is proposed in this paper. The AMS's 0.35µm CMOS process is used for simulation by HSPICE. The result provides wide-band of current gain, less require MOSFETs is needed, the bias current is very low, lower power consumption, and wider controlled- transconductance value when compare with the translinear CMOS CCCDTA.

TABLE II

CONCLUSION OF CCCDTA PARAMETERS

Parameters	Proposed	Original
Power supply voltages	±1.5 V	±1.5 V
Power consumption	900 µW	1.48mW
-3dB Bandwidth	387.51 MHz (Iz/In)	453 MHz (Iz/In)
	358.82 MHz (Iz/Ip)	947MHz (Iz/Ip)
	323.31 MHz (Ix/In)	350MHz (Ix/In)
	320.89 MHz (Ix/Ip)	372MHz (Ix/Ip)
Input bias current range for controlling transconductance	1µA – 0.981mA	1nA – 100uA
Transconductance	6.68mS – 0.583S	0.25mS -1mS
Input bias current range for controlling Rn and Rp	1uA - 1.5mA	1uA -1.5mA
Rn	5.62kΩ - 1.33kΩ	1.83kΩ - 1.37kΩ
Rp	776kΩ - 1.76kΩ	1.83kΩ - 1.30kΩ
Rz	307.52kΩ	190kΩ
Rx	302.71kΩ	301.43kΩ

11. REFERENCE

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