ALL DIFFERENTIAL-PAIR CMOS CURRENT-CONTROLLED CURRENT DIFFERENCING TRANSCONDUCTANCE AMPLIFIER (CCCDTA)

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A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF MASTER OF ENGINEERING (COMPUTER ENGINEERING)
FACULTY OF ENGINEERING
KING MONGKUT'S UNIVERSITY OF TECHNOLOGY THONBURI
2013

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A Thesis Submitted in Partial Fulfillment of the Requirements for
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Thesis Title	All Differential-Pair CMOS Current-Controlled Current Differencing Transconductance Amplifier (CCCDTA)
Thesis Credits	12
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Program	Master of Engineering
Field of Study	Computer Engineering
Department	Computer Engineering
Faculty	Engineering
Academic Year	2013

Abstract

A novel structure based on balanced differential-pair current controlled current differencing transconductance amplifier (CCCDTA) is proposed. The AMS’s 0.35μm CMOS process is used to realize in CMOS technology. The performance of the structure is measured by HSPICE simulation under the ±1.5V supply voltages. The characteristics are compared to the characteristics obtained from translinear CCCDTA. The proposed CCCDTA has better characteristics such as wide-band current gain, less power consumption and wider conductance value.

Keywords : Balanced differential-pair/ CCCDTA

หัวข้อวิทยานิพนธ์	วงจรขยายผลต่างกระแสส่งผ่านความนำที่ควบคุมด้วยกระแสโดยใช้วงจรคู่ต่างกระแสแบบ CMOS ทั้งหมด (CCCDTA)
หน่วยกิต	12
ผู้เขียน	นายเอกรัฐ กาญจนากระจ่าง
อาจารย์ที่ปรึกษา	รศ. ดร. บุญเจริญ ศิริเนาวกุล รศ. บุญรักษ์ จิปิภพ
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ปีการศึกษา	2556

บทคัดย่อ

วงจรรูปแบบใหม่ที่นำเสนอมีพื้นฐานมาจาก วงจรขยายผลต่างกระแสส่งผ่านความนำที่ควบคุมด้วยกระแสโดยใช้ วงจรคู่ต่างกระแสแบบ CMOS ในการออกแบบวงจรในที่นี้ได้ใช้เทคโนโลยี CMOS ทั้งหมด (CCCDTA) แบบ AMS’s 0.35 μm ซึ่งเป็นเทคโนโลยีของ CMOS ที่เลือกใช้ในการทดสอบและการทดสอบวงจรได้ใช้โปรแกรม HSPICE เพื่อทดสอบสมรรถนะของวงจร ภายใต้แรงดัน ±1.5 V คุณสมบัติของวงจรที่ออกแบบใหม่จะถูกนำมาเปรียบเทียบกับวงจรแบบดั้งเดิมที่ใช้เทคโนโลยี Translinear ของวงจรขยายผลต่างกระแสส่งผ่านความนำที่ควบคุมด้วยกระแส ผลการทดสอบกับวงจรที่นำเสนอของวงจรขยายผลต่างกระแสส่งผ่านความนำที่ควบคุมด้วยกระแสทั้งหมดโดยใช้ วงจรคู่ต่างกระแสจะได้คุณสมบัติที่ดีกว่าเกี่ยวกับ รองรับการตอบสนองความถี่ของการขยายกระแสที่กว้างขึ้น มีความต้องการในการใช้พลังงานน้อยกว่า และ มีค่าความนำที่กว้างกว่า

คำสำคัญ : วงจรคู่ต่างกระแส/วงจรขยายผลต่างกระแสส่งผ่านความนำที่ควบคุมด้วยกระแสทั้งหมด (CCCDTA)

ACKNOWLEDGEMENTS

I couldn’t complete this thesis without the help of my advisor, Assoc. Prof. Dr. Booncharoen Sirinaovakul and Assoc. Prof. Boonruk Chipipop, who had shared his time to advise me. They had opened many courses to teach about this thesis, they also gave useful comments, revision, and sincere support. Their great experiences for designing the structure is very grateful. I herewith would like to thank them very much. Lastly, I would like to thank my family for encouraging me and their love.

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LIST OF SYMBOLS

SYMBOL		UNIT
I_n	current input at n	A
I_p	current input at p	A
I_x	current output at x	A
I_z	current output at z	A
L	gate length	µm
M_n	N-MOS	
M_p	P-MOS	
R	Resistor	Ω
R_L	loaded resistor	Ω
R_n	Resistance at n	Ω
R_p	Resistance at p	Ω
R_x	Resistance at x	Ω
R_z	Resistance at z	Ω
V_n	voltage at n	V
V_p	voltage at p	V
V_x	voltage at x	V
V_z	voltageat z	V
V_{DD}	positive supply voltage	V
V_{SS}	negative supply voltage	V
W	gate width	µm

LIST OF TECHNICAL VOCABULARY AND ABBREVIATIONS

CMOS = Complementary MOS
dB = Decibel
Hz = Hertz
MHz = Megahertz
GHz = Gigahertz
MOSFET = Metal-Oxide-Semiconductor Field-Effect Transistors
NMOS = N-channel MOSFET
PMOS = P-channel MOSFET
V = Volt
W = Watt
A = Ampere
s = second
m = meter or milli
Ω = Ohm
μ = micro
μm = micron

CHAPTER 1 INTRODUCTION

1.1 Motivation

The current differencing transconductance amplifier (CDTA) [1] was proposed as an option to the famous current differencing buffered amplifier (CDBA) suitable to current-mode applications [1]. However, the CDTA-based circuits require external passive resistor because it has no internal resistance or transconductance. Therefore, recently, an improved version of CDTA was proposed by modeling and controlling the intrinsic parasitic resistance of CDTA input stage via the bias current which is resulted in the current-controlled current differencing transconductance amplifier (CCCDTA) [2]

The internal structure of CCCDTA is composed of two current-controlled second generation current conveyors (CCCII) connected as current-controlled current differencing amplifier (CCCDA) and operational transconductance amplifier (OTA) in Figure 1.1. The translinear loop of CCCII is used to implement the input terminal because of its simple structure. However, the translinear-loop can suffer large offset voltage and poor voltage as in [3, 4].

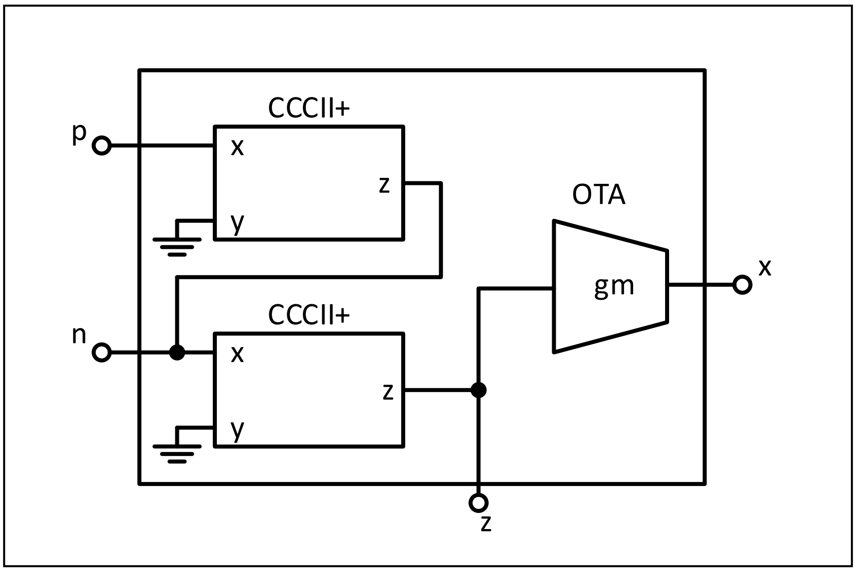


Figure 1.1 Building block of CCCDTA

1.2 Research Objective

To improve the performance of CCCDTA and to reduce the number of MOSFETs. We propose the new CCCDTA. The expected result are the wide-band current gain, less power consumption and wider conductance value.

1.3 General Approach

Recently, the CMOS CCCII based on balanced differential-pair was proposed in [5]. It requires less number of MOSFET than the translinear-based CCCII. In addition, its performance still serves better than the performance of translinear CCCII in applications [5]. Therefore, to provide an option in synthesizing the CCCDTA, the balanced differential-pair structure is targeted to replace the present translinear structure. It requires less number of MOSFETs which is needed low voltage and smaller size of area. Moreover, the structure provides higher current gain bandwidth at the output which is a target of the proposed structure of CCCDTA.

1.4 Scopes of the Thesis

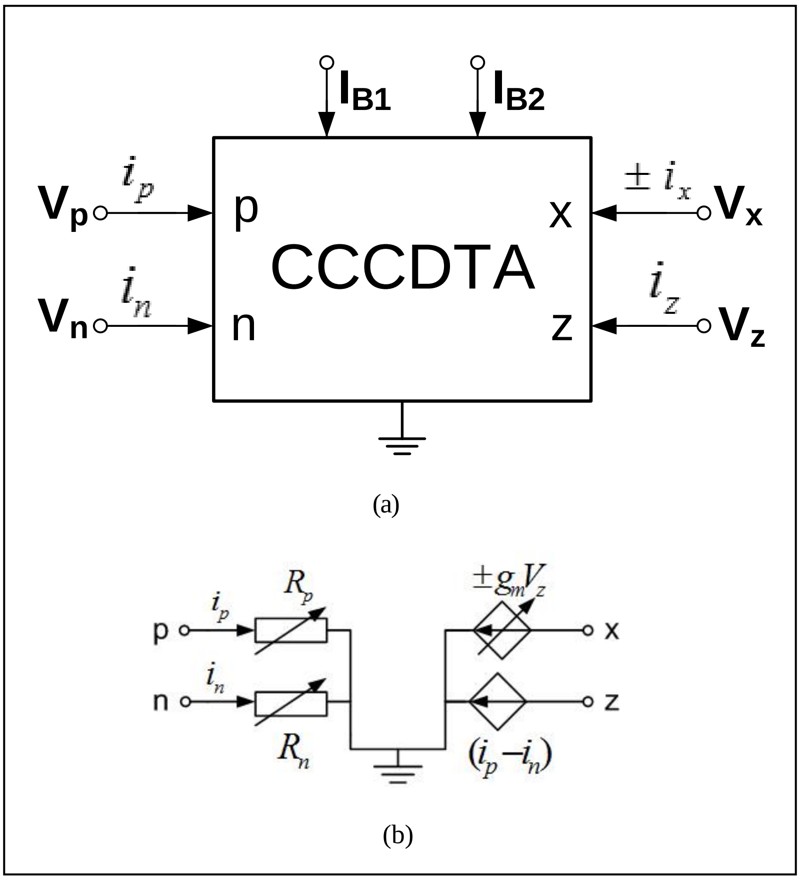
1. Study the original CCCDTA.
2. Consider the balance differential-pair structure which offers better performance than translinear structure.
3. Propose the CCCDTA structure that uses balance differential-pair structure.
4. Simulate the performance of both original and proposed structure of CCCDTA.

CHAPTER 2 THEORETICAL ISSUE AND RELATED WORK

2.1 The Principle of CCCDTA

The structure of CCCDTA is quite similar to CDTA but the input resistances of CCCDTA are not zero. The resistance of CCCDTA at input ports which are R_p and R_n at p and n terminals, respectively. The parasitic resistances are equally and can be adjusted via controlled bias current (I_{B1}). The input currents are at port p and port n. The output current is at port z which is conveyed from difference of the input current that causes the output current at port x which is also the CCCDTA output. The R_p, R_n and g_m are intrinsic resistances and transconductance, respectively.

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} R_p & 0 & 0 & 0 \\ 0 & R_n & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix} \tag{2.1}$$



(a)

(b)

Figure 2.1 CCCDTA (a) Symbol (b) Equivalent circuit

2.2 The CMOS Translinear CCCDTA

The original current-controlled current differencing transconductance amplifier is shown in Figure 2.2. The circuit implementation consists of mixed translinear loops (M_1–M_6). The mixed loops are DC biased by I_{B1} using current mirrors (M_7–M_{10} and M_{14}–M_{16}). The output z-terminal that generates the current difference of p and n terminals is realized using transistors (M_{11}–M_{13} and M_{17}–M_{21}). [2]

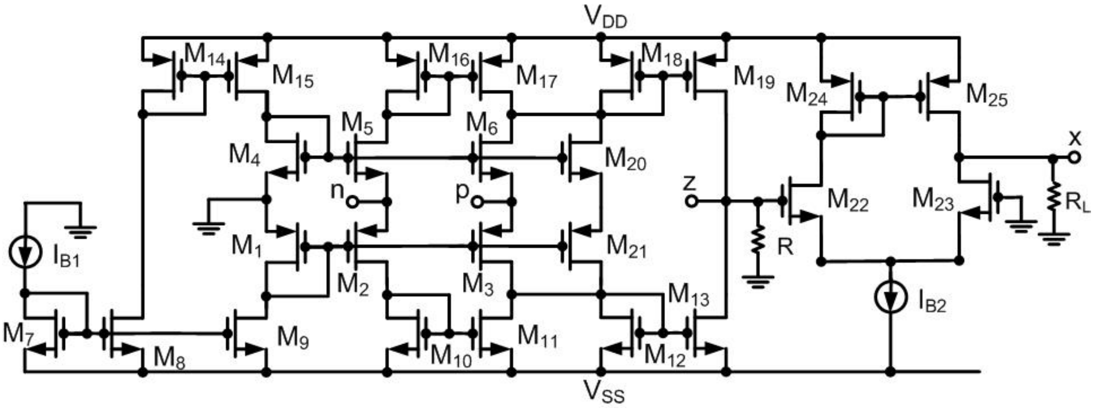


Figure 2.2 Original Current-Controlled Current Differencing Transconductance Amplifier

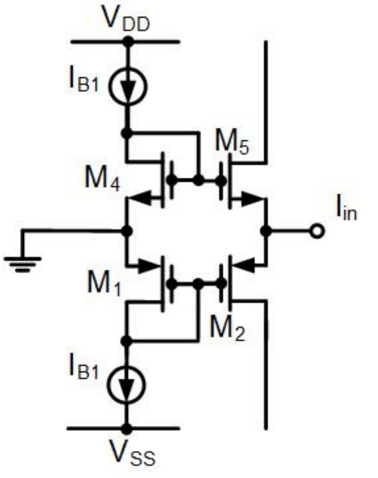


Figure 2.3 Translinear loop

Figure 2.3. displays a class AB translinear loop, which is used as input section. By straightforward analysis. If $g_{m1} = g_{m4}$ and $g_{m2} = g_{m5} = g_m$, we will obtain the parasitic resistance at input terminal as [2]

$$R_p = R_n = \frac{1}{2g_{mi}} = \frac{1}{\sqrt{8I_{B1}\mu_n Cox\frac{W_D}{L_D}}} \tag{2.2}$$

$$g_{mi} = \sqrt{2I_{B1}\mu_n Cox\frac{W_D}{L_D}} \tag{2.3}$$

If transistors are matched, which means that

$$g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5} = g_{m6} = g_{m20} = g_{m21} \tag{2.4}$$

$$g_{m10} = g_{m11} = g_{m12} = g_{m13} \tag{2.5}$$

$$g_{m16} = g_{m17} \tag{2.6}$$

$$g_{m18} = g_{m19} \tag{2.7}$$

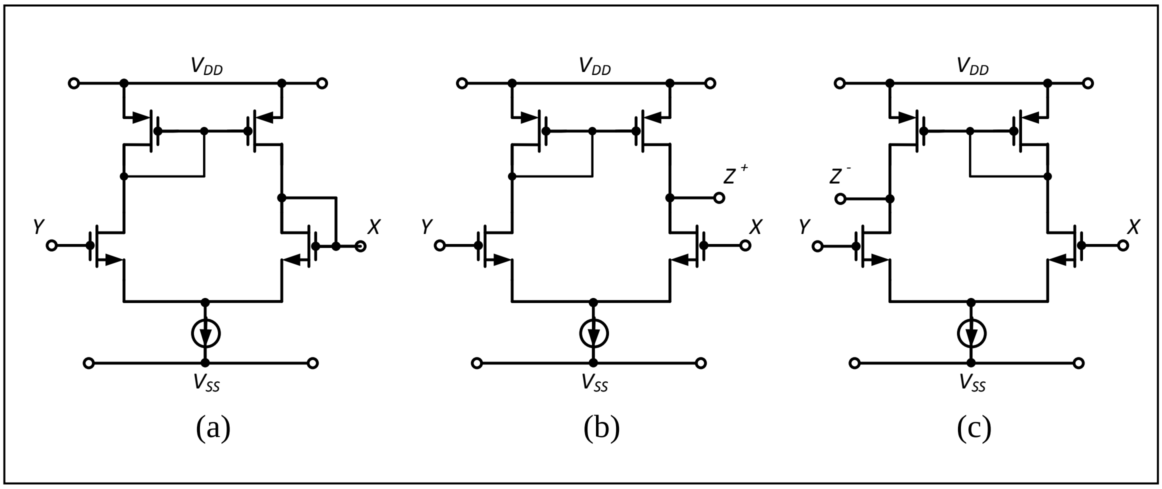
The current at z terminal can be expressed as

$$I_Z = I_p - I_n \tag{2.8}$$

The output resistance looking into the z terminal (R_Z) can be, respectively, expressed as

$$R_Z \cong \frac{r_{o13} r_{o19}}{r_{o13} + r_{o19}} \tag{2.9}$$

2.3 The CMOS Balanced Differential-Pair CCCII



(a) (b) (c)

Figure 2.4 Balanced Differential-Pair CCCII (a) Input pair (b) Z^+ pair (c) Z^- pair

The structure of balanced differential-pair CCCII shown in Figure 2.4. is based on various types of active-loaded differential-pair, which are configured as input and output stages. To compose a CCCII of any output requirements, the selected components are just to be piled up sharing the same input ports (X and Y). The input pair is almost the same as the Z^+ pair except the presence of feedback connection which is not included in the Z^+ pair. To alter the direction of the output current, the Z^- pair is simply the mirrored version of the Z^+ pair. [5]

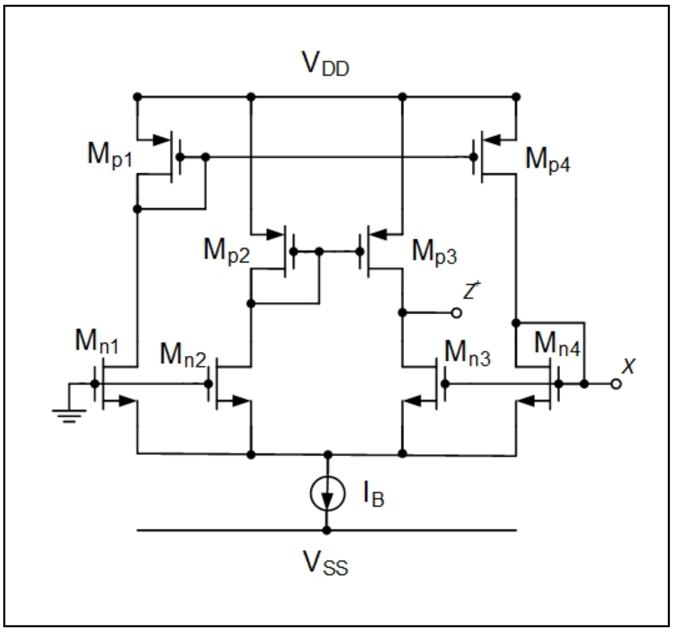


Figure 2.5 Balanced Differential-Pair CCCII

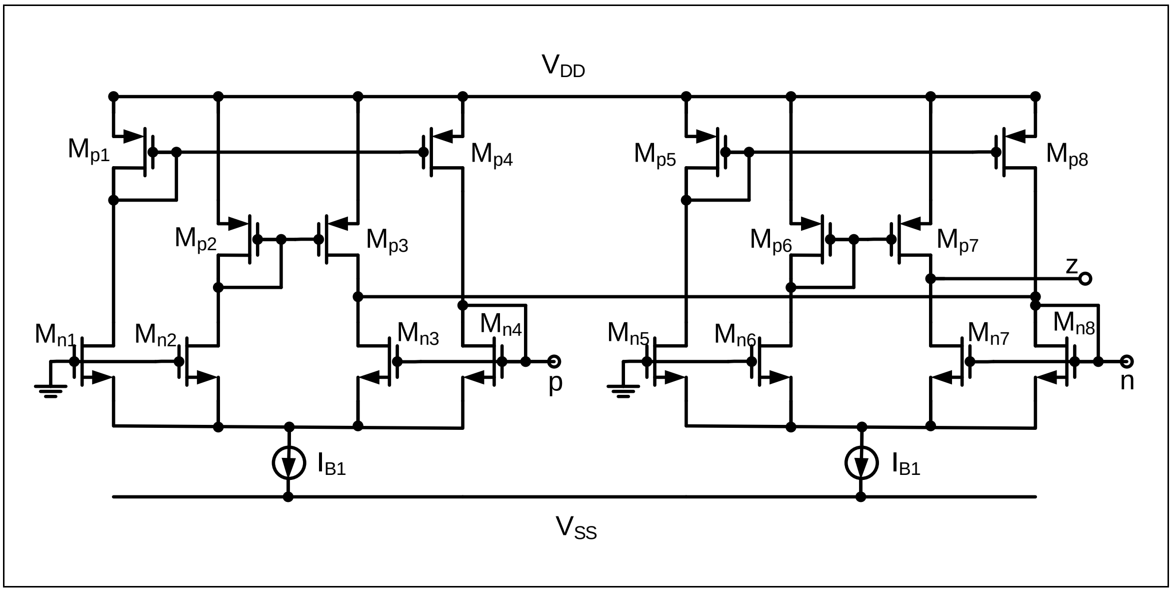


Figure 2.6 Proposed Current-Controlled Current Differencing Amplifier (CCCDA)

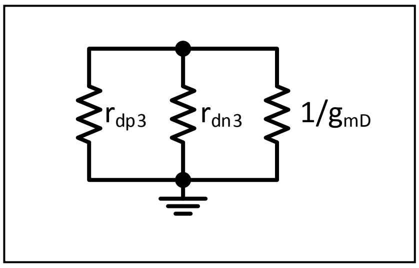


Figure 2.7 Equivalent circuit of R_n

Figure 2.6. shows the input of proposed current-controlled current differencing transconductance amplifier (CCCDA). It consists of input at n terminal, input at p terminal and output at z terminal. Assume that identical PMOS active load and NMOS differential-pair [5] :

$$g_{mp1} \cong g_{mp2} \cong g_{mp3} \cong g_{mp4} \cong g_{mM} \tag{2.10}$$

$$g_{mn1} \cong g_{mn2} \cong g_{mn3} \cong g_{mn4} \cong g_{mD} \tag{2.11}$$

$$g_{dsp1} \cong g_{dsp2} \cong g_{dsp3} \cong g_{dsp4} \cong g_{dsM} \tag{2.12}$$

$$g_{dsm1} \cong g_{dsm2} \cong g_{dsm3} \cong g_{dsm4} \cong g_{dsD} \tag{2.13}$$

The input resistance at p terminal is given by

$$R_p = \frac{1}{g_{mD}} = \frac{1}{\sqrt{2I_{B1}\mu_n Cox \frac{W_D}{L_D}}} \tag{2.14}$$

The input resistance at n terminal is given by

$$R_n = \frac{1}{g_{mD}} // r_{dp3} // r_{dn3} \tag{2.15}$$

g_{mD} depends on I_{B1}

The output resistance at Z terminal is given by

$$R_z = \frac{1}{g_{dsn_7} + g_{dsp_7}} \tag{2.16}$$

The current at z terminal is given by

$$I_z = I_p - I_n \tag{2.17}$$

2.4 Transconductance Amplifier

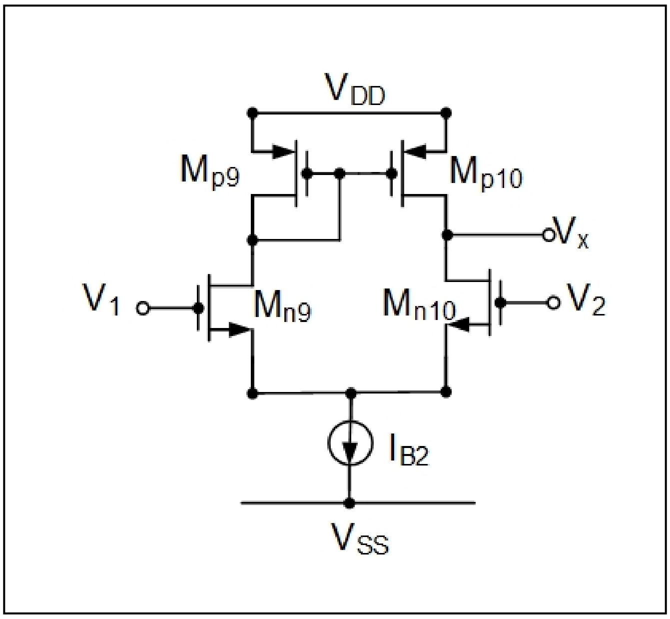


Figure 2.8 Transconductance Amplifier

Figure 2.8. presents a simple differential pair amplifier with active load [6]. The MOSFETs M_{p9} and M_{p10} are current-mirror, the function of M_{n9} and M_{n10} is differential-pair and I_{B2} is bias current.

If $g_{mn9} \cong g_{mn10} \cong g_{mDx}$ and $g_{mp9} \cong g_{mp10} \cong g_{mMx}$ the relationship of I_x and V_{in} is given by

$$I_x = g_{mDx} V_{in} \tag{2.18}$$

Where $$V_{in} = V_1 - V_2 \tag{2.19}$$

If $$V_2 = 0, I_x \cong g_m V_1 \tag{2.20}$$

And

$$g_m = g_{mDx} = \sqrt{2 I_{B2} \mu_n Cox \frac{W_{D_3}}{L_{D_3}}} \tag{2.21}$$

Therefore, the transconductance is

$$g_{mDx} = \frac{I_x}{V_{in}} \tag{2.22}$$

The output resistance at output terminal is

$$R_x = \frac{1}{g_{mDx} + g_{mMx}} \tag{2.23}$$

CHAPTER 3 PROPOSED CMOS CCCDTA

3.1 Novel CMOS Current-Controlled Current Differencing Transconductance Amplifier

The novel CMOS CCCDTA consists of two balanced differential-pair CCCII+ connected as current-controlled current differencing amplifier (CCCDA) and one operational transconductance amplifier (OTA) that is shown in Figure 3.1. Following the CDTA – Building block [1] the function of CCCDA is an input state connected with OTA as an output state. The resistor R is the load of the CCCDA that changes differencing current I_Z to be voltage V_Z for input of the OTA. The load resistance R_L changes output current Ix to be output voltage V_X.

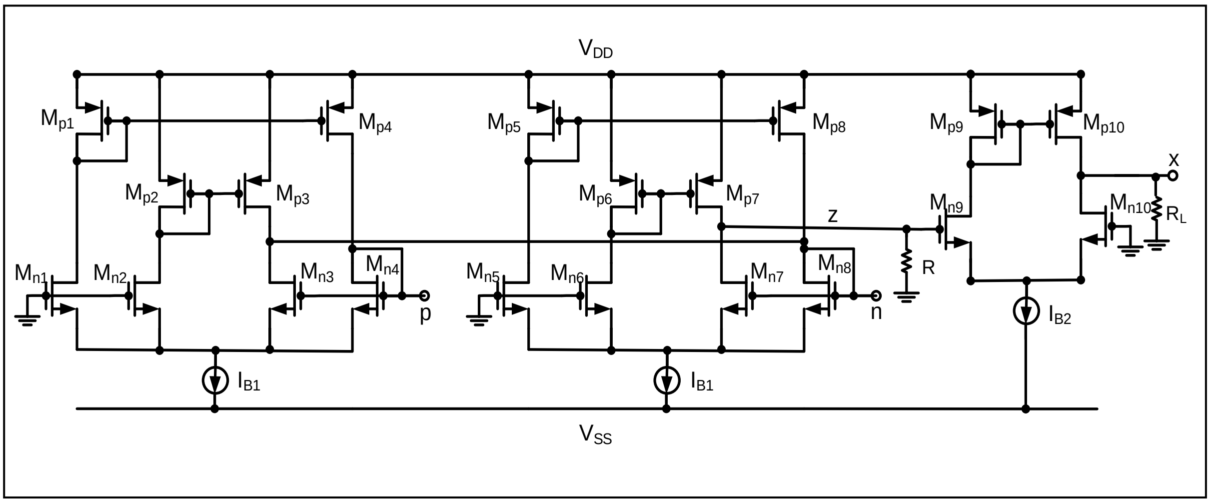


Figure 3.1 Proposed Current-Controlled Current Differencing Transconductance Amplifier

CHAPTER 4 RESULTS

4.1 Simulation Result

To observe the performance of CCCDTA, the element was simulated with HSPICE simulation program under ±1.5 supply voltages based on the AMS's 0.35µm CMOS model. Figure 2.2. is the original CCCDTA that is compared with the proposed CCCDTA in Figure 3.1. The channel length of the proposed CCCDTA and the original CCCDTA are 0.7µm and aspect ratios of CMOS are listed in Table 4.1.

Table 4.1 Dimension of MOS transistors

CMOS Transistor	**W(µm)/L(µm)**
Proposed CCCDTA	
M_{p1}-M_{p10}	20
M_{n1}-M_{n10}	30
Original CCCDTA	
M_{p1}-M_{p3},M_{p21}	30
M_{n4}-M_{n6},M_{n20}	9.29
M_{n7}-M_{n9}	28.57
M_{n10}-M_{n13}	20
M_{p14}-M_{p19}	51.4
M_{p22}-M_{p23}	20
M_{p24}-M_{p25}	30

Figure 4.1. presents the comparison of the parasitic resistance at p and n input terminals between the proposed CCCDTA and the original CCCDTA when I_{B1} is varied. The I_{B1} current is adjusted for controlling the parasitic resistances. The bias current that is more than 300µA will be difficult to control the input parasitic resistances of the original CCCDTA. But for the proposed CCCDTA, the bias current is better controlled to the maximum of 1 mA.

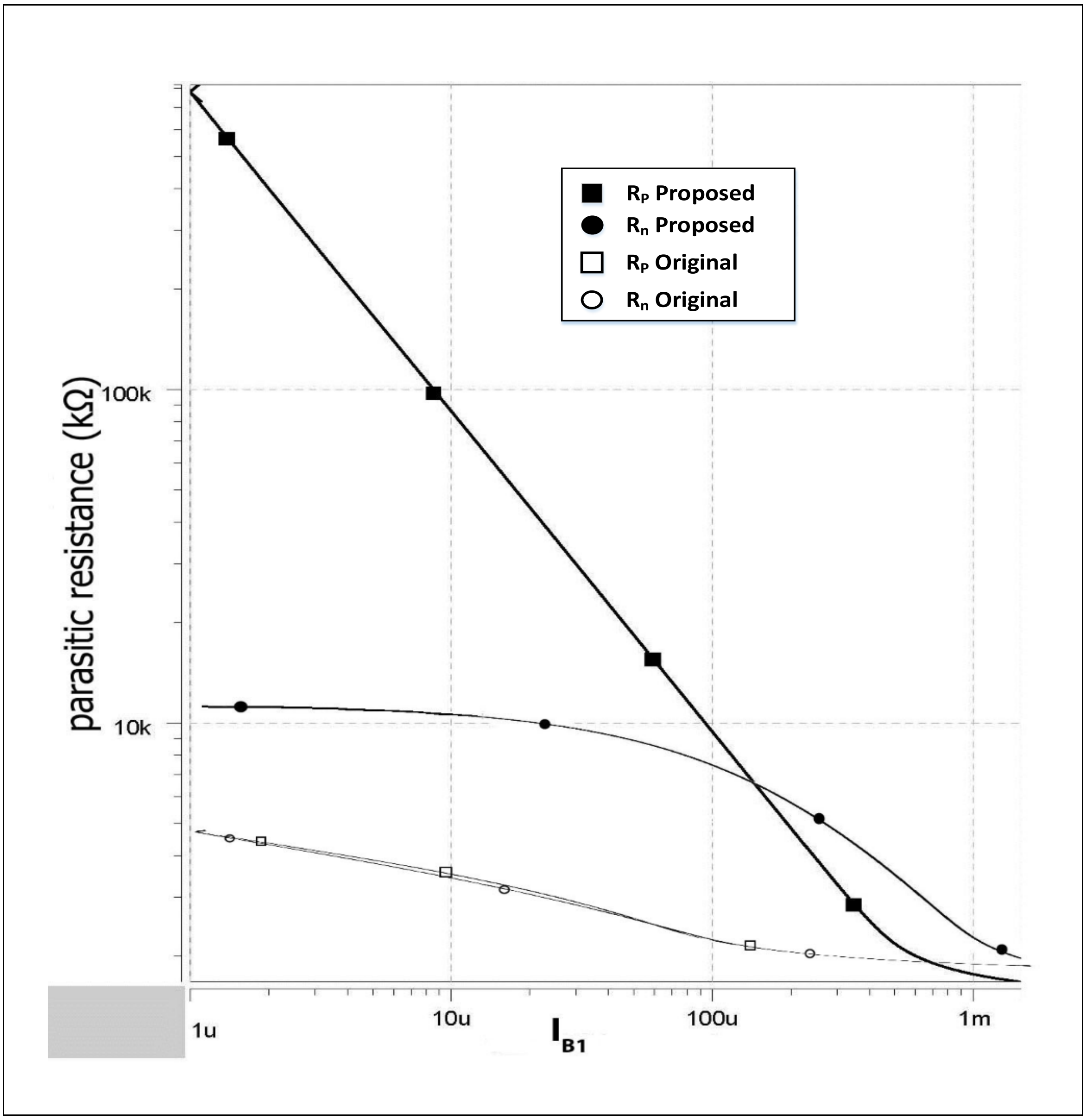


Figure 4.1 Parasitic resistances at input terminals

Figure 4.2. presents the comparison of DC transfer characteristics between the proposed CCCDTA and the original CCCDTA when I_{B1} = -25, -10, 0, 10 and 25µA. The linearity of DC transfer characteristics is limited by I_{B1}.

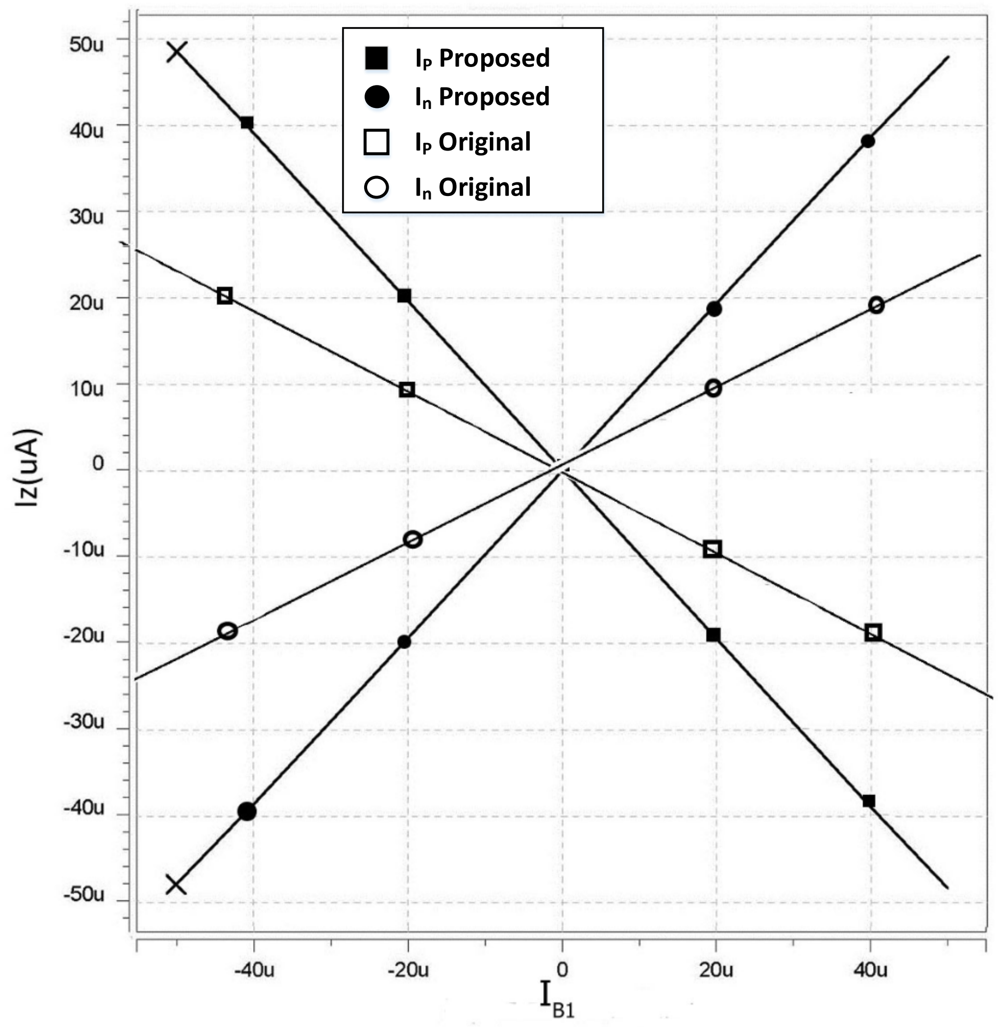


Figure 4.2 DC transfer characteristic of the CCCDTA

The transconductance values are compared between the proposed CCCDTA and the original CCCDTA when I_{B2} is varied from 0 to 600 µA and maximum transconductance is at 1 mA in Figure 4.3.

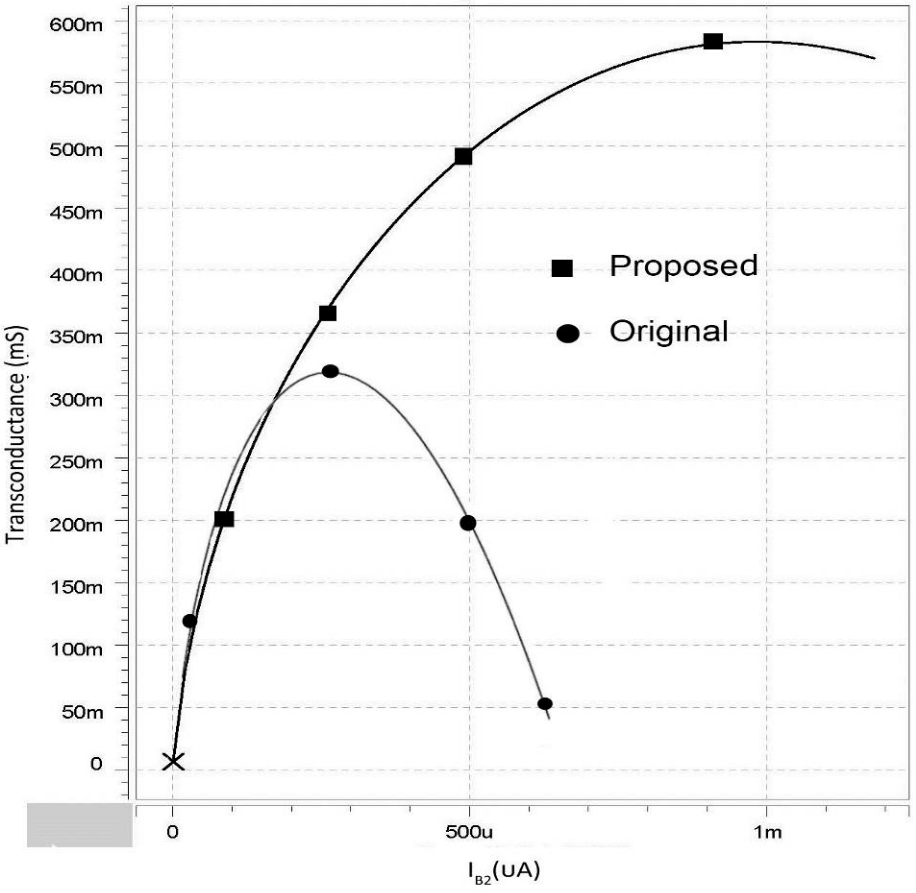


Figure 4.3 Transconductance value relative to I_{B2}

Figure 4.4. presents the comparison of the -3dB bandwidth of the current gained between the proposed CCCDTA and the original CCCDTA. The proposed are I_z/I_n, I_z/I_p, I_x/I_n and I_x/I_p, located at 453 MHz, 947 MHz, 350 MHz and 372 MHz, when $I_{B1} = 50\mu A$, $I_{B2} = 100\mu A$. The original are I_z/I_n, Iz/Ip, I_x/I_n and I_x/I_p, located at 387.51 MHz, 358.82 MHz, 323.31 MHz and 320.89 MHz, when $I_{B1} = 50\mu A$, $I_{B2} = 100\mu A$.

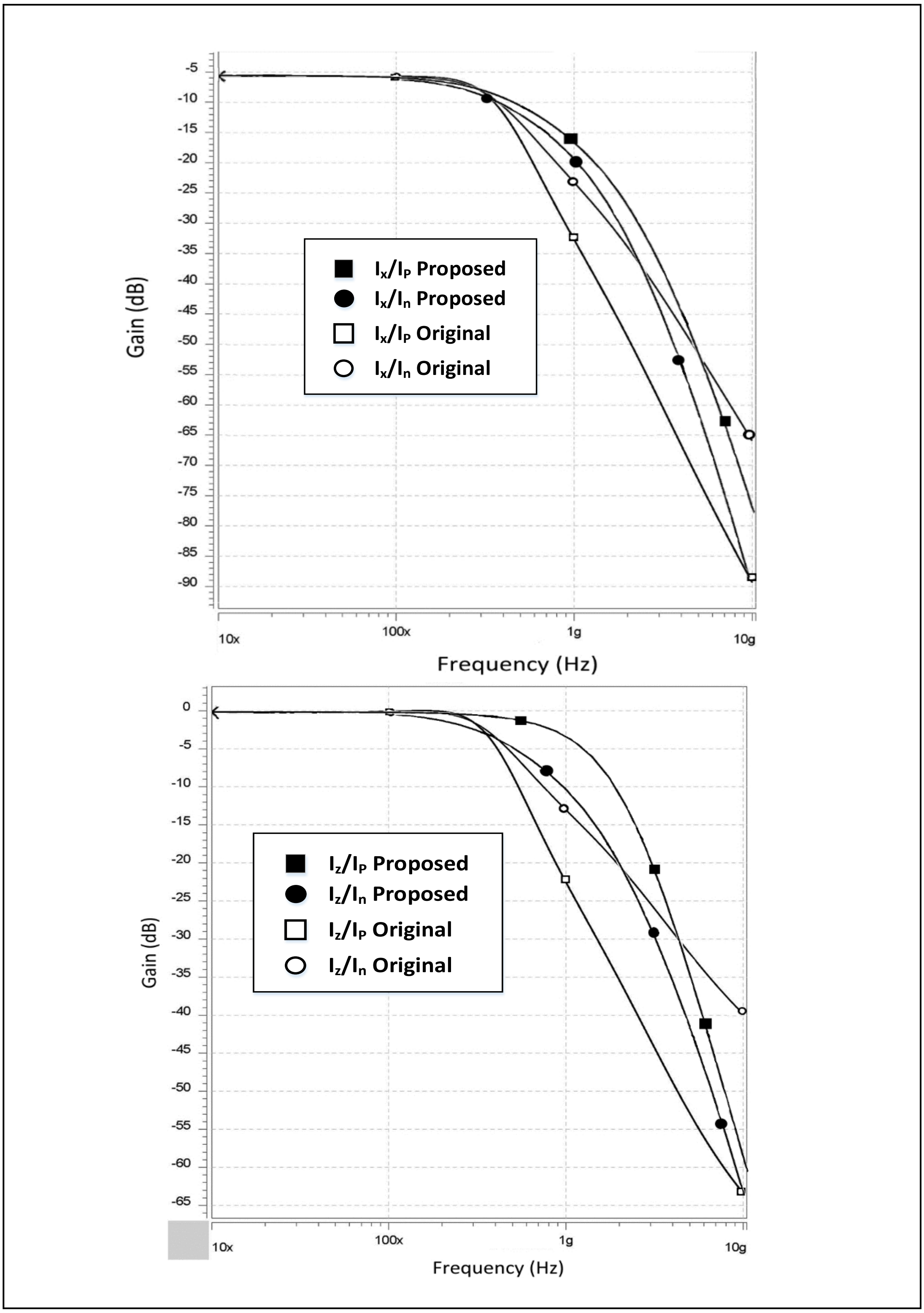


Figure 4.4 Frequency responses at output

Figure 4.5. presents the frequency response of g_m of OTA at I_{B2}

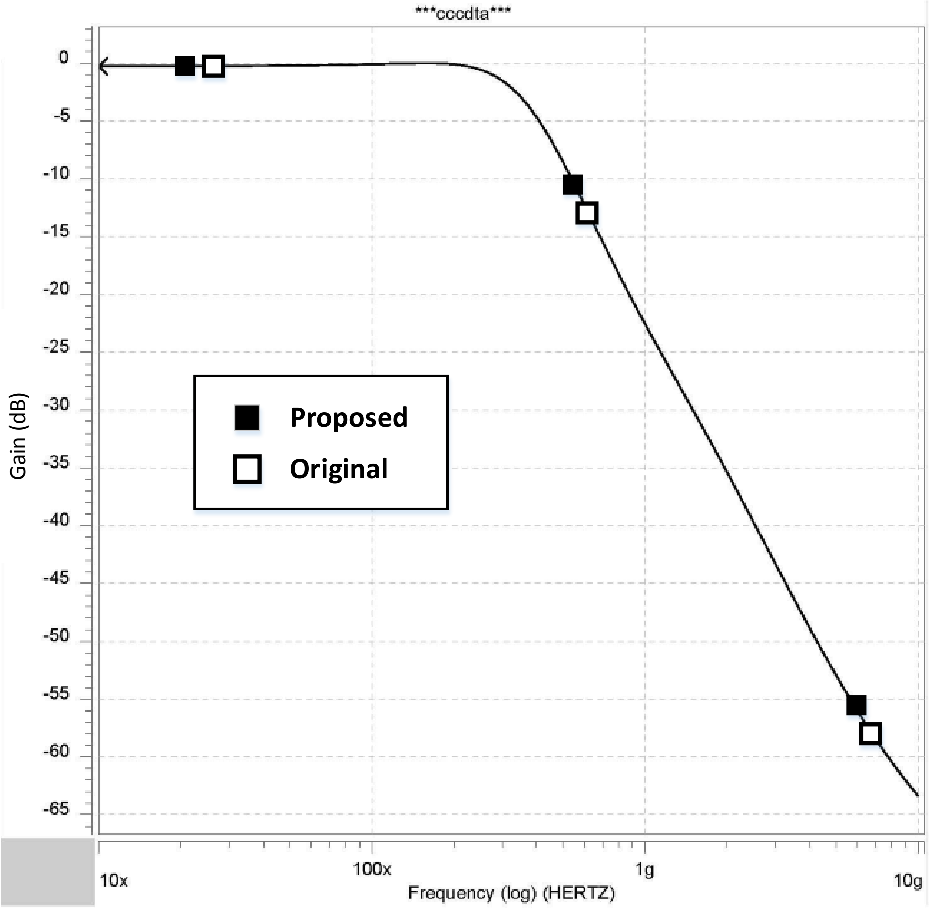


Figure 4.5 Frequency response of g_m

From Table 4.2, the values of R_z and R_x of the proposed structure are 307.52kΩ and 302.71kΩ, respectively. The original CCCDTA has the values 190kΩ and 301.43kΩ for R_z and R_x, respectively. The frequency response simulations I_z/I_p, I_z/I_n, I_x/I_p and I_x/I_n of the proposed CCCDTA can be used with values of R and R_L lie between 10Ω and 1kΩ. Therefore, the proposed element works well when $R_z \geq 300R$ and $R_x \geq 300R_L$. As seen in the simulations of the original structure, the values of R and R_L lie between 10Ω and 1kΩ. So, it works well when $R_z \geq 200R$ and $R_x \geq 300R_L$ [7].

Table 4.2 Conclusion of CCCDTA parameters

Parameters	**Proposed CCCDTA**	**Original CCCDTA**
Power supply voltages	±1.5 V	±1.5 V
Power consumption	900 µW	1.48mW
-3dB Bandwidth	453 MHz (I_z/I_n)	387.51 MHz (I_z/I_n)
	947 MHz (I_z/I_p)	358.82 MHz (I_z/I_p)
	350 MHz (I_x/I_n)	323.31 MHz (I_x/I_n)
	372 MHz (I_x/I_p)	320.89 MHz (I_x/I_p)
Input bias current range for controlling transconductance	1µA – 0.981mA	1µA – 100µA
Transconductance	6.68mS – 0.583S	0.25mS -1mS
Input bias current range for controlling R_n and R_p	1uA - 1.5mA	1µA -1.5mA
R_n	5.62kΩ - 1.33kΩ	1.83kΩ - 1.37kΩ
R_p	776kΩ - 1.76kΩ	1.83kΩ - 1.30kΩ
R_z	307.52kΩ	190kΩ
R_x	302.71kΩ	301.43kΩ

4.2 Loading Effect

Loading effect at z terminal and x terminal of both structures are shown in Figure 4.6.

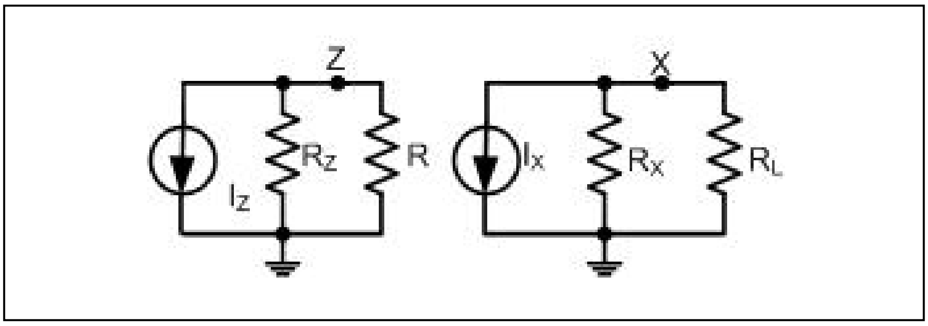


Figure 4.6 Loading effects at z and x terminals

Table 4.3 R_x and R_z values from simulation

Measurement Value	Proposed CCCDTA	Original CCCDTA
R_z	307.52kΩ	190kΩ
R_x	302.71kΩ	301.43kΩ

Loading effect values of R_z and R_x of the proposed structure are 307.52kΩ and 302.71kΩ, respectively. The original CCCDTA has the values 190kΩ and 301.43kΩ for R_z and R_x, respectively. The frequency response simulations I_z/I_p, I_z/I_n, I_x/I_p and I_x/I_n of the proposed CCCDTA can be used with values of R and RL lie between 10Ω and 1kΩ. Therefore, the proposed element works well when $R_z \geq 300R$ and $Rx \geq 300R_L$. From the simulations of the original structure, the values of R and R_L lie between 10Ω and 1kΩ. So, it works well when $R_z \geq 200R$ and $R_x \geq 300R_L$ [7]

4.3 Application of CCCDTA

The application of the proposed novel CCCDTA to current-mode BIQUAD filter is shown in Figure 4.7[2]. The structure uses only one active element and two capacitors. The pole frequency and quality factor of each filter response are shown as following:

$$\omega_p = \sqrt{\frac{g_m}{C_1 C_2 R_n}} \tag{4.1}$$

and

$$Q_p = \sqrt{\frac{C_1 g_m R_n}{C_2}} \tag{4.2}$$

To confirm the theory, HSPICE simulation program is used to define the performance of the current-mode BIQUAD filter with parameter C1 = C2 = 10pF and IB1 = IB2 = 50µA. Figure 4.8, Figure 4.9 and Figure 4.10 show gain and phase response of BIQUAD filter of proposed novel CCCDTA and Figure 4.11, Figure 4.12, and Figure 4.13 show gain and phase response of BIQUAD filter of original CCCDTA.

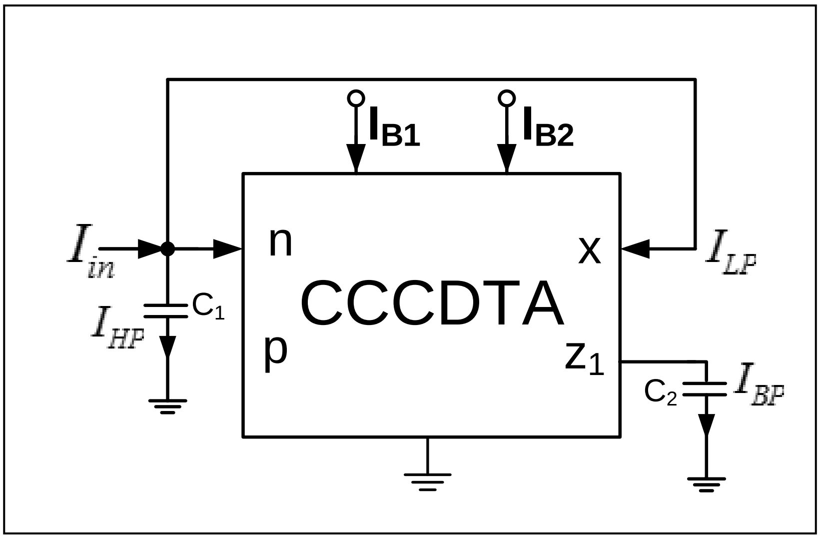


Figure 4.7 Current-mode BIQUAD filter based on CCCDTA

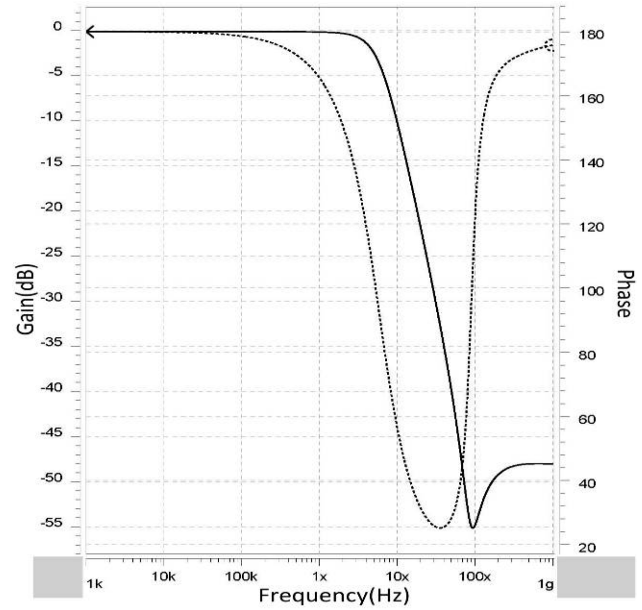


Figure 4.8 Gain and phase responses of current-mode BIQUAD low-pass filter of proposed CCCDTA

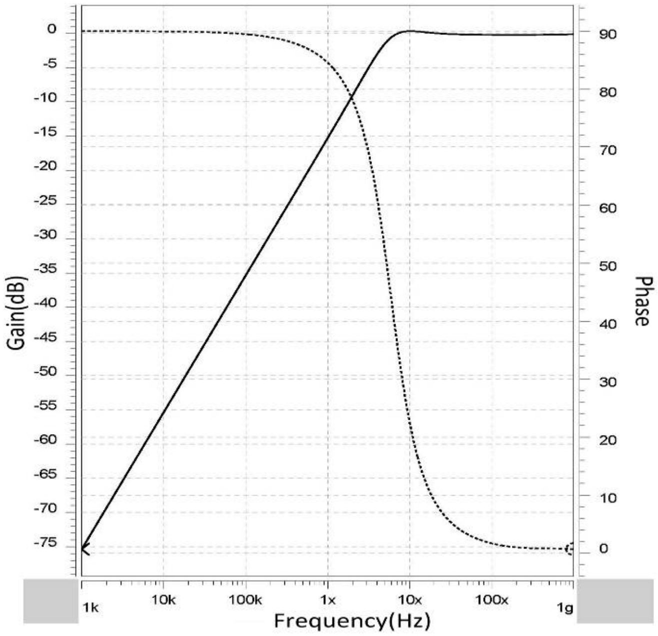


Figure 4.9 Gain and phase responses of current-mode BIQUAD high-pass filter of proposed CCCDTA

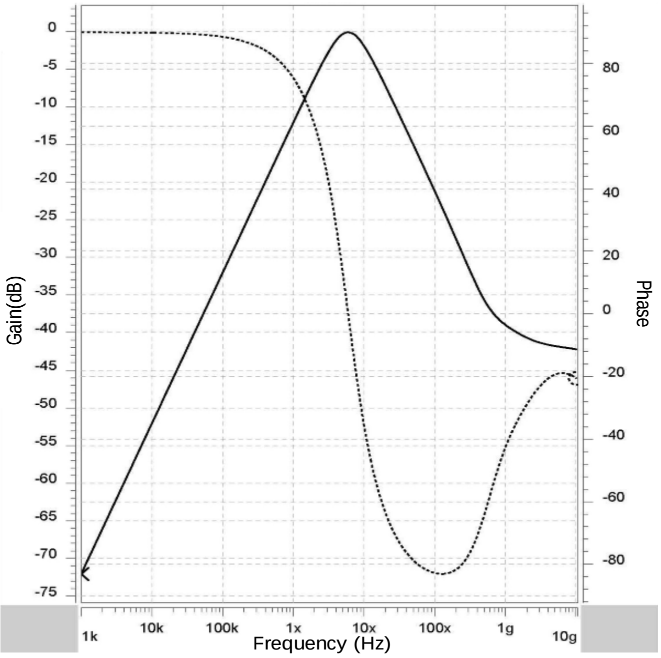


Figure 4.10 Gain and phase responses of current-mode BIQUAD band-pass filter of proposed CCCDTA

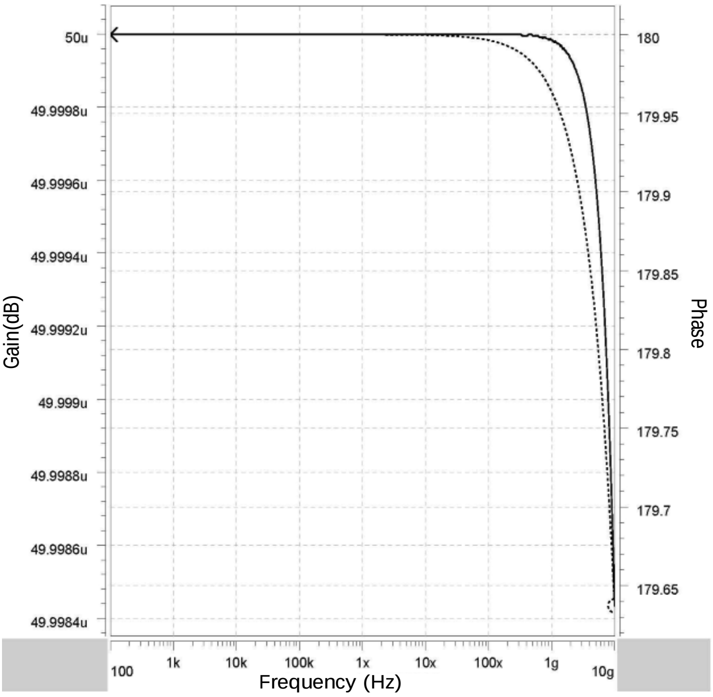


Figure 4.11 Gain and phase responses of current-mode BIQUAD low-pass filter of original CCCDTA

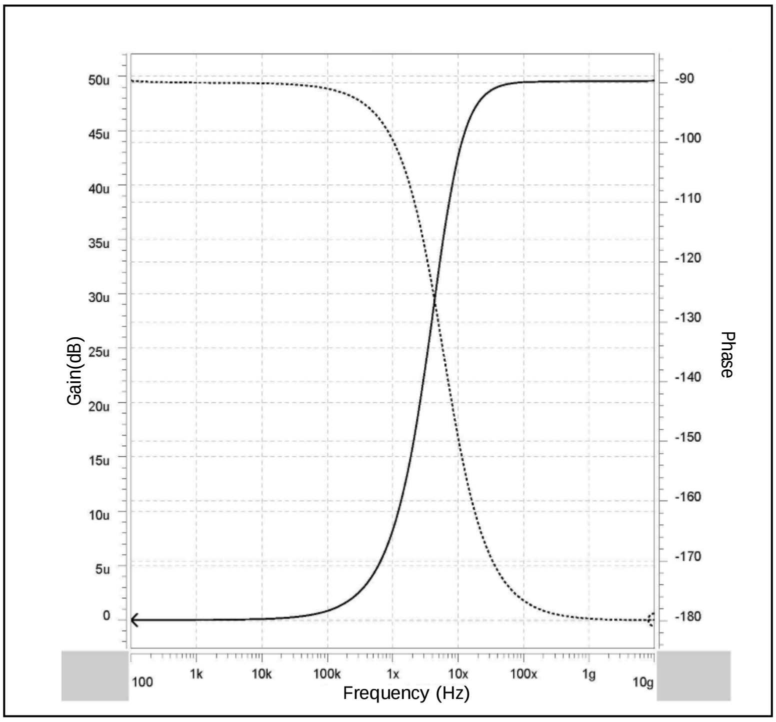


Figure 4.12 Gain and phase responses of current-mode BIQUAD high-pass filter of original CCCDTA

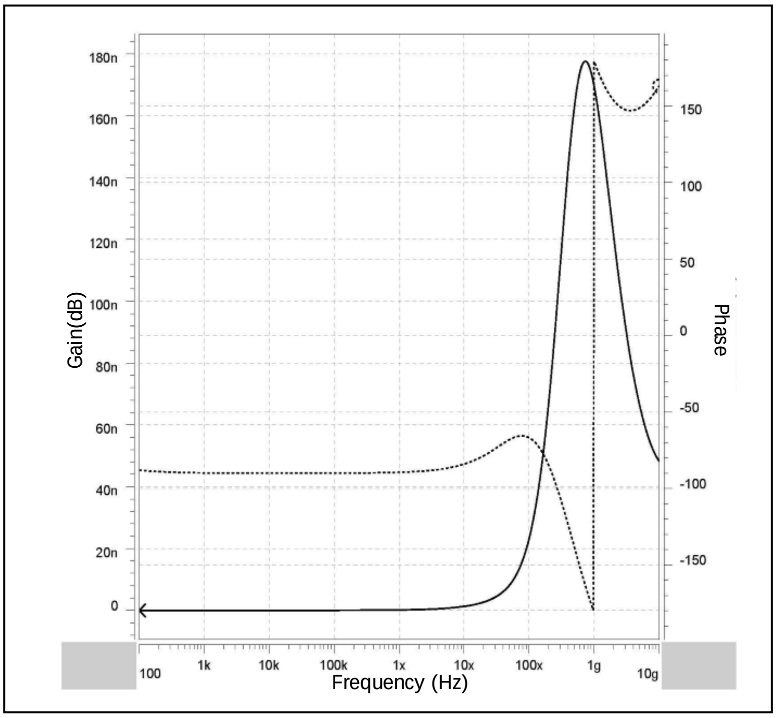


Figure 4.13 Gain and phase responses of current-mode BIQUAD band-pass filter of original CCCDTA

CHAPTER 5 CONCLUSION

5.1 Conclusion

In this thesis, the balanced differential-pair CMOS CCCDTA is proposed to compare with translinear CMOS CCCDTA. The proposed CMOS CCCDTA improves lower bias current, reduces power consumption and has wider current gain responses and lower number of MOSFETs.

The performance of the proposed and original element of CMOS CCCDTA are compared by HSPICE simulation based on AMS’s 0.35μm CMOS process.

The advantages of the proposed CMOS CCCDTA are wide-band of current gain and less required number of MOSFETs is needed. The bias current is also lower and it has lower power consumption, better frequency response and wider controlled-transconductance value when compared with the translinear CMOS CCCDTA.

However, the original CMOS CCCDTA has lower parasitic resistance and wider range of controllability of DC transfer characteristic.

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APPENDIX A

CCCDTA Simulation

Code for simulation

1. Original CCCDTA

```
************define parameter*******************
.param          vdd = 3
+               vss = -3
.param          L = .7u
+               Wn = 21u
+               Wp = 14u
+               bias = 100u
****************CCCII+1*******************
*MOS            d       g       s       b       mos     L       W
Mp1             N01     N01     0       vdd     modp    L       21u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp2             N02     N01     n       vdd     modp    L       21u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp3             N04     N01     p       vdd     modp    L       21u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn4             N15     N15     0       vss     modn    L       6.5u    ad=16p    as=32p
pd=16u ps=24u nrd=1 nrs=2
Mn5             N16     N15     n       vss     modn    L       6.5u    ad=16p    as=32p
pd=16u ps=24u nrd=1 nrs=2
Mn6             N17     N15     p       vss     modn    L       6.5u    ad=16p    as=32p
pd=16u ps=24u nrd=1 nrs=2
Mn7             b       b       vss     vss     modn    L       20u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn8             N14     b       vss     vss     modn    L       20u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn9             N01     b       vss     vss     modn    L       20u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn10            N02     N02     vss     vss     modn    L       14u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn11            N04     N02     vss     vss     modn    L       14u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn12            N04     N04     vss     vss     modn    L       14u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn13            z       N04     vss     vss     modn    L       14u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp14            N14     N14     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp15            N15     N14     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp16            N16     N16     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp17            N17     N16     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp18            N17     N17     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp19            z       N17     vdd     vdd     modp    L       36u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
```

```
Mn20        N17   N15   N06   vss   modn  L     6.5u    ad=16p     as=32p
pd=16u ps=24u nrd=1 nrs=2
Mp21        N04   N01   N06   vdd   modp  L     21u ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2

Ib1 b 0 bias

*****************OTA***********************
*MOS        d     g     s     b     mos   L     W
Mn23        x     0     bb    vss   modn  L     Wn ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mn22        N24   z     bb    vss   modn  L     Wn ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp25        x     N24   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2
Mp24        N24   N24   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u
ps=24u nrd=1 nrs=2

Ib3 bb vss  bias2
```

2. Proposed CCCDTA

```
************define parameter*******************
.param vdd = 3
+      vss = -3
.param L = .7u
+      Wn = 21u
+      Wp = 14u
+      bias = 100u
***************define stimulii******************
vdd vdd 0 vdd
vss vss 0 -vss

*****************CCCII+1*******************
*MOS d     g     s     b     mos   L     W
Mp1  N01   N01   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn1  N01   0     N11   vss   modn  L     Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp2  N02   N02   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn2  N02   0     N11   vss   modn  L     Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp3  N03   N02   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn3  N03   N04   N11   vss   modn  L     Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp4  N04   N01   vdd   vdd   modp  L     Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn4  N04   N04   N11   vss   modn  L     Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
```

```
Ib11 N11 vss  bias
Ib12 N11 vss  bias

*****************CCCII+2********************
*MOS d      g      s      b      mos    L      W
Mp5  N05    N05    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn5  N05    0      N12    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp6  N06    N06    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn6  N06    0      N12    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp7  N07    N06    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn7  N07    N03    N12    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp8  N03    N05    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn8  N03    N03    N12    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2

Ib21 N12 vss bias
Ib22 N12 vss bias

*****************OTA***********************
*MOS d      g      s      b      mos    L      W
Mp9  N09    N09    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn9  N09    N07    N13    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mp10 N10    N09    vdd    vdd    modp   L      Wp ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2
Mn10 N10    0      N13    vss    modn   L      Wn ad=16p as=32p pd=16u ps=24u
nrd=1 nrs=2

Ib3 N13 vss  bias
```

APPENDIX B

PUBLICATION PAPER

CURRICULUM VITAE

NAME	Mr. Ekkarat Karnjanakrajang
DATE OF BIRTH	12 April 1987
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HIGH SCHOOL	High School Graduation Trattrakarnkhun School, 2006
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MASTER'S DEGREE	Master of Engineering (Computer Engineering) King Mongkut's University of Technology Thonburi, 2013
EMPLOYMENT RECORD	System Consultant Engineer Chunbok Co. Ltd., 2010-Present
PUBLICATION	Karnjanakrajang, E., Chaisricharoen, R. and Chipipop, B., 2010 "All differential-pair CMOS current-controlled current differencing transconductance amplifier (CCCDTA)", **Proceeding Of 2010 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS 2010)**, 6-8 December 2010, University of Electronic Science and Technology of China, Cheng Du, China.