EPCOS

Surge Arrester **A71-H08X**

2-Electrode-Arrester Ordering code: **B88069X2140S102**

DC spark-over voltage [1) 2)]	800 ± 15	V %
Impulse spark-over voltage at 100 V/µs - for 99 % of measured values - typical values of distribution at 1 kV/µs - for 99 % of measured values - typical values of distribution	 < 1100 < 1000 < 1200 < 1100	 V V V V
Nominal impulse discharge current (wave 8/20 µs) Single impulse discharge current (wave 8/20 µs)	10 10	kA kA
Nominal alternating discharge current (50 Hz, 1 s) Alternating discharge current (50 Hz, 9 cycles)	10 65	A A
Insulation resistance at 100 V_{dc}	> 10	GΩ
Capacitance at 1 MHz	< 1	pF
Arc voltage at 1 A Glow to arc transition current Glow voltage	~ 20 ~ 0.5 ~ 160	V A V
Weight	~ 1	g
Operation and storage temperature	-40 ... +90	°C
Climatic category (IEC 60068-1)	40/ 90/ 21	
Marking, green	**EPCOS 800 YY O** 800 - Nominal voltage YY - Year of production O - Non radioactive	

1) At delivery AQL 0.65 level II, DIN ISO 2859
2) In ionized mode
Terms in accordance with ITU-T Rec. K.12 and DIN 57845/VDE0845

EPCOS

Surge Arrester	A71-H08X
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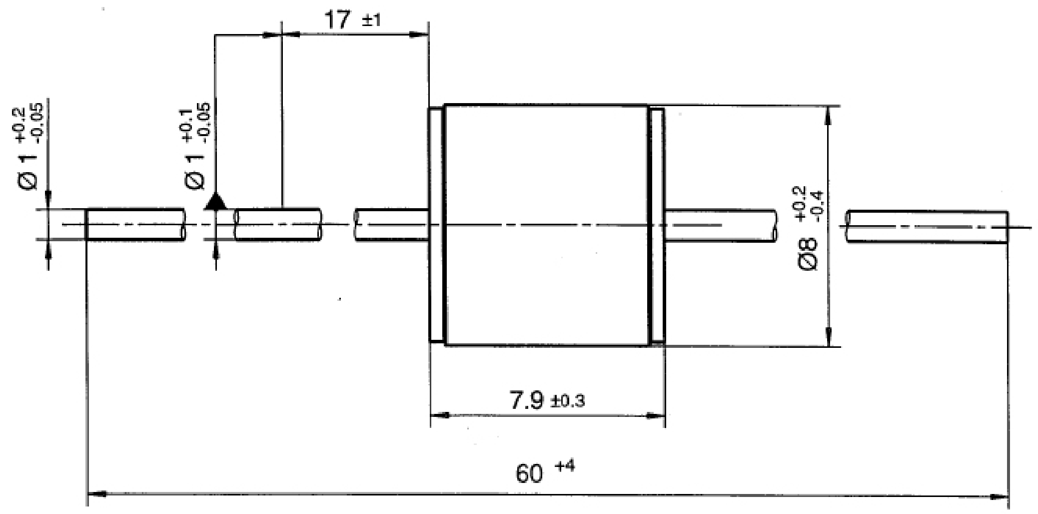


Not to scale

Dimensions in mm

Non controlled document

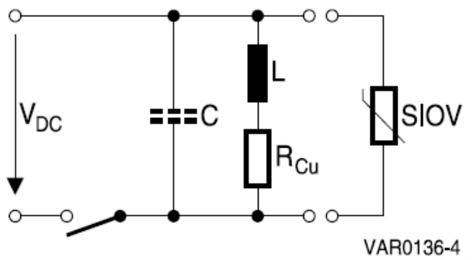
1 Calculation examples

1.1 Switching off inductive loads

The discharge of an inductor produces high voltages that endanger both the contact breaker (switching transistor and the like) and the inductor itself. According to equation 17 the energy stored in the coil is $W = \frac{1}{2} L i^2$. So, when the inductor is switched off, this energy charges a capacitor in parallel with the inductor (this capacitor can also be the intrinsic capacitance of the coil). Not allowing for the losses, and for $\frac{1}{2} C v^2 = \frac{1}{2} L i^2$, the values of figure 1 produce:

$$v^* = i^* \sqrt{\frac{L}{C}} = 1 \sqrt{\frac{0.1}{250 \cdot 10^{-12}}} = 20\ 000\ \text{V}$$

To suppress this transient, a varistor is to be connected in parallel with the inductor as a flywheel circuit.



V_{DC}	=	24 V
L	=	0.1 H
R_{Cu}	=	24 Ω
I	=	1 A
C	=	250 pF
Required switching rate	=	10^6
Period	=	10 s
Required protection level	<	65 V

Figure 1 Limiting switching transients with a varistor as a flywheel circuit

Operating voltage

The DC operating voltage is given as 24 V (cf. figure 1). If the possible increase in operating voltage is no more than 2 V, types with a maximum permissible DC operating voltage of 26 V should be chosen from the product tables to achieve at as low a protection level as possible. Type S … K20 and S … K20E2 are available for this application.

Surge current

When it is cut off, the current through an inductor cannot change abruptly, so it flows across the varistor initially with the value of the operating current (here 1 A), then decaying towards zero following an exponential function.

The simplest ways of determining the current duration are simulation or measurement ($\tau = t^*_r$).

EPCOS

Calculation examples

The time constant can also be calculated to an approximation with equation 13.
Here the varistor resistance of voltage class K20 is calculated for 1 A. As the protection levels of the various type series do not differ much, the S10K20 has been chosen arbitrarily to determine the resistance (the voltage is taken from the appropriate V/I characteristics).

$$R_{SIOV} = \frac{55\ V}{1\ A} = 55\ \Omega$$

So τ according to equation 13 is

$$\tau = t^*_r = \frac{0.1\ H}{24\ \Omega\ +\ 55\ \Omega} \approx 1.3\ ms$$

For S10K20 with t^*_r = 1.3 ms and 10^6 load repetitions, you obtain
$i_{max} = 3\ A > i^* = 1\ A$
from the derating curves.

Taking this result, you should check whether other types with lower current ratings satisfy the selection criterion:

S05K20: $i_{max} = 0.5\ A < i^* = 1\ A$
S07K20: $i_{max} = 1.4\ A > i^* = 1\ A$

For example, using a varistor of AdvanceD series S…K20E2 would not achieve any advantages at 10^6 load repetitions because in this region the derating fields of this series are not different from those of the StandarD series.
So the selection criterion of equation 9 is met by SIOV-S07K20 and all types with higher current ratings.

Energy absorption

The maximum energy absorption capacity of SIOV-S07K20 for t*r =1.3 ms, i_{max} = 1.4 A and 10^6 repetitions according to equation 18 is

$W_{max} = v_{max} \cdot i_{max} \cdot t_{r\ max} = 60 \cdot 1.4 \cdot 0.0013 = 0.11\ J$ (with $t_{r\ max} = t^*_r$ according to chapter "Selection procedure", section 1.5.3)

According to equation 17 the varistor must in the worst case absorb energy of
$W^* = ½\ L\ i^{*2} = ½ \cdot 0.1\ H \cdot 1\ A^2 = 0.05\ J < W_{max} = 0.11\ J$
per switching cycle. Thus SIOV-S07K20 also satisfy the selection requirement of equation 10.

Average power dissipation

According to equation 19, applied energy of 0.05 J every 10 s produces average power dissipation of

$$P^* = \frac{W^*}{T^*} = \frac{0.05}{10} = 0.005\ W$$

The product table shows maximum dissipation capability of 0.02 W for SIOV-S07K20. So on this point too, the choice is correct (equation 11).

For the sake of completeness, the minimum permissible time between two applications of energy is calculated (equation 20):

$$T_{min} = \frac{W^*}{P_{max}} = \frac{0.05\ J}{0.02\ W} = 2.5\ s$$

Maximum protection level

The V/I curve for S07K20 shows a protection level of 60 V at 1 A for the worst-case position in the tolerance field (PSpice supplied by EPCOS: TOL = +10).
This means that type S07K20 meets the requirement for a protection level < 65 V.

1.2 Ensuring EMC of equipment connected to 230 V line voltages

The example describes the selection procedure for a varistor that is to ensure the EMC of a device in accordance with IEC 61000-4-5 for 230 V operating voltage and a test voltage of 4 kV.

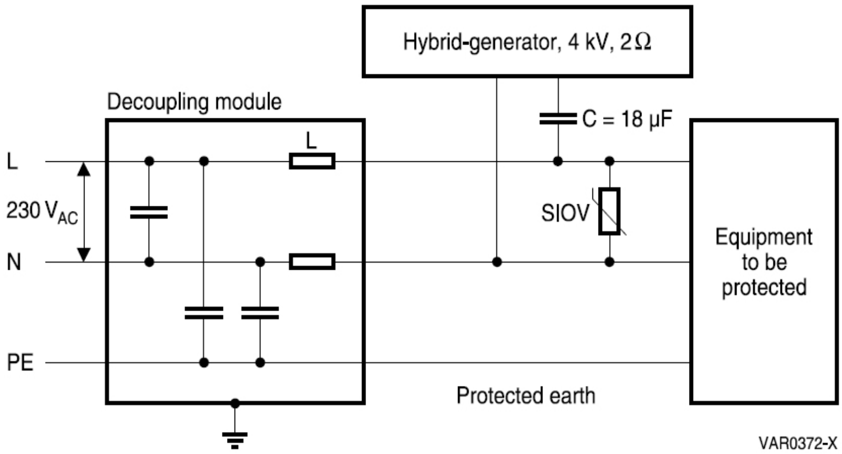


Figure 2 EMC test in accordance with IEC 61000-4-5 with R_i = 2 Ω, charge voltage 4 kV on a 230 V_{AC} line voltage

Line voltage:	230 V_{AC} ±10%
Hybrid test generator:	4 kV, 2 Ω
Number of repetitions:	10 (5 in each polarity)
Voltage endurance of equipment to be protected:	1 kV

Look up this type in the derating diagram (drawing S14K50 … 320) to check whether or not an S14K275 can be subjected to the above surge current load. As a result of the investigation, a current of 1590 A (8/20 μs) is only permissible for two consecutive load cycles. For the required number of ten repetitions, the current i_{max} would be 1000 A only.

Since $i^* > i_{max}$, S14K275 is not a suitable choice for the given application conditions.

The type with the next highest surge current capability would be S14K275E2. The derating field yields i_{max} (10 ×) = 1500 A. For this reason this type is not suitable either.

As a result the selection check procedure must be repeated for the type series having the next highest power dissipation capability, SIOV-S20 series. In this case the type in question is the varistor type S20K275:

Here equation 12 results in

$$i^* = \frac{4000\ \text{V} - \left(950 \cdot \frac{0.9}{1.1}\right)\text{V}}{2\ \Omega} = \frac{4000\ \text{V} - 780\ \text{V}}{2\ \Omega} = \frac{3220\ \text{V}}{2\ \Omega} = 1610\ \text{A}$$

For ten load repetitions (at $t_r^* = t_r = 20\ \mu s$) the derating field of the S20K275 shows

$i_{max} = 2500$ A.

With this value the S20K275 meets the selection criterion of equation 9:

$i^* \leq i_{max}$.

Energy absorption

Since energy absorption, as calculated by equation 6, is directly correlated to surge current, the S20K275 also fulfils the selection criterion of equation 10:

$W^* \leq W_{max}$.

Power dissipation

In order to determine power dissipation, you must calculate the energy absorbed by the S20K275 when conducting the surge current. According to equation 16:

$W^* = v^* \cdot i^* \cdot t_r^* = 780\ \text{V} \cdot 1610\ \text{A} \cdot 20 \cdot 10^{-6}\ \text{s} = 25\ \text{J}$

As a pulse repetition rate, IEC 61000-4-5 specifies a maximum of one pulse/60 s. Inserting this in equation 19 results in:

$$P^* = \frac{W^*}{T^*} = \frac{25\ \text{J}}{60\ \text{s}} \approx 0.4\ \text{W}$$

From the product table the maximum permissible periodic load, i.e. average maximum power dissipation of an S20K275, is found to be 1 W. With this the selection criterion of equation 11,

$P^* \leq P_{max}$

is also met.

Calculation examples

Protection level

The protection level is found to be 900 V (from the V/I characteristics for a value of 1610 A). In this case the 4 kV “overvoltage” is limited to 23%.

The protection level is lower than the voltage strength of the equipment to be protected, which is equal to 1000 V.

By fulfilling this final criterion, the StandarD SIOV-S20K275 is found to meet all selection criteria and can thus be considered suitable for the application.

Comparison to PSpice

Selection of the varistors for table 3 was carried out using PSpice calculations. The results for S20K275 correlate well with the values calculated here.

Other suitable types

If the physical dimensions of the chosen component SIOV-S20K275 are too large, similar selection calculations show that the EnergetiQ varistor SIOV-Q14K275, which requires less headroom, is also suitable.

For comparison:

For comparison:

SIOV-S20K275	h_{max} = 25.5 mm
SIOV-Q14K275	h_{max} = 19.5 mm

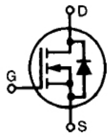
IXYS

MegaMOS™ Power MOSFET

IRFP 460

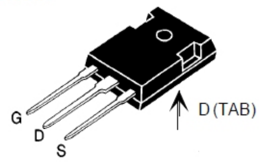
V_{DSS} = 500 V
$I_{D(cont)}$ = 20 A
$R_{DS(on)}$ = 0.27Ω

N-Channel Enhancement Mode, HDMOS™ Family



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	20	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	80	A
I_{AR}		20	A
E_{AR}	T_C = 25°C	28	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100 A/µs, $V_{DD} \le V_{DSS}$, $T_J \le$ 150°C, R_G = 2 Ω	3.5	V/ns
P_D	T_C = 25°C	260	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque	1.15/10	Nm/lb.in.
Weight		6	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

TO-247 AD



G = Gate, D = Drain,
S = Source, TAB = Drain

Features

- Repetitive avalanche energy rated
- Fast switching times
- Low $R_{DS (on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- High Commutating dv/dt Rating

Applications

- Switching Power Supplies
- Motor controls

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 µA		500			V
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2		4	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0				±100	nA
I_{DSS}	V_{DS} = 0.8 • V_{DSS}	T_J = 25°C			25	µA
	V_{GS} = 0 V	T_J = 125°C			250	µA
$R_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			0.25	0.27	Ω

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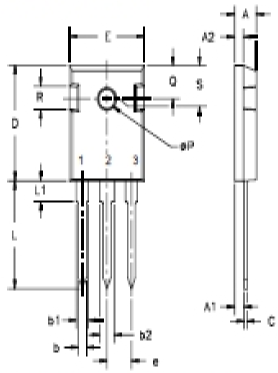
Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	V_{DS} = 10 V; I_D = 12 A, pulse test	13	21		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		4200		pF
C_{oss}			450		pF
C_{rss}			135		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 250 V, I_D = 20 A; R_G = 4.3 Ω, (External)		23	35	ns
t_r			81	120	ns
$t_{d(off)}$			85	130	ns
t_f			65	98	ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 200 V, I_D = 20 A		135	210	nC
Q_{gs}			28	40	nC
Q_{gd}			62	110	nC
R_{thJC}				0.45	K/W
R_{thCK}			0.25		K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
I_S	V_{GS} = 0 V			20	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			80	A
V_{SD}	I_F = 20 A, V_{GS} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %			1.8	V
t_{rr}	I_F = 20 A, -di/dt = 100 A/µs, V_R = 100 V		570	860	ns
Q_{rr}			5.7		µC

TO-247 AD Outline



Terminals: 1 - Gate 2 - Drain
3 - Source Tab - Drain

Dim.	Millimeter Min.	Millimeter Max.	Inches Min.	Inches Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15 BSC		242 BSC	

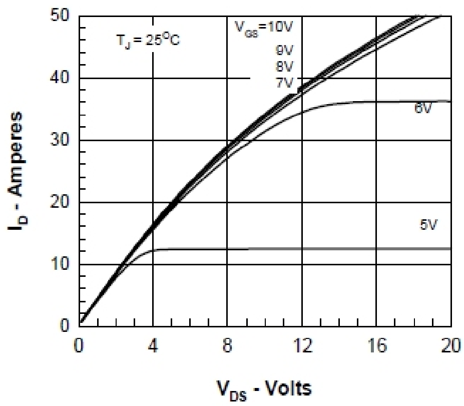


Figure 1. Output Characteristics at 25°C

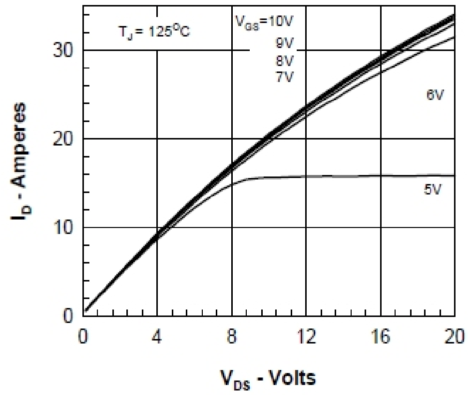


Figure 2. Output Characteristics at 125°C

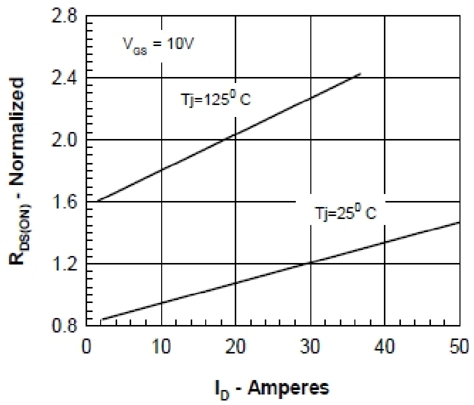


Figure 3. $R_{DS(on)}$ normalized to value at I_D = 12A

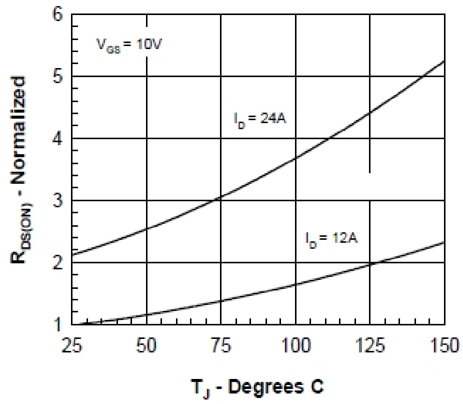


Figure 4. $R_{DS(on)}$ normalized to value at I_D = 12A

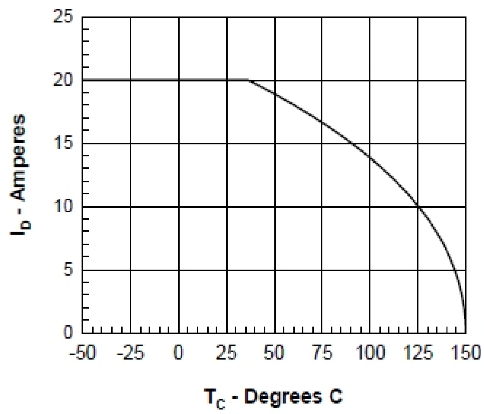


Figure 5. Drain Current vs. Case Temperature

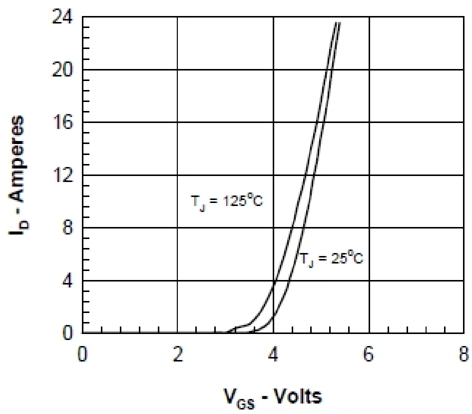
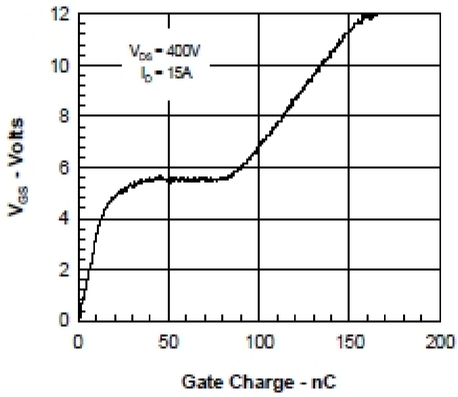
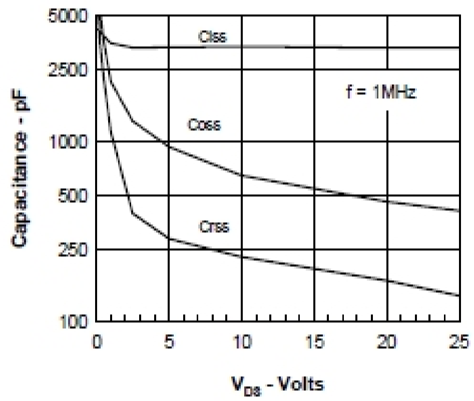
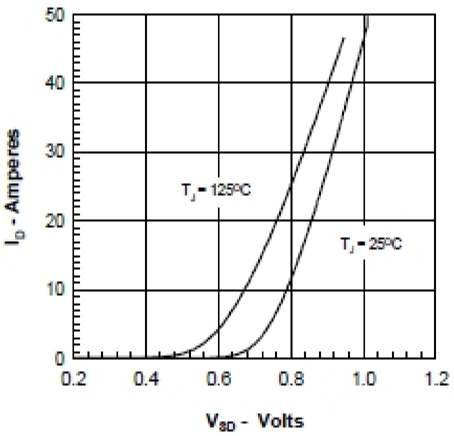


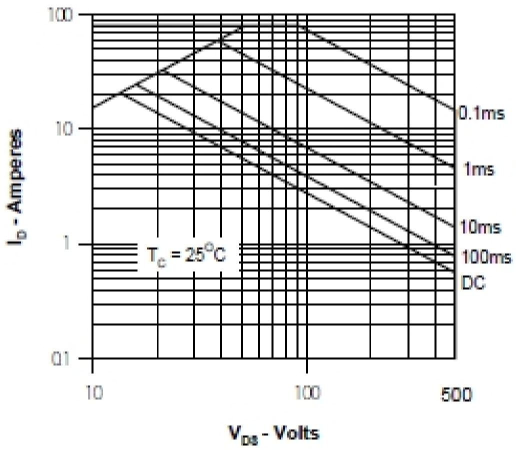
Figure 6. Admittance Curves

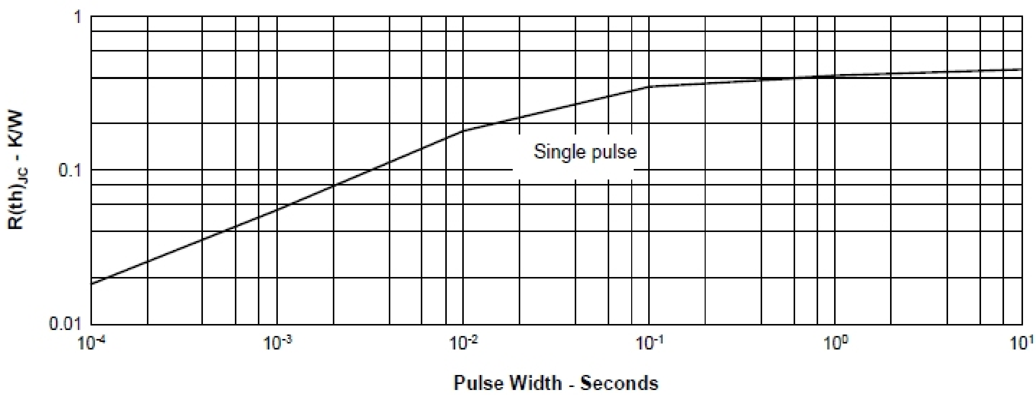
IXYS **IRFP 460**

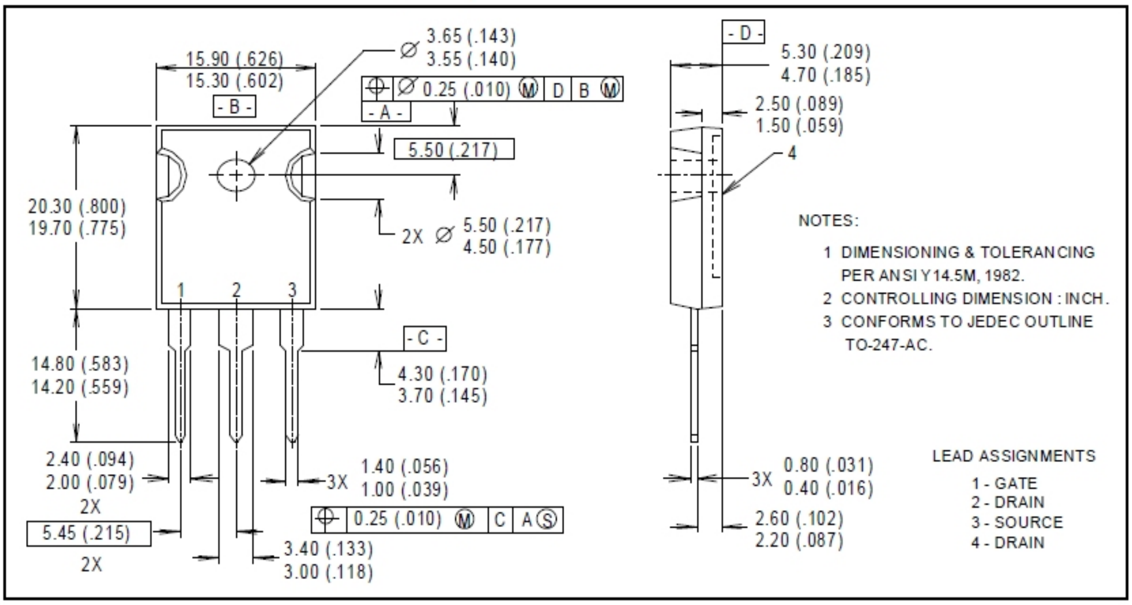






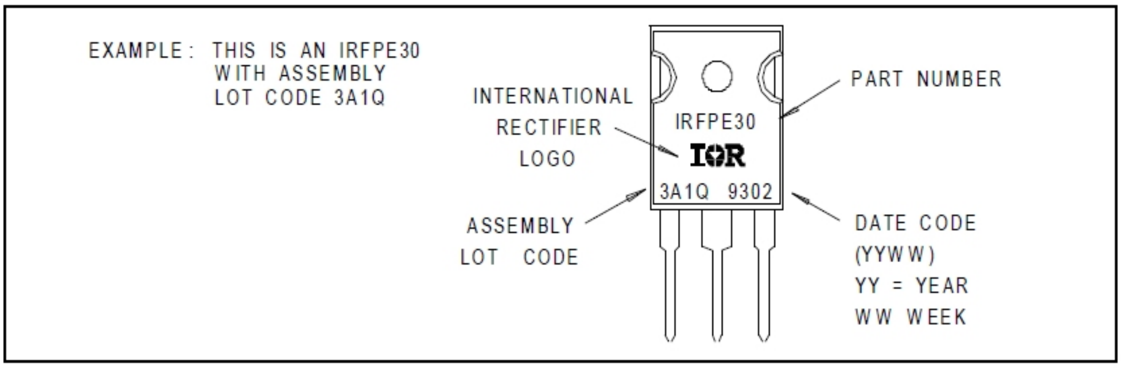






Part Marking Information

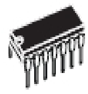
HEXFET TO-247AC



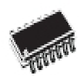
LM124
LM224 - LM324

LOW POWER QUAD OPERATIONAL AMPLIFIERS

- WIDE GAIN BANDWIDTH : 1.3MHz
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GROUND
- LARGE VOLTAGE GAIN : 100dB
- VERY LOW SUPPLY CURRENT/AMPLI : 375µA
- LOW INPUT BIAS CURRENT : 20nA
- LOW INPUT OFFSET VOLTAGE : 5mV max. (for more accurate applications, use the equivalent parts LM124A-LM224A-LM324A which feature 3mV max.)
- LOW INPUT OFFSET CURRENT : 2nA
- WIDE POWER SUPPLY RANGE :
  SINGLE SUPPLY : +3V TO +30V
  DUAL SUPPLIES : ±1.5V TO ±15V



N
DIP14
(Plastic Package)



D
SO14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

DESCRIPTION

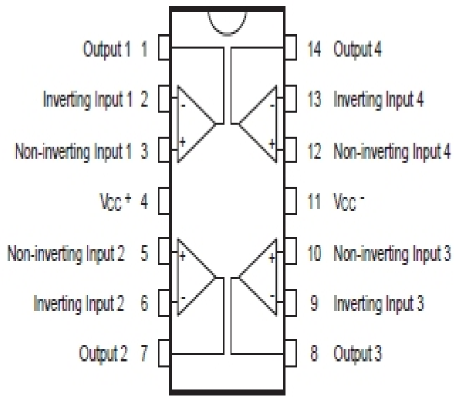
These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

ORDER CODE

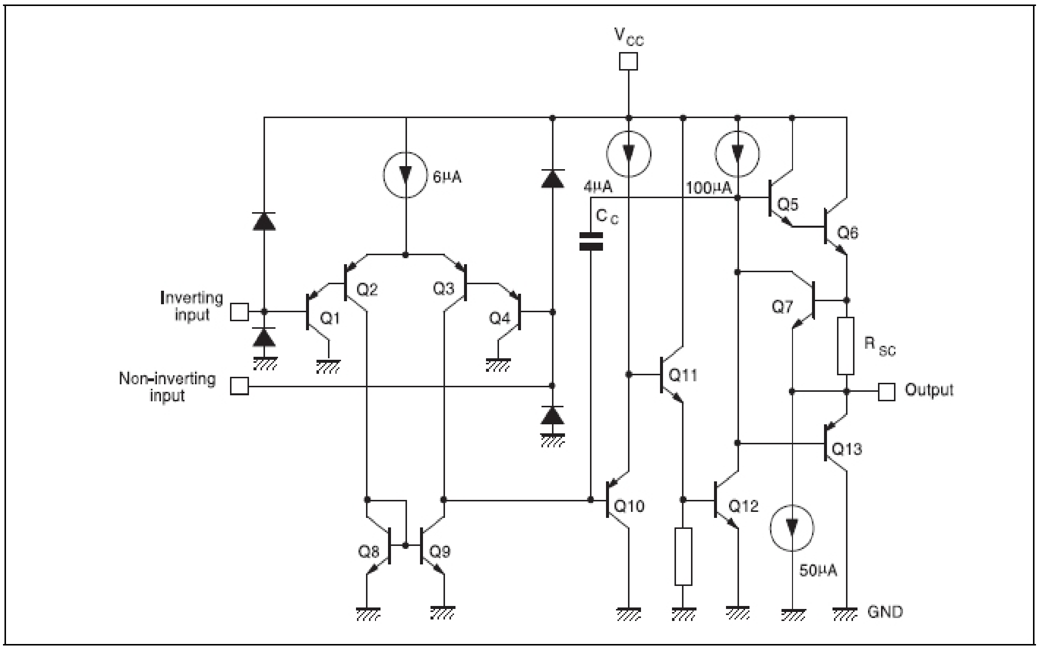
Part Number	Temperature Range	Package		
		N	D	P
LM124	-55°C, +125°C	•	•	•
LM224	-40°C, +105°C	•	•	•
LM324	0°C, +70°C	•	•	•
Example : LM224N				

N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape &Reel (PT)

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM (1/4 LM124)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		LM124	LM224	LM324	Unit
V_{CC}	Supply voltage		±16 or 32			V
V_i	Input Voltage		-0.3 to +32			V
V_{id}	Differential Input Voltage 1)		+32			V
P_{tot}	Power Dissipation	N Suffix D Suffix	500	500 400	500 400	mW mW
	Output Short-circuit Duration 2)		Infinite			
I_{in}	Input Current 3)		50	50	50	mA
T_{oper}	Opearting Free-air Temperature Range		-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range		-65 to +150			°C

1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-.
2. Short-circuits from the output to VCC can cause excessive heating if V_{CC} > 15V. The maximum output current is approximately 40mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuit on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diodes clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. this transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time duration than an input is driven negative.
This is not destructive and normal output will set up again for input voltage higher than -0.3V.

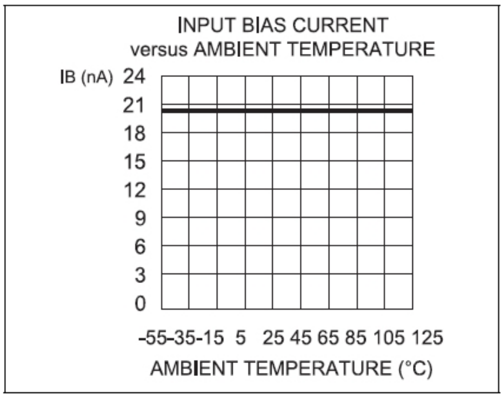
ELECTRICAL CHARACTERISTICS

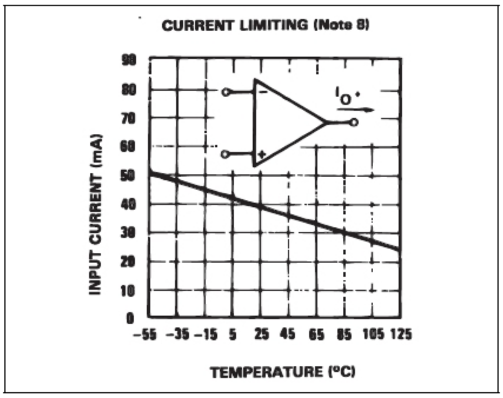
V_{CC}^+ = +5V, V_{CC}^-= Ground, V_o = 1.4V, T_{amb} = +25°C (unless otherwise specified)

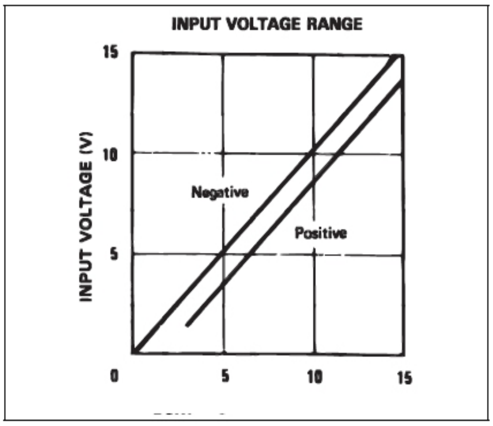
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - note 1) T_{amb} = +25°C LM324 $T_{min} \le T_{amb} \le T_{max}$ LM324		2	5 7 7 9	mV
I_{io}	Input Offset Current T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		2	30 100	nA
I_{ib}	Input Bias Current - note 2) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		20	150 300	nA
A_{vd}	Large Signal Voltage Gain V_{CC}^+ = +15V, R_L = 2kΩ, V_o = 1.4V to 11.4V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio ($R_s \le$ 10kΩ) V_{CC}^+ = 5V to 30V T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	65 65	110		dB
I_{CC}	Supply Current, all Amp, no load T_{amb} = +25°C V_{CC} = +5V V_{CC} = +30V $T_{min} \le T_{amb} \le T_{max}$ V_{CC} = +5V V_{CC} = +30V		0.7 1.5 0.8 1.5	1.2 3 1.2 3	mA
V_{icm}	Input Common Mode Voltage Range V_{CC} = +30V - note 3) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	0 0		V_{CC} -1.5 V_{CC} -2	V
CMR	Common Mode Rejection Ratio ($R_s \le$ 10kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	70 60	80		dB
I_{source}	Output Current Source (V_{id} = +1V) V_{CC} = +15V, V_o = +2V	20	40	70	mA
I_{sink}	Output Sink Current (V_{id} = -1V) V_{CC} = +15V, V_o = +2V V_{CC} = +15V, V_o = +0.2V	10 12	20 50		mA µA
V_{OH}	High Level Output Voltage V_{CC} = +30V T_{amb} = +25°C R_L = 2kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25°C R_L = 10kΩ $T_{min} \le T_{amb} \le T_{max}$ V_{CC} = +5V, R_L = 2kΩ T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	26 26 27 27 3.5 3	27 28		V

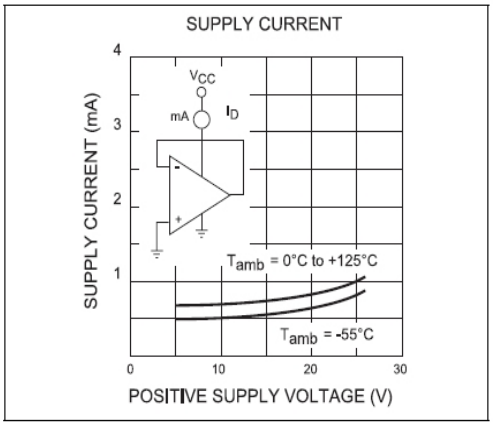
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Low Level Output Voltage ($R_L = 10k\Omega$) $T_{amb} = +25°C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew Rate $V_{CC} = 15V$, $V_i = 0.5$ to $3V$, $R_L = 2k\Omega$, $C_L = 100pF$, unity Gain		0.4		V/µs
GBP	Gain Bandwidth Product $V_{CC} = 30V$, $f = 100kHz$, $V_{in} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$		1.3		MHz
THD	Total Harmonic Distortion $f = 1kHz$, $A_v = 20dB$, $R_L = 2k\Omega$, $V_o = 2V_{pp}$, $C_L = 100pF$, $V_{CC} = 30V$		0.015		%
e_n	Equivalent Input Noise Voltage $f = 1kHz$, $R_s = 100\Omega$, $V_{CC} = 30V$		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input Offset Voltage Drift		7	30	µV/°C
DI_{Iio}	Input Offset Current Drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel Separation - note 4) $1kHz \leq f \leq 20kHZ$		120		dB

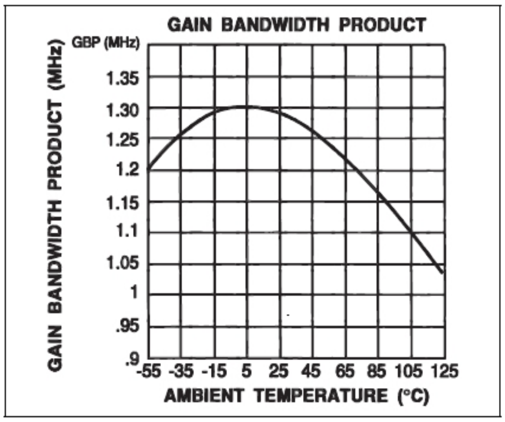
1. $V_o = 1.4V$, $R_s = 0\Omega$, $5V < V_{CC}^+ < 30V$, $0 < V_{ic} < V_{CC}^+ - 1.5V$
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{CC}^+ - 1.5V$, but either or both inputs can go to +32V without damage.
4. Due to the proximity of external components insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequences.

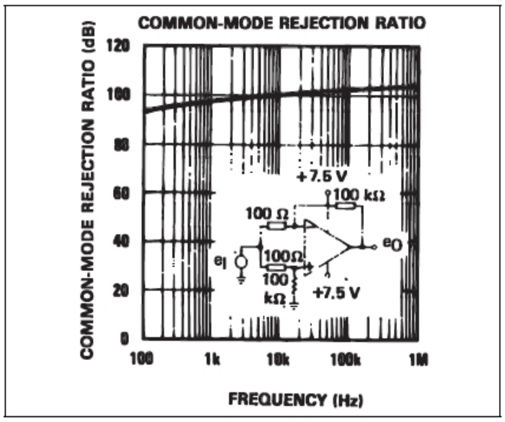

INPUT BIAS CURRENT
versus AMBIENT TEMPERATURE
IB (nA)
24
21
18
15
12
9
6
3
0
-55-35-15 5 25 45 65 85 105 125
AMBIENT TEMPERATURE (°C)


CURRENT LIMITING (Note 8)
INPUT CURRENT (mA)
90
80
70
60
50
40
30
20
10
0
-55 -35 -15 5 25 45 65 85 105 125
TEMPERATURE (°C)

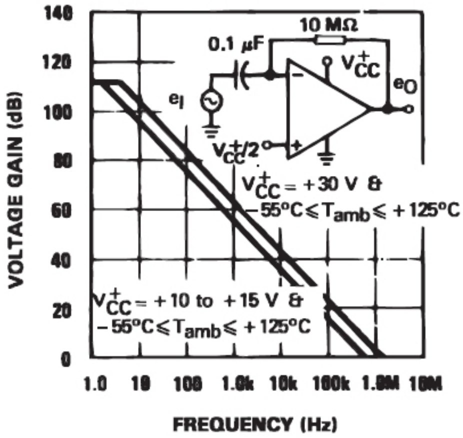

INPUT VOLTAGE RANGE
INPUT VOLTAGE (V)
15
10
5
0
5
10
15
Negative
Positive


SUPPLY CURRENT
SUPPLY CURRENT (mA)
4
3
2
1
VCC
mA
ID
Tamb = 0°C to +125°C
Tamb = -55°C
0
10
20
30
POSITIVE SUPPLY VOLTAGE (V)

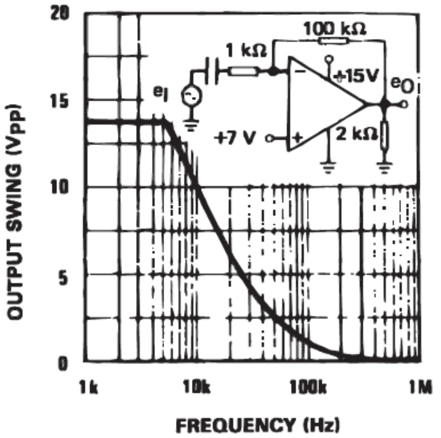

GAIN BANDWIDTH PRODUCT
GAIN BANDWIDTH PRODUCT (MHz)
GBP (MHz)
1.35
1.30
1.25
1.2
1.15
1.1
1.05
1
.95
.9
-55 -35 -15 5 25 45 65 85 105 125
AMBIENT TEMPERATURE (°C)


COMMON-MODE REJECTION RATIO
COMMON-MODE REJECTION RATIO (dB)
120
100
80
60
40
20
0
+7.5 V
100 kΩ
100 Ω
100Ω
100 kΩ
eI
eO
+7.5 V
100
1k
10k
100k
1M
FREQUENCY (Hz)

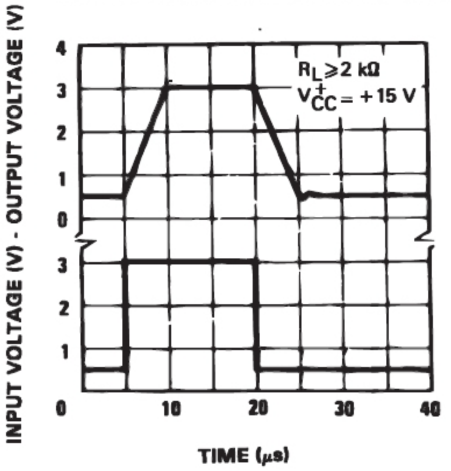
OPEN LOOP FREQUENCY RESPONSE



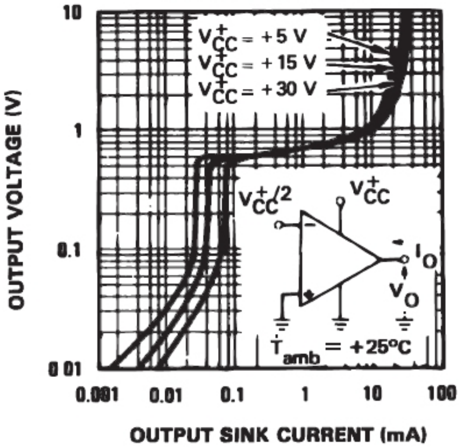
LARGE SIGNAL FREQUENCY RESPONSE



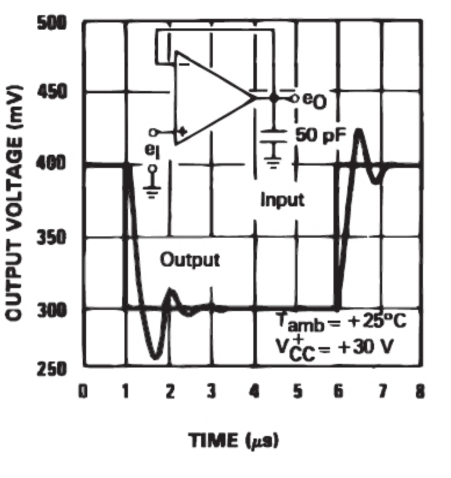
VOLTAGE FOLLOWER PULSE RESPONSE



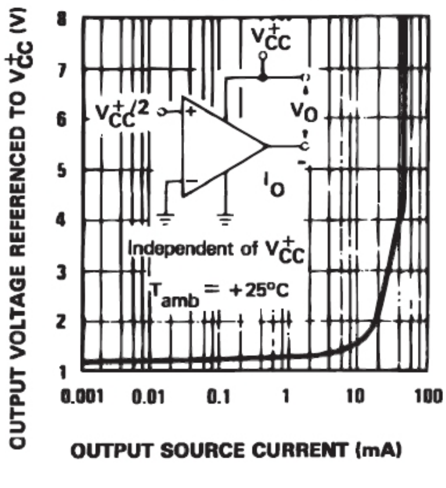
OUTPUT CHARACTERISTICS (CURRENT SINKING)

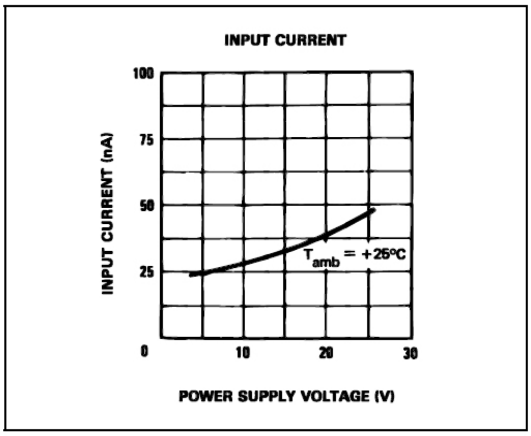


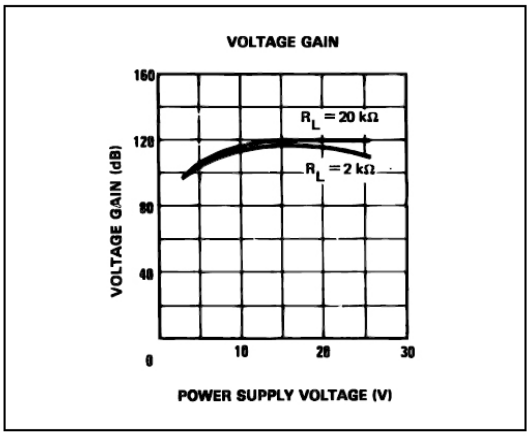
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

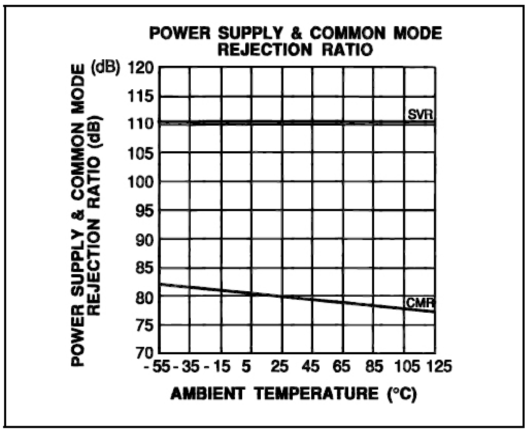


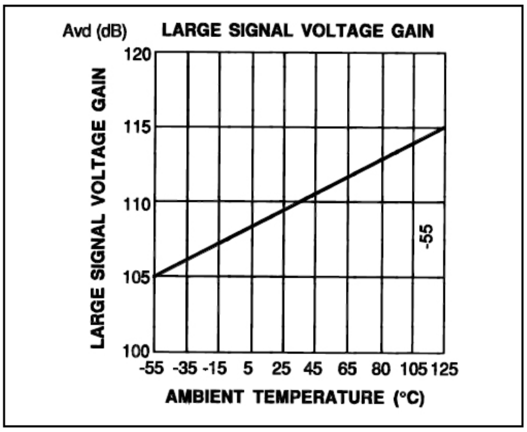
OUTPUT CHARACTERISTICS (CURRENT SOURCING)





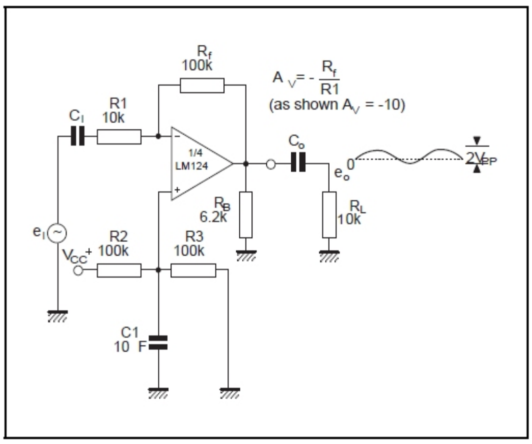




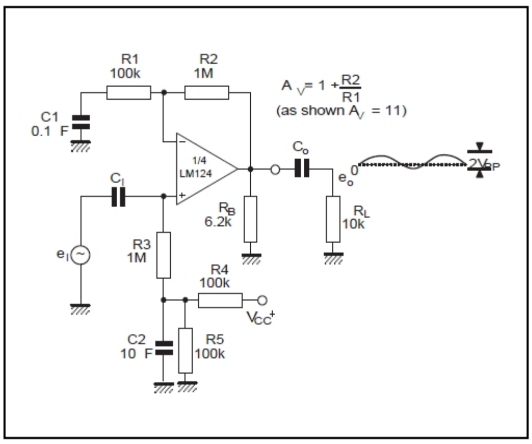


TYPICAL SINGLE - SUPPLY APPLICATIONS

AC COUPLED INVERTING AMPLIFIER

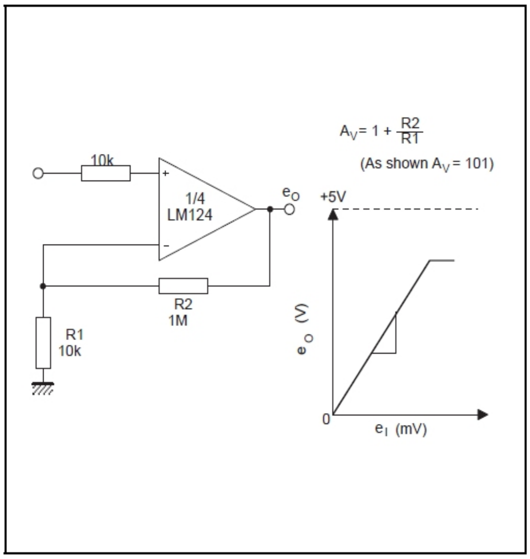


AC COUPLED NON INVERTING AMPLIFIER

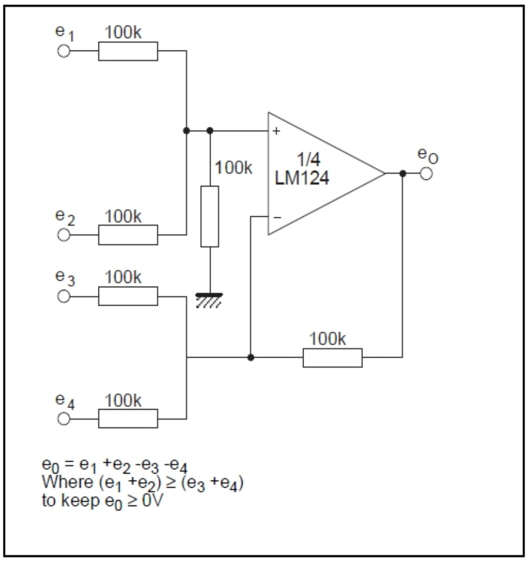


TYPICAL SINGLE - SUPPLY APPLICATIONS

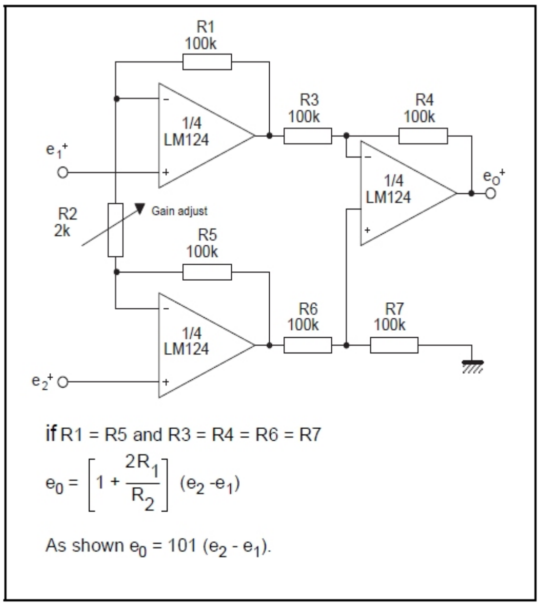
NON-INVERTING DC GAIN



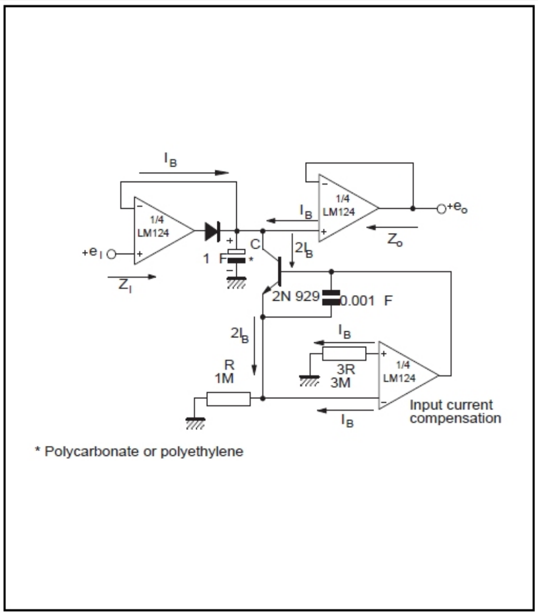
DC SUMMING AMPLIFIER



HIGH INPUT Z ADJUSTABLE GAIN DC INSTRUMENTATION AMPLIFIER

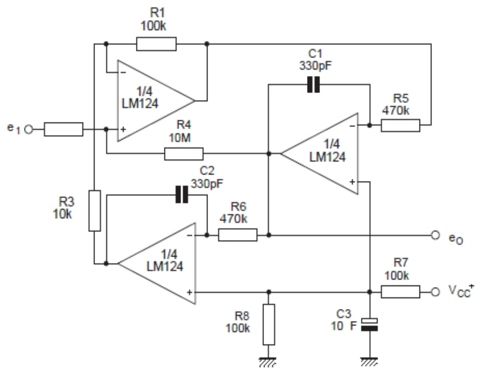


LOW DRIFT PEAK DETECTOR



TYPICAL SINGLE - SUPPLY APPLICATIONS

ACTIVER BANDPASS FILTER



F_o = 1kHz

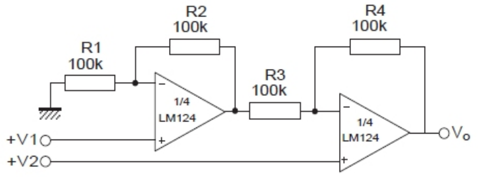
Q = 50

A_v = 100 (40dB)

HIGH INPUT Z, DC DIFFERENTIAL AMPLIFIER

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$

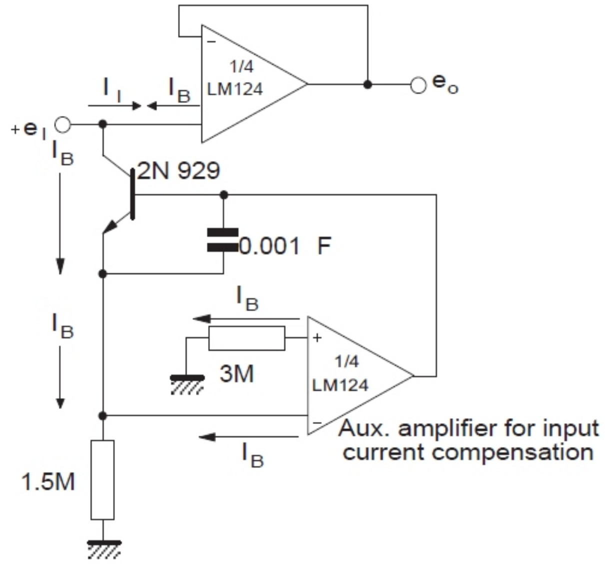
(CMRR depends on this resistor ratio match)



$e_0 \left(1 + \frac{R_4}{R_3}\right) (e_2 - e_1)$

As shown $e_0 = (e_2 - e_1)$

USING SYMETRICAL AMPLIFIERS TO REDUCE INPUT CURRENT (GENERAL CONCEPT)



MACROMODEL

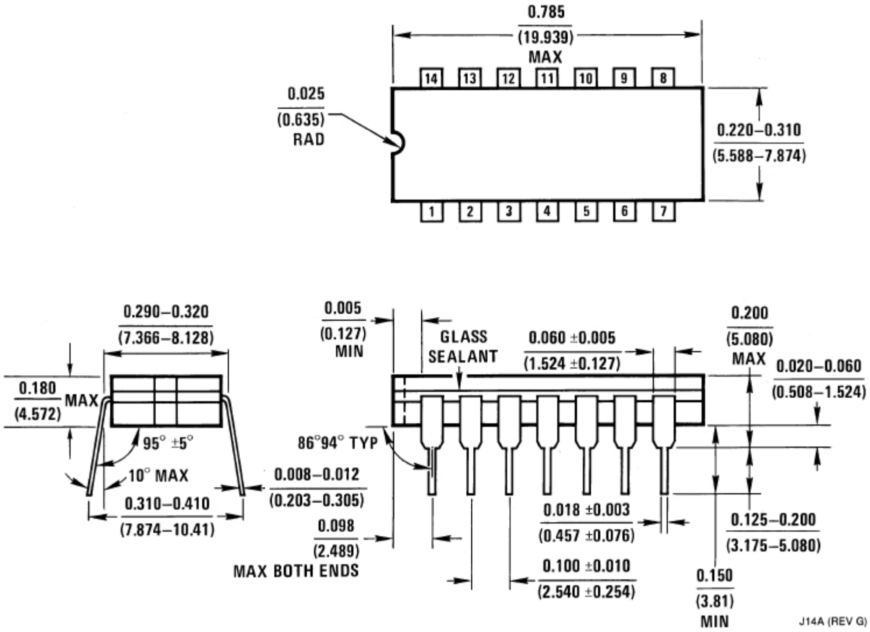
```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT LM124 1 3 2 4 5 (analog)
**********************************************************
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
 VOFP 12 13 DC 0
 VOFN 13 14 DC 0
 IPOL 13 5 1.000000E-05
 CPS 11 15 3.783376E-09
 DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS
```

ELECTRICAL CHARACTERISTICS

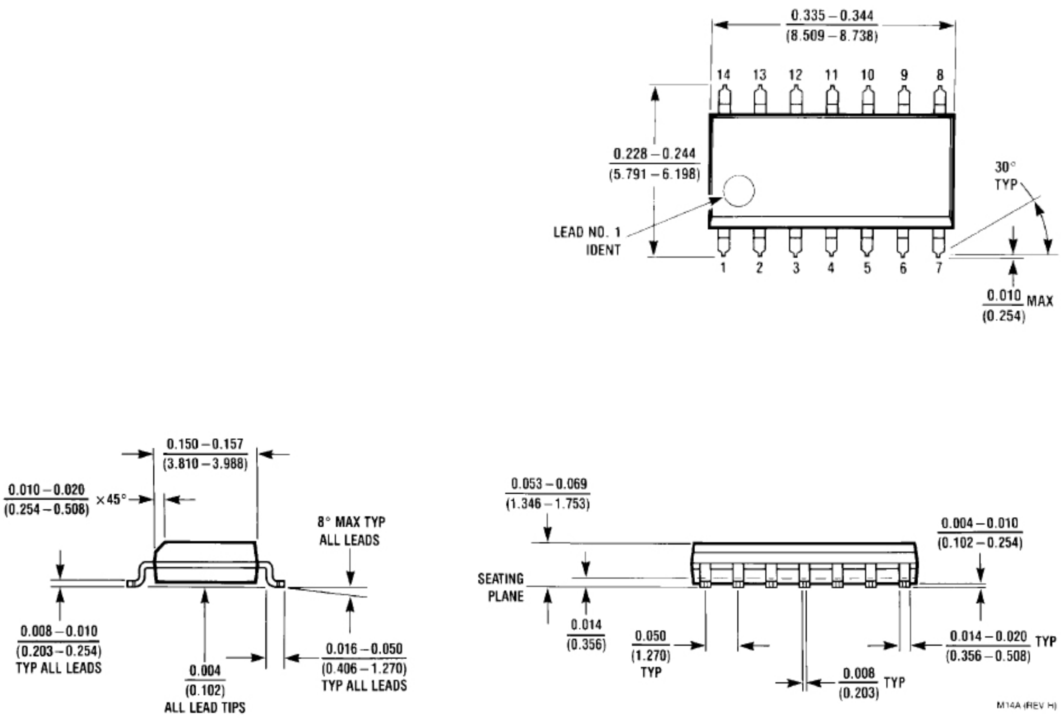
$V_{cc}^{+} = +15V$, $V_{cc}^{-} = 0V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 2k\Omega$	100	V/mV
I_{cc}	No load, per amplifier	350	µA
V_{icm}		-15 to +13.5	V
V_{OH}	$R_L = 2k\Omega$ ($V_{CC}^{+}=15V$)	+13.5	V
V_{OL}	$R_L = 10k\Omega$	5	mV
I_{os}	$V_o = +2V$, $V_{CC} = +15V$	+40	mA
GBP	$R_L = 2k\Omega$, $C_L = 100pF$	1.3	MHz
SR	$R_L = 2k\Omega$, $C_L = 100pF$	0.4	V/µs

Physical Dimensions inches (millimeters) unless otherwise noted

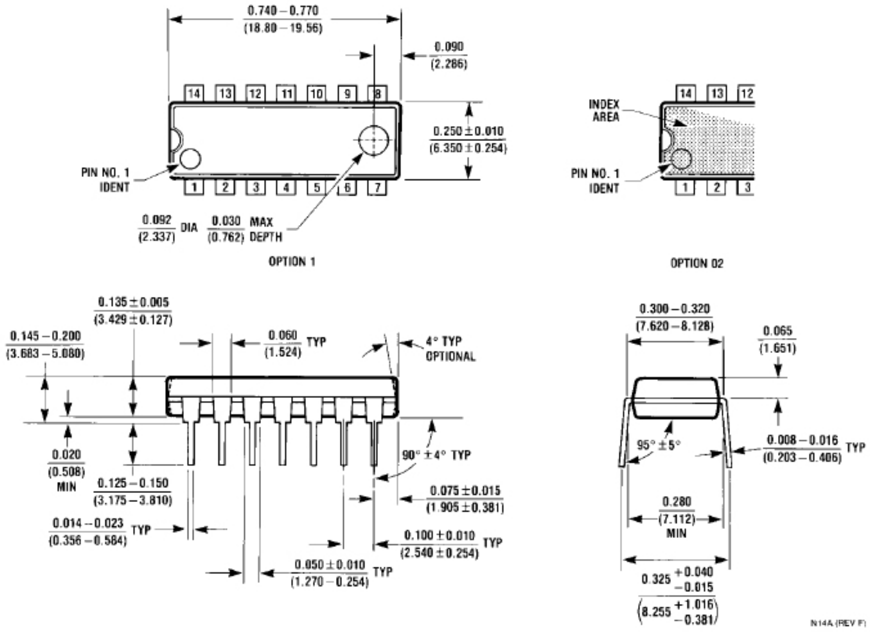


Ceramic Dual-In-Line Package (J)
Order Number JL124ABCA, JL124BCA, JL124ASCA, JL124SCA, LM124J, LM124AJ, LM124AJ/883, LM124J/883, LM224J, LM224AJ or LM324J
NS Package Number J14A

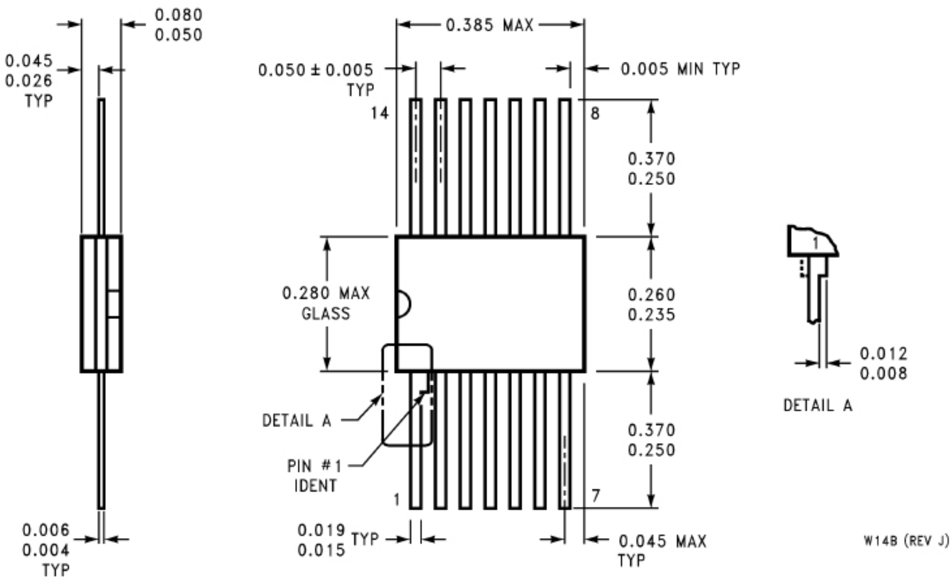


MX S.O. Package (M)
Order Number LM324M, LM324MX, LM324AM, LM324AMX, LM2902M or LM2902MX
NS Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

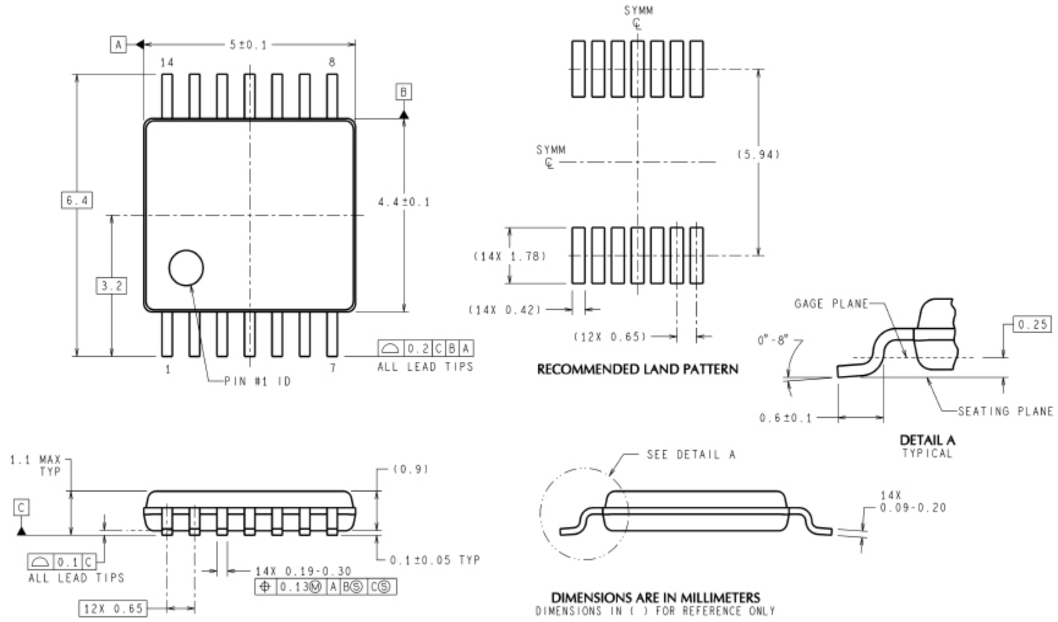


Molded Dual-In-Line Package (N)
Order Number LM324N, LM324AN or LM2902N
NS Package Number N14A



Ceramic Flatpak Package
Order Number JL124ABDA, JL124ABZA, JL124ASDA, JL124BDA, JL124BZA, JL124SDA, LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
NS Package Number W14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC14 (Rev D)

14-Pin TSSOP
Order NumberLM324MT or LM324MTX
NS Package Number MTC14

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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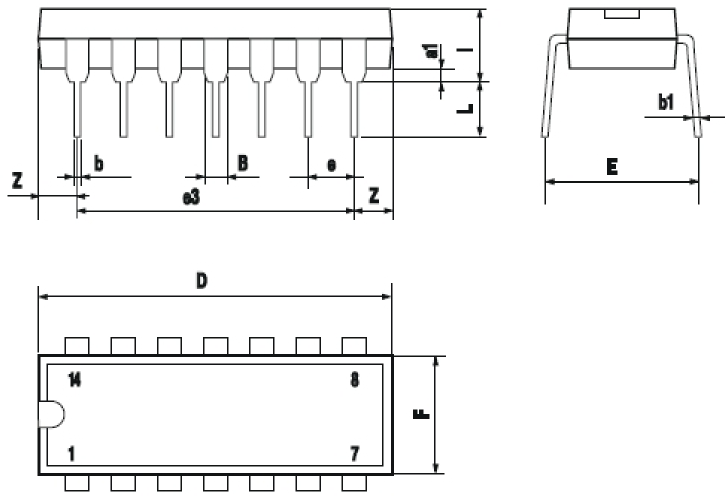
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560

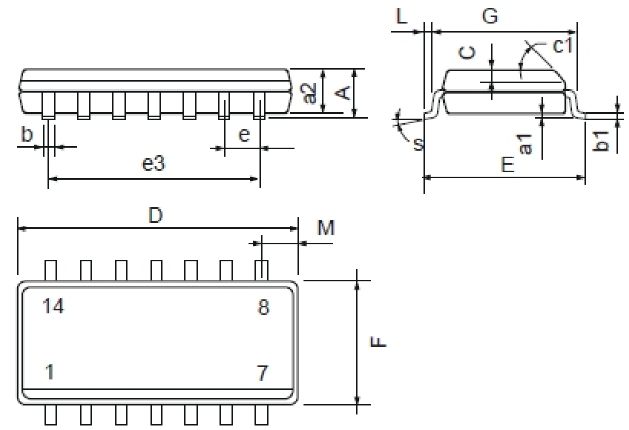
PACKAGE MECHANICAL DATA
14 PINS - PLASTIC DIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)

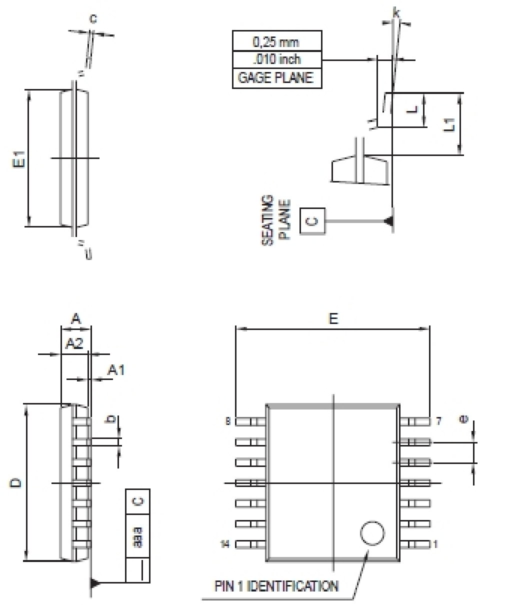


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

Note : (1) D and F do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.066 inc) ONLY FOR DATA BOOK.

PACKAGE MECHANICAL DATA

14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	4.90	5.00	5.10	0.192	0.196	0.20
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.00			0.039	
aaa			0.100			0.004