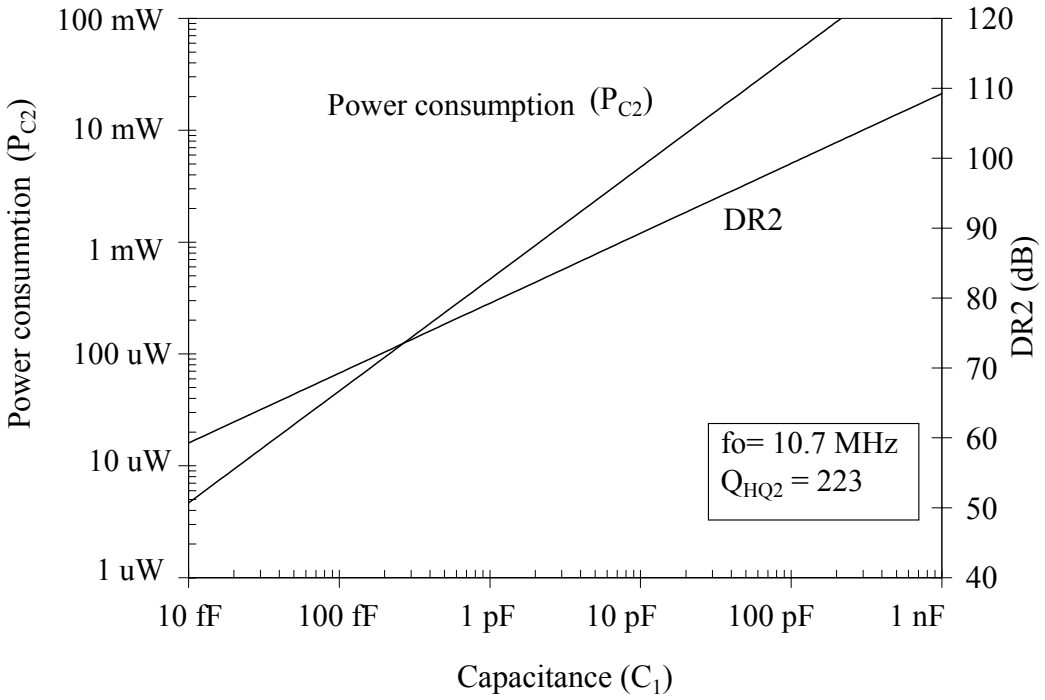

Figure 4.19 Preliminary interpolation of the power consumption (P_{C2}) and the dynamic range (DR2) of Technique 2 at 1% IM_3 versus C_1 at f_0 = 10.7 MHz and Q_{HQ2} = 223

4.9 High-Frequency Performance

High-frequency performance of the circuit will be limited by the transition frequency (f_T) of the transistor. Equation (3.9) suggests that a higher, more useful, center frequency can be expected using a smaller value of capacitor C_1 (e.g. using stray capacitances), a higher value of I_2 and a higher f_T (e.g. in the region of several GHz) of better transistors. For Techniques 1 and 2 described in Chapter 3, all transistors in Figures 3.2 and 3.3 are alternatively modeled by a better transistor BFR90A with higher f_T at 5 GHz (RF Transistor Data, Vishay Semiconductor GmbH. 1999), β = 120 and the bias currents $I_1 = I_2 = 1$ mA.

4.9.1 High-Frequency Simulation of Technique 1

Figure 4.20 shows high-frequency simulation of Technique 1 shown in Figure 3.2 through the analysis and the PSPICE simulations in terms of the center frequency f_{o1} and the quality factor Q_{HQ1} versus capacitance C_1. In Technique 1, Q_{HQ1} is maintained relatively high and the upper frequency is limited at approximately 600 MHz at C_1 = 1 pF.

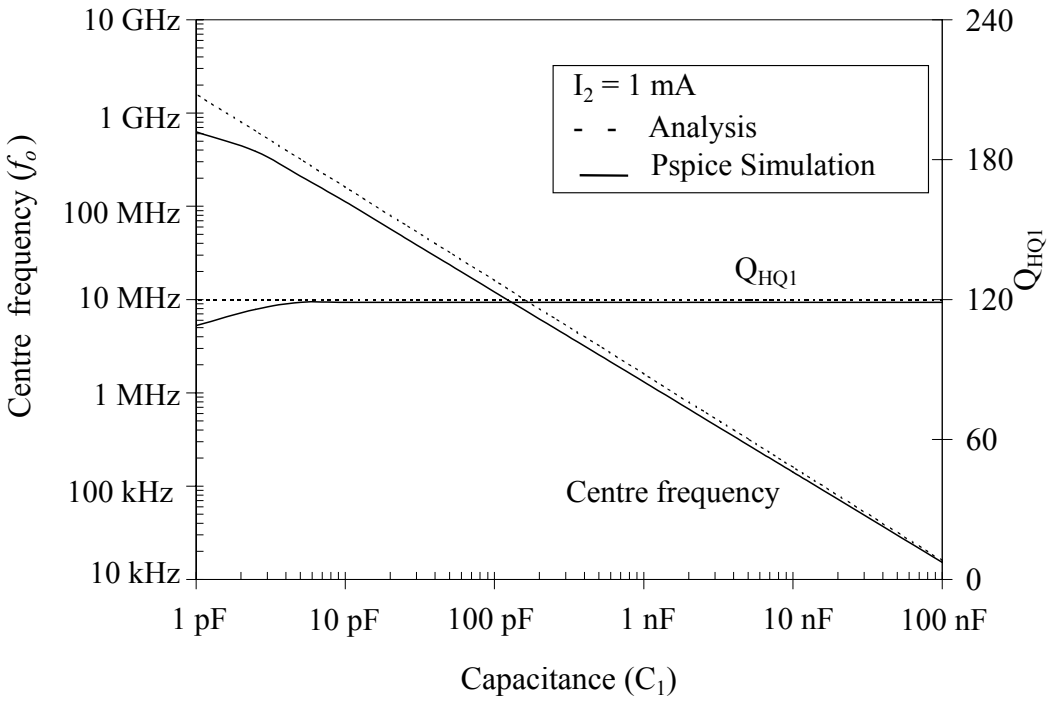

Figure 4.20 An example of the center frequencies f_0 and the quality factor Q_{HQ1} versus capacitance C_1 of Technique 1 shown in Figure 3.2.

4.9.2 High-Frequency Simulation of Technique 2

Similarly, Figure 4.21 illustrates high-frequency simulation of Technique 2 shown in Figure 3.3 through the analysis and the PSPICE simulation in terms of the center frequency f_{o2} and the quality factor Q_{HQ2} versus capacitance C_1. Both bias currents I_1 and I_2 are fixed at

1 mA and I_3 = 0.5 mA. In Technique 2, Q_{HQ2} is maintained relatively high and the upper frequency is limited at approximately 500 MHz at C_1 = 1 pF.

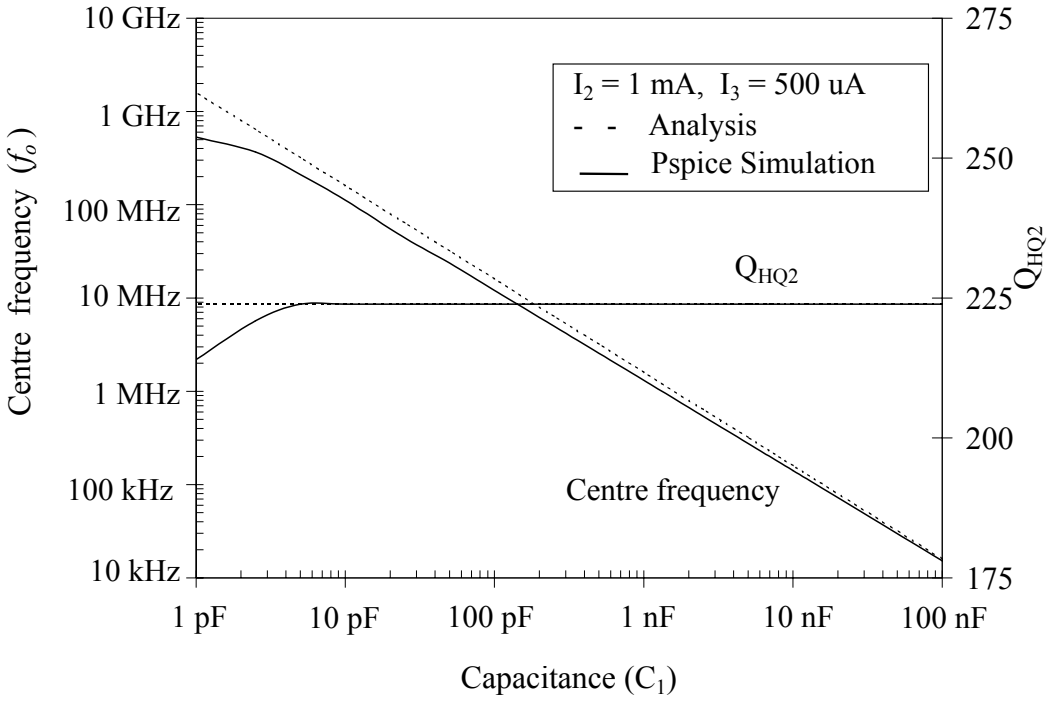

Figure 4.21 An example of the center frequencies f_0 and the quality factor Q_{HQ2} versus capacitance C_1 of Technique 2 shown in Figure 3.3.

4.10 Physical Layout Simulations

Figure 4.22(a) shows a physical layout of the circuit in Technique 1 which correspond to Figure 3.2. Figure 4.22(b) shows an exploded version of the layout of Technique 1 excluding capacitors C_1 and $2C_1$. Figure 4.23(a) shows a physical layout of the circuit in Technique 2 which correspond to Figure 3.3. Figure 4.23(b) shows an exploded version of the layout of Technique 2 excluding capacitors C_1 and $2C_1$. As a particular example, the layouts are modeled by 1.2μm N-well Technology of ORBIT Semiconductor. As shown in Figure 4.22 and 4.23, the circuit layout consists of NPN transistors, capacitors and resistors. A NPN transistor is formed by a P_BASE, N_WELL, N_SELECT, METAL1 and ACTIVE_AREA.

The P_BASE layer is an active area. The base contact is enclosed in N_SELECT. The emitter is an N_SELECT region. The collector is the entire P_BASE sitting in an N_WELL. A contact hole is modeled by a CONTACT, a METAL1 and an ACTIVE_AREA. The area of a NPN transistor is approximately 0.0385 mm(Width) × 0.0605 mm(Length) = 2.32925×10^{-3} mm^2. The β parameter obtained from measurements is 128.

A capacitor is formed by POLY and POLY_CAP1. The POLY_CAP1 surround the POLY everywhere; the area of the capacitor is the area of the POLY. POLY is physically on top of POLY_CAP1, so that contact to the POLY_CAP1 must be made in the region where it extends beyond the POLY. The area of the POLY of 1.9773×10^{-3} mm^2 result in the capacitor of 1 pF and the large area. A resistor is formed by POLY_R and METAL1. The area of the METAL1 of 69.75×10^{-6} mm^2 results in the resistor of 50 Ω. As shown in Figure 4.22 and 4.23, the area of the circuit layouts are approximately 1.12 mm(Width) × 0.90 mm(Length) = 1.008 mm^2 and 0.88 mm(Width) × 1.13 mm(Length) = 0.994 mm^2, respectively. The performance of the circuit layout has been simulated through parasitic extractions.

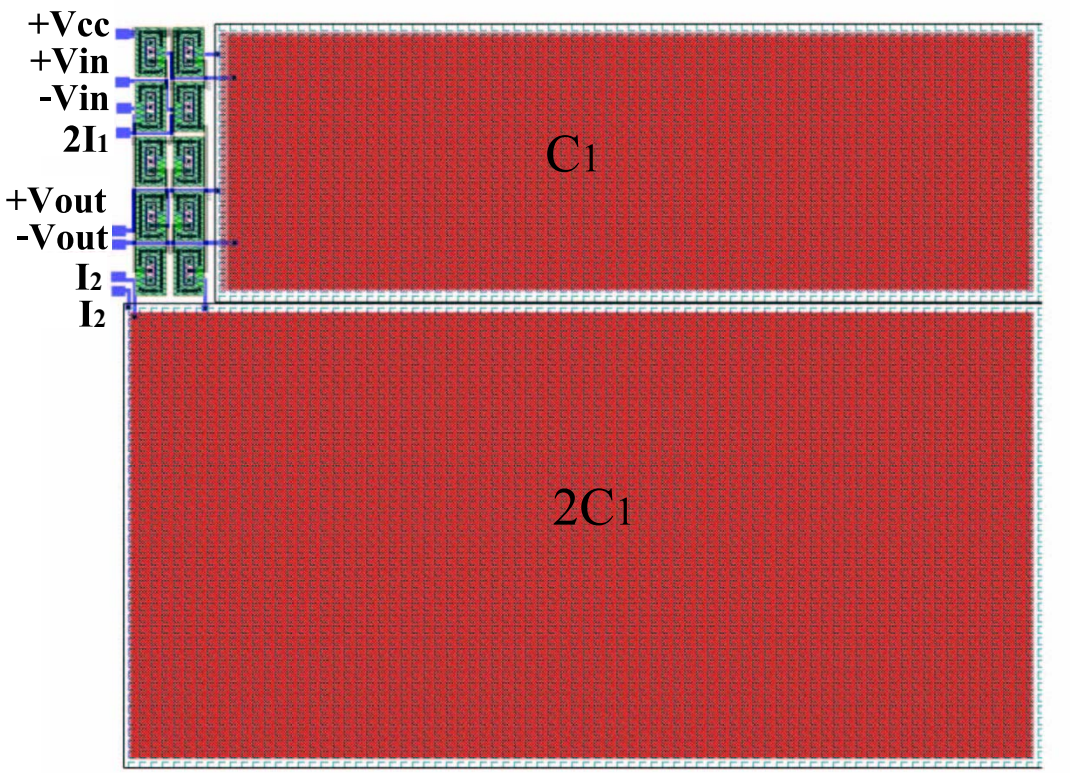

Figure 4.22 (a) The layout of Technique 1 shown in Figure 3.2 where C_1=*150 pF*