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Defect Distribution and Yield Analysis Technique on Silicon Wafer

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Abstract. This paper presents the defect distribution and yield analysis on silicon wafer. The generation and recombination lifetime were the key parameters and obtained from the current–voltage and the capacitance–voltage of diode characteristics for forward bias. Then 3D contour maps were plotted as defect distribution and can be analyzed for the whole wafer which is useful for the yield analysis of the defects that were caused from fabrication process.

Introduction

Currently, the semiconductor manufacturing consists of a sequence of various process steps. But some physical characteristics are not fully under the semiconductor manufacturing control, and should be noted that there are many variation of each of these process. The effect of variations in processing parameter on the performance of small geometry devices could be significant. All these areas may introduce defects in a device. These defects may cause the failure on each dice and decrease the yield of wafers [1,2]. All semiconductor companies aim to maximize wafer yield to reduce manufacturing cost. The higher test yield means gaining the faster time to profit.

The defect on the Silicon wafer can cause the leakage current which can be analyzed from generation and recombination lifetime [3] those are calculated from the current–voltage (I-V) and the capacitance–voltage (C-V) characteristic [4], and analyze with derivative technique [5].

Experiment Details

Preparation. In this study, we use the standard diode which is made from 0.8 μm CMOS standardized electronics device processing150 mm of 5 Ω-cm of P-Silicon substrate.N-well was built from Phosphorus implantation at $4x10^{12}$ ion/cm^2 with energy 140 keV. For n^+ was built from Arsenic $5x10^5$ ion/cm^2 with energy 50 keV. And p^+ region was built from Boron $3x10^{15}$ ion/cm^2 with energy 40 keV. Finally, the boundary junction will be connected to the metal.

The basic structure of diode according to the geometry type, we can define into 2 structure types. Table 1 is the geometry description of Large Area Diode and Meander Diode. These parameters will be used for next section.

Measurement method. The current–voltage (I-V) characteristic of each diode was measured from forward bias with 0.01 V step from 0 to 1 V. The Voltage applied on n+ and measured the current at p+. The measurement was controlled at 300K in the black box. For the capacitance–voltage (C-V) characteristic was measured on the same diode with 100 kHz signal at 300K.

Table 1 The geometry description of each diode

Diode Type	Area (cm^2)	Perimeter (cm)
Large (LA) (p^+ - N_{well})	$8x10^{-4}$	0.12
Meander (ME) (p^+ - N_{well})	$8x10^{-4}$	$4.04x10^{-4}$

Results and Discussion

In order to studying the leakage current analysis in diode, Large Area and Meander Diode were built on the Silicon wafer per table 1. And the summary of forward bias current (I_F) at p-n junction is consist of geometry elements, these are area leakage current and perimeter leakage current per Eq. 1. [6]

$$I_F = I_A + I_P = AJ_A + PJ_P \tag{1}$$

where J_A is area current density that related with diode area (A). For J_P is perimeter current density that related with diode perimeter (P).

And J_A can be extracted to 2 physical elements. The first is area generation current densityand area diffusion current density per Eq. 2.

$$J_A = J_{dA} + J_{rbA} \tag{2}$$

From Ideal diode equation (Shockley diode equation)

$$I = I_0[\exp(qV/kT) - 1] \tag{3}$$

where I_0 is the saturation current (A), q is electron charge (1.602×10^{-19} C), k is Boltzmann's constant (8.617×10^{-5}eV/K), T is absolute temperature (K)

By substituting current in Eq. 3 with area current density, the result is saturation area current density as Eq. 4.

$$J_{A0} = \frac{J_A}{[\exp(qV/kT) - 1]} \tag{4}$$

From Eq. 4, the relation between saturation area current density and forward bias voltage shows as Fig 1. At low bias voltage (less than 0.1 V), J_{A0} is controlled by recombination current. When voltage is between 0.1 – 0.4 V, area diffusion current density will perform J_{dA}. And estimate the J_{dA} as a linear from 0.1 - 0.4 V at V= 0V, the result of J_{dA} is 63 pA/cm^2.

Typically, the value J_A can be written as

$$J_A = J_{dA} + \left\{ \left[qn_i W_A \Big/ 2\tau_r \exp\left(\frac{qV}{2kT}\right) + \tau_g \right] . [\exp(qV/kT) - 1] \right\} \tag{5}$$

where n_i is the charge carrier density in intrinsic semiconductor (cm^{-3}) and W_A is area depletion region width (cm)

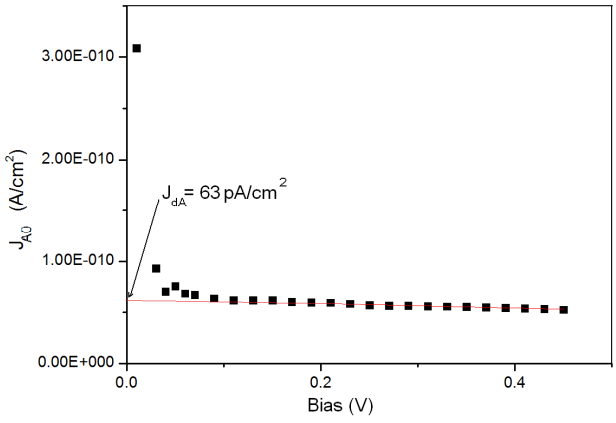

Fig 1. The relation between area current density and forward bias voltage

The area current density is depended with the depletion region width and area diffusion current. So the calculation of τ_r and τ_g will be discussed later.

With the same scenario as current element, the capacitance at the junction C_j is the summary of 2 linear elements by

$$C_j = AC_A + PC_P \tag{6}$$

where C_A is area capacitance density which related with diode area (A). C_P is perimeter capacitance density (F/cm) which related with diode perimeter (P) (F/cm^2).

Typically, junction capacitance (C_j) is measured by the response of small signal across DC voltage. Area capacitance density (C_A) and perimeter capacitance density (C_P) can be assumed to summarize as Eq. 6.

Generation lifetime is depended on depletion region width and area current density. The depletion region width can be gathered from area capacitance density (C_A)

$$W_A = \frac{k_{si}\varepsilon_o}{C_A} \tag{7}$$

where k_{si} is Silicon's dielectric constant (=11.8) and ε_0 is vacuum permittivity (=8.854x10^{-14} F/cm).

From equation, saturation area recombination current density J_{rbA0} is J_{A0} - J_{dA} which can be calculated from Eq. 5. The result after arrange the form is Eq. 8.

$$\frac{qn_iW_A}{J_{rba0}} = 2\tau_r \exp(qV/2kT) + \tau_g \,. \tag{8}$$

Figure 2 shows the relation between qn_iW_A/J_{abr0} and exp($qV/2kT$). So τ_r and τ_g can be calculated from slope and y-intercept ($qn_iW_A/J_{abr0}= 0$) respectively.

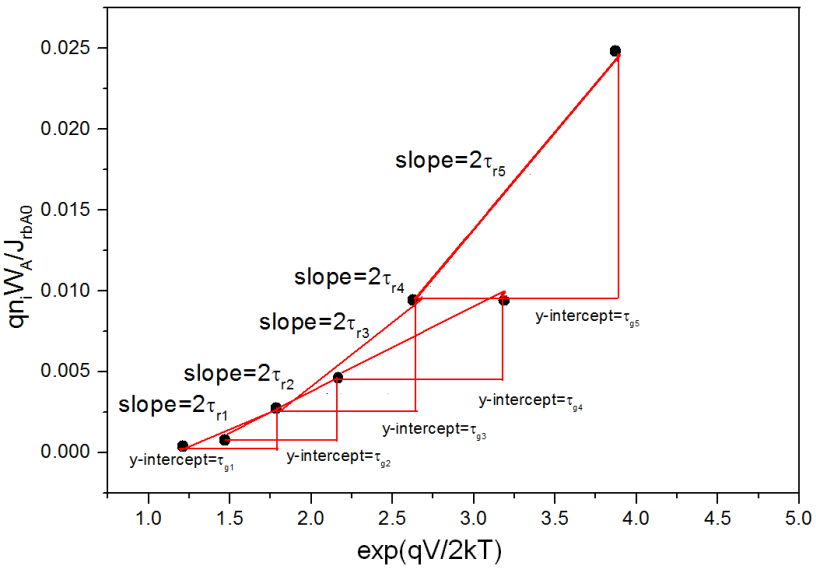

Fig 2. The relation between qn_iW_A/J_{abr0} and exp($qV/2kT$)

After we gathered τ_r and τ_g value for each point, Average value will be used to calculate, and we obtained τ_r = 367.2 μs and τ_g = 11.879 ms.

From the above data is the value for only 1 sample dice. Then, do the collecting the data for 125 dices, and show the result as 3D graph. So the distribution of generation lifetime and recombination lifetime are shown in Fig.3 and Fig.4. The result is this Silicon wafer is non-uniform defect because generation and recombination lifetime is not the same level for whole wafer.

This non-uniformed defect distribution can be occurred from ion-implantation and annealing process which the new reforming of Phosphorus cluster at n-well is not completed. It looks like the random defect. That affects to wafer yield loss due to higher leakage current.

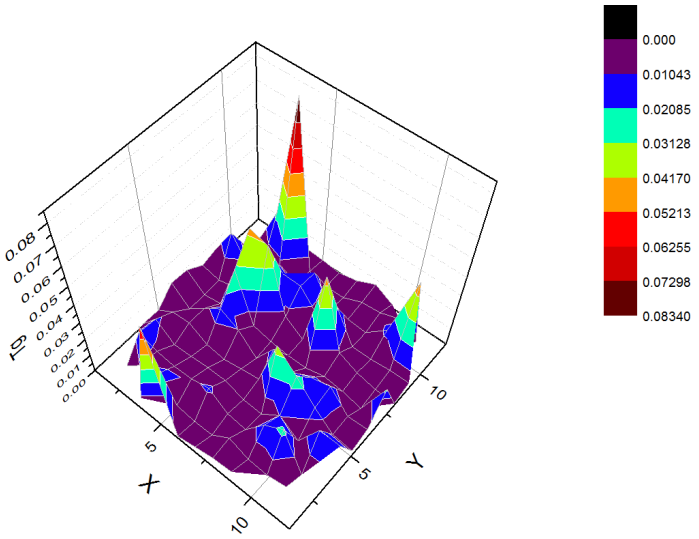

Fig 3. The distribution of τ_g on the Silicon wafer.

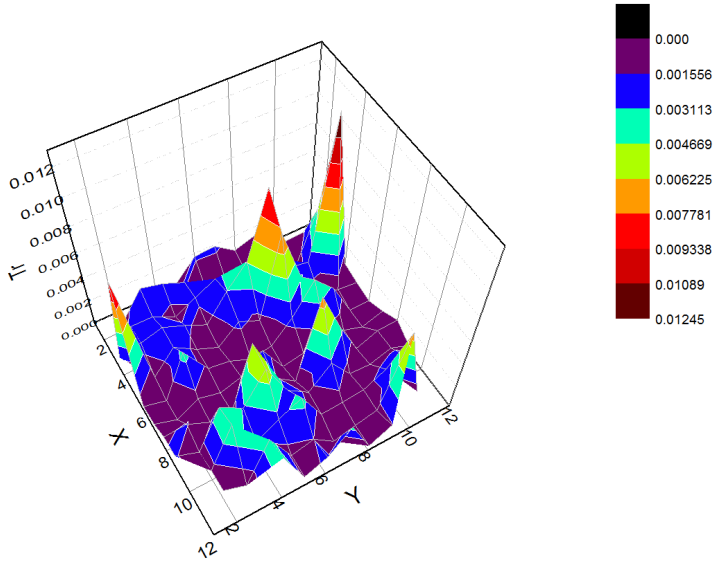

Fig 4. The distribution of τ_r on the Silicon wafer.

Summary

According to generation and recombination lifetime which calculated from derivative technique and show as 3D graph, can analyze the non-uniformity of the defect distribution on silicon wafer. For the dices which lifetime is higher, that means the leakage current is higher than other area and may cause of the yield loss on the wafer. So, the other parameter will be considered for the total yield calculation.

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