Research Title: Defect and Yield Analysis of Electronics Devices on Silicon Wafer
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ABSTRACT

This research presents the technique for the defect and yield analysis of electronics devices on silicon wafer. The defect distribution for p-n junctions of diodes on silicon wafer were used the derivative technique. Electronic devices fabricated with 0.8 μm standard CMOS fabrication process. Next, the current - voltage and the capacitance – voltage of diode characteristics for forward bias were measured. The generation and recombination lifetime were obtained by using the derivative technique analysis. Then, the result was shown as the defect distribution with 3D contour map which is useful to the study of the defect or the leakage current that obtained from ion implantation process in p-n junctions.

Keywords : p-n junctions, leakage current, defects, generation and recombination lifetime, CMOS Technology