

Thesis Title	A low-power eighth-order bandpass sigma-delta modulator.
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ABSTRACT

This thesis describes the design of a low-power eighth-order bandpass sigma-delta modulator for analog to digital conversion in a digital-IF receiver. The modulator comprises switched-capacitor resonators, dynamic latch comparator and digital to analog converter connected in a negative-feedback loop. The bandpass sigma-delta modulator is implemented with discrete time circuits and double sampling technique in a 0.35 μm CMOS technology. It works at 1.5 volts of supply voltage and was simulated by Spectre Cadence.