

Sittiporn Prabhavat 2014: A Performance Improvement of a Circuit Fault Simulation Using Parallel Processing. Master of Engineering (Computer Engineering), Major Field: Computer Engineering, Department of Computer Engineering. Thesis Advisor: Associate Professor Pradondet Nilagupta, M.Eng. 49 pages

We use parallel processing technique for finding Stuck-at fault in the ISCAS85 benchmark for combinational circuit and ISCAS89 benchmark for sequential circuit. We modify HOPE Program for simulate both of ISCAS85 and ISCAS89 in fault simulation.

The result of a simulation using 2 and 4 processors gives a speed up between 1.5 - 3 and about 4 using 8 and 16 processors. Circuit Problem Size and Fault List Size are two factors for using Parallel Computing. We find that the number of a test vectors, the number of outputs and the number of a fault list affect the speed up of a computation. Speed up is good when circuit problem size is over 10000. It means that a large circuit problem size has more speed up and efficiency than a small circuit problem size. We compare the two circuits that have a similar circuit problem size. We find that a large number of a fault list spends more time than a circuit which has a less number of a fault list.

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Student's signature

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Thesis Advisor's signature