

Thesis Title	Theory and Applications of CMOS Analog Four-Quadrant Multiplier
Student	Mr. Thitipong Busabongkrose
Thesis Advisor	Assoc.Prof.Dr. Kobchai Dejhan
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Department	Telecommunication Engineering King Mongkut's Institute of Technology Ladkrabang
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Abstract

This thesis proposes theory and applications of CMOS analog four-quadrant multiplier. All circuit have been improved for obtaining the better performances by using MOSFET. Two methods are presented. The first multiplier is based on the current/voltage characteristic of MOS transistors operating in the triode region which has the simple configuration with four shunt feedback buffers and four NMOS transistor. The second multiplier is based on the current/voltage characteristic of MOS transistors operating in the saturation region which consists of four two-transistor differential amplifier, four NMOS transistor and additional for two signal summing circuits which is implemented from differential pairs and current mirror. The proposed CMOS analog four-quadrant multipliers have a wide dynamic range and good linearity. Experimental results and simulation results by PSpice program are given to demonstrate the performances of the proposed circuits which are expected to be useful in analog signal processing applications. The frequency doubler and balanced modulator are presented as its applications.