Thesis Title	Design Techniques of MOS Analog Multiplier Circuit
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Abstract

This thesis presents two techniques employed in the design of MOS analog multiplier. The first design is a CMOS triode analog multiplier which two transistors operated in the triode region are used. This design circuit consists two parts. The first part uses scaled floating voltage subcircuit and regulated voltage subcircuit. The second part uses scaling voltage circuit. This part is a CMOS saturation analog multiplier circuit that uses differential coupled pairs circuit as the main design. Other two subcircuits, namely, the level shifter and the voltage scaling are additionally used. The results of performance are shown by PSpice program. It's frequently responsed that CMOS operating in triode region is better than CMOS operating in saturation region and the number of device is less. Both of the circuits have good linearity but the dynamic range is wider than the former research.