A New Versatile Precision Rectifier

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Dear Prof. Ray,

I would like to thank you and the reviewers for the valuable comments. I tried my best to correct our manuscript to fulfill the requests of reviewers. Please find the manuscript after correction to be reviewed and also find below a summary how I addressed the comments of the reviewers.

Thank you in advance.

Best Regards,
Montree Kumngern

COMMENTS FOR THE AUTHOR

Reviewer # 1

I would like to thank the Reviewer #1 for his kindness.

Reviewer # 5

The following are the comments I would like to make on this revised paper

1.) Based on the previous corrections, If Rin is going to be external, then MR1 and MR2 need not be shown in the circuits as this may confuse the readers.

I would like to thank the Reviewer # 5 for his advices.

For this comment, I was improved by replacing MR1-MR2 with a symbol of Rin and used Fig. 2(b) for MOS resistor Rin.

2.) It looks like the reference name in [34] is not correct.

I was corrected.

3.) The author can compare the performance of this work with the previous works.

The table 3 for comparison was added.

A new versatile precision rectifier

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Abstract

This paper presents a versatile precision rectifier. The circuit yields a positive half-wave signal, a negative half-wave signal, a positive full-wave signal and a negative full-wave signal into one single structure. The PSPICE simulation is performed to examine the performance of the new circuit. The experimental result is also confirmed workability of the proposed circuit.

Keywords:

Precision rectifier, full-wave rectifier, half-wave rectifier, current-mode circuit, nonlinear circuit, analog signal processing

1. Introduction

In a conventional rectifier, diodes are simply used for rectification. However, it has generally been acknowledged that such a circuit is incapable of rectifying incoming signals whose amplitudes are less than the cut-in voltage (e.g., approximately 0.7 V for the silicon diode and 0.3 V for the germanium diode). Therefore, diode-only rectifiers are normally used in applications in which the precision in the range of cut-in voltage is of less importance, such as RF demodulators and DC voltage supply rectifiers. The precision rectifier is an important circuit building block that is widely used in various applications, such as in wattmeters, AC voltmeters, function fitting, triangular-wave frequency doubling, error measurements, RMS to DC conversions, and peak detectors to floor detectors in ultrasonic. As a result, a number of precision rectifiers have been introduced in the technical literature [1]-[38]. In [1]-[9], several precision rectifiers using operational amplifiers (op-amps), diodes and resistors have been proposed. However, op-amp-based circuits typically utilize excessive external passive components, many of

which are floating components. Moreover, the classical problem of the rectifier using op-amps is that during the non-conduction/conduction transition of the diodes, the op-amps must recover with a finite small-signal dv/dt (slew rate) [10]. The result of this effect is an output distortion in the crossover region, known as 'corner distortion'. Thus, the op-amp-based rectifiers are restricted to a frequency performance well below its gain-bandwidth product. This problem is reduced by designing the rectifier using a current-mode technique [10]. Several current-mode precision rectifiers have been introduced [10]-[23]. These circuits provide the attractive feature of high precision rectification. However, some of these circuits either require an ungrounded resistor, which is not ideal for integrated circuit (IC) implementation, or suffer from high frequency limitation. In addition, the rectifiers in [10]-[13] also require two identical current conveyors. Mismatch of these current conveyors affects the output waveform of full-wave format, i.e., the amplitude of the first polarity signal may not be equal to that of the second polarity signal. Other rectifiers using operational transconductance amplifiers (OTAs) [24]-[30] provide the attractive feature of IC implementation, some of which nevertheless suffer from the use of a large number of active components and limitation to the high frequency performance (i.e., [28], [29]).

To achieve the high operating frequency, the current-mode class-AB rectifiers were used in [31]-[34]. Although this technique requires the signal current to be four times as large as the bias current in order to avoid the square-law error of the transistors, the precision and the operating frequency of class-AB rectifier can be obtained approximating from the quiescent current [34]. In addition, the rectifiers using all-MOS transistors proposed in [35]-[37] are very suitable for CMOS technology implementation. It should be noted from the rectifiers [1]-[37] that the circuits in [1]-[33] are the full-wave rectifiers while the circuits in [34]-[37] are the half-wave rectifiers. Only the rectifier in [38] can provide both half-wave rectification and full-wave rectification into one single topology; however, this scheme is unfit for operation in high frequency.

In this paper, design of the versatile precision rectifier which can realize both half-wave and full-wave signals is presented. The proposed circuit provides both high precision rectifier and high frequency performance. The positive half-wave, negative half-wave, positive full-wave and negative full-wave rectifiers can be obtained in one single structure. PSPICE simulations are performed for the verification of the circuit. The

experimental results are included for the sake of completeness and to confirm workability of the proposed circuit.

2. Circuit Realization

The proposed versatile precision rectifier is shown in Fig. 1. It consists of three main components: the voltage-to-current (V-I) converter, the current-mode class-AB rectifier cell, and the current-to-voltage (I-V) converter. The V-I converter is composed of a second generation current conveyor (CCII) and a resistor R_{in} as shown in Fig. 2. The class-AB precision rectifier cell comprises transistors MD_1 to MD_4, current sources I_1 to I_8, and current mirrors CM_1 to CM_6. The resistors R_{o1} to R_{o4} are operated as the I-V converters The operation of the V-I converter is as follows: when input voltage V_{in} travels into the circuit, it is converted into a current i_z by CCII and resistor R_{in} (MR_1-MR_2). Assume that MR_1 and MR_2 are matched and operated in saturation regions, the resistance value can be determined by [39]

$$R_{in} = \frac{1}{2K\left(V_{DD} - V_{TH}\right)} \tag{1}$$

where $K = \mu C_{ox}\left(W/L\right)$ is the transconductance parameter, V_{TH} the threshold voltage, V_{DD} the supply voltage ($V_{DD} = |V_{SS}|$), μ the carrier mobility, C_{ox} the gate capacitance per unit area, W the channel width, and L the channel length. The terminal relations of CCII are determined by $i_y = 0$, $v_x = v_y$, and $i_z = i_x$ [40]-[43]. Using these relations, the current i_z can be obtained as

$$i_z = \frac{V_{in}}{R_{in}} \tag{2}$$

The current i_z will be applied into the input of current-mode class-AB precision rectifier. The transistor MD_2 and the current source I_1 generate a constant voltage V_A to provide a bias voltage for transistor MD_1 while transistor MD_4 and the current source I_2 generate a constant voltage V_B to provide a bias voltage for transistor MD_3 [16]. The constant voltages V_A and V_B should be fairly close to the respective threshold voltages of

transistors MD_1 and MD_3 to obtain precision results. V_A and V_B cause MD_1 and MD_3 to operate in class-AB. The current sources I_3 and I_4 are supplied to the current mirrors CM_1 to CM_6 to ensure that these current mirrors are continuously on and thereby improve the frequency response and the overall system linearity.

The operation of the proposed half-wave rectifier is as follows: when $i_z < 0$, it is fed through MD_1 and then is mirrored by CM_1 to the drain of MC_2 as I_{o1} $(+i_z)$. On the other hand, when $i_z > 0$, it is fed through MD_3 and then is mirrored by CM_2 to the drain of MC_4 as I_{o2} $(-i_z)$. From the operation of the proposed circuit, the relations between the input current i_z and the output currents I_{o1} and I_{o2} can be expressed as

$$i_z < 0 \,;\, I_{o1} = +i_z + I_1 + I_3 \tag{3}$$

$$i_z > 0 \,;\, I_{o2} = -i_z + I_2 + I_4 \tag{4}$$

As the current sources I_5 and I_6 respectively compensate the offset currents $I_1 + I_3$ and $I_2 + I_4$, the relations between i_z and the currents I_{Ro1} and I_{Ro2} can be expressed as

$$i_z < 0 \,;\, I_{Ro1} = +i_z \tag{5}$$

$$i_z > 0 \,;\, I_{Ro2} = -i_z \tag{6}$$

where I_{Ro1} and I_{Ro2} are the currents flowing through the resistors R_{o1} and R_{o2}, respectively. Letting $R_{o1} = R_{o2} = R_{in}$ and using Equation (2), the relation between the input and the output voltages of half-wave rectifier can be obtained as

$$V_{in} < 0 \,;\, V_{H+} = V_{in} \tag{7}$$

$$V_{in} > 0 \,;\, V_{H+} = 0 \tag{8}$$

$$V_{in} < 0 \,;\, V_{H-} = 0 \tag{9}$$

$$V_{in} > 0 \,;\, V_{H-} = -V_{in} \tag{10}$$

From Equations (7) to (10), it can be seen that the proposed circuit provides both a positive half-wave rectifier and a negative half-wave rectifier. It is also evident from Equations (7) to (10) that the temperature effect is non-existent due to the absence of V_{TH} and μ.

The operation of full-wave rectifier can be explained by the continuous operation of the half-wave rectifier. Its operation is as follows: when $i_z < 0$, it is fed through MD_1

and then is mirrored by current mirror CM_1 to the drain of MC_5 as $+i_z$. This $+i_z$ is second mirrored by CM_5 to the drain of MC_8 as $-i_z$ and this $-i_z$ is third mirrored by CM_3 to the drain of MC_{10} as I_{o3} $(+i_z)$. Conversely, when $i_z > 0$, it is fed through MD_3 and then is mirrored by CM_2 to the drain of MC_6 as $-i_z$. This $-i_z$ is again mirrored by CM_4 to the drain of MC_{10} as I_{o3} $(+i_z)$. From the operation of the circuit, the relation between the input current $(+i_z)$ and the output current to the drain of MC_{10} (I_{o3}) can be expressed as

$$i_z > 0 \;;\; I_{o3} = +i_z + I_1 + I_2 + I_3 + I_4 \tag{11.1}$$

$$i_z < 0 \;;\; I_{o3} = +i_z + I_1 + I_2 + I_3 + I_4 \tag{11.2}$$

Since the current source I_7 compensates the offset current $I_1 + I_2 + I_3 + I_4$, the relation between i_z and I_{Ro3} is $I_{Ro3} = i_z$, where I_{Ro3} is a current flowing through the resistor R_{o3}. Letting $R_{o3} = R_{in}$ and using Equation (2), the relation between V_{in} and V_{F+} can be expressed as

$$\left.\begin{array}{l} V_{in} < 0 \;;\; V_{F+} = +V_{in} \\ V_{in} > 0 \;;\; V_{F+} = -V_{in} \end{array}\right\} \tag{12}$$

Again, when $i_z < 0$ it is fed through MD_1 and then is mirrored by current mirror CM_1 to the collector of MC_{12} as $+i_z$. This $+i_z$ is again mirrored by CM_6 to the drain of MC_{16} as I_{o4} $(-i_z)$. In contrast, when $i_z > 0$, it is fed through MD_3 and then is mirrored by current mirror CM_2 to the drain of MD_{11} as $-i_z$. This $-i_z$ is second mirrored by CM_4 to the drain of MC_{14} as $+i_z$, and this $+i_z$ is third mirrored by CM_6 to the collector of MC_{16} as I_{o4} $(-i_z)$. From the operation of the circuit, the relation between the input current $(-i_z)$ and the output current I_{o4} can be expressed as

$$i_z < 0 \;;\; I_{o4} = -i_z + I_1 + I_2 + I_3 + I_4 \tag{13.1}$$

$$i_z > 0 \;;\; I_{o4} = -i_z + I_1 + I_2 + I_3 + I_4 \tag{13.2}$$

Since the current source I_8 compensates the offset current $I_1 + I_2 + I_3 + I_4$, the relation between i_z and I_{Ro4} is $I_{Ro4} = i_z$, where I_{Ro4} is a current flowing through the resistor

R_{o4}. Letting $R_{o4} = R_{in}$ and using Equation (2), the relation between V_{in} and V_{F-} can be expressed as

$$\left.\begin{array}{l} V_{in} < 0 \;\; ; \;\; V_{F-} = -V_{in} \\ V_{in} > 0 \;\; ; \;\; V_{F-} = +V_{in} \end{array}\right\} \tag{14}$$

According to Equations (12) and (14), the proposed circuit can operate as a positive full-wave rectifier and a negative full-wave rectifier. Moreover, the full-wave rectifier provides good temperature stability as there is no temperature effect due to the absence of V_{TH} and μ. It is evident from Equations (7)-(10), (12) and (14) that the proposed rectifier in Fig. 1 can perform as a positive half-wave rectifier, a negative half-wave rectifier, a positive full-wave rectifier and a negative full-wave rectifier within the same configuration. It should also be noted that if only half-wave rectifier is required, the circuit should consist merely of CCII, MD_1 to MD_4, MC_1 to MC_4, I_1 to I_6, R_{in}, R_{o1}, and R_{o2}. In addition, if only full-wave rectifier is required, the circuit should consist of CCII, MD_1 to MD_4, MC_1, MC_3, MC_5 to MC_{16}, I_1 to I_4, I_7, I_8, R_{in}, R_{o3}, and R_{o4}.

3. Circuit Performance

The ideal circuit performance so far has been based on the assumptions that the current conveyor has no tracking errors, that current mirrors have unity gain, and that MOS transistors are perfectly matched. However, in a practical realization, several non-idealities that cause deviation from the ideal performance are presented. The major factors to consider in this paper are non-ideal effects of the CCII, non-ideal effects of the class-AB rectifier cell, and non-ideal effects of the current mirror.

3.1 Non-ideal effects of the CCII

The proposed rectifier is analyzed by taking into account the non-idealities of a CCII. The non-ideal CCII characteristics can be accounted for by letting $v_x = \beta v_y$, $i_z = \alpha i_x$ and $i_y = 0$, where $\beta = 1 - \varepsilon_v$ and ε_v ($|\varepsilon_v| << 1$) represents the voltage tracking error from y to x terminals, and $\alpha = 1 - \varepsilon_i$ and ε_i ($|\varepsilon_i| << 1$) represents the current tracking error from x to z terminals. Taking the voltage and current tracking errors into consideration, the current i_z can be expressed as

$$i_z = \frac{\alpha\beta V_{in}}{R_{in} + R_x} \tag{15}$$

where R_x is the parasitic resistance obtained by looking into the terminal x of the CCII. When the CCII in Fig. 2 is simulated by PSPICE simulators, the parameters α=0.998, β=0.999 and R_x =1.1 kΩ are obtained and the simulated results are presented in Table 1. To investigate this case, the CCII in Fig. 2 was designed using TSMC 0.18 μm n-well CMOS parameter [43] and aspect ratios as shown in Table 2. For this simulation, resistor R_{in} is removed and the body of each of the transistors M_1 and M_2 is connected to V_{SS}, while the body of each of the transistors M_3 and M_4 is connected to its source. From Table 1, the CCII provides wide bandwidth. This parameter will be supported the high operating frequency of the proposed rectifier.

3.2 Non-ideal effects of the current mirrors

Let us assume from the circuit in Fig. 1 that the body of each of the transistors MC_1 to MC_{16} is connected to its sources, and thus the operation of the current mirrors CM_1 to CM_6 is insensitive to the variation of the threshold voltage caused by the body effect. However, the current mismatch should be considered.

Assume that the current i_{in} is the current reference that flows through input transistor, and the current i_o are the output current that is mirrored by output transistor of current mirror. Hence, the relation of i_o and i_{in} that includes the channel-length modulation effect can be written as

$$i_o = i_{in}\left(\frac{K_o}{K_i}\right)\left(\frac{V_{GS} - V_{THo}}{V_{GS} - V_{THi}}\right)^2\left(\frac{1+\lambda V_{DSo}}{1+\lambda V_{DSi}}\right) \tag{16}$$

where K_o and K_i are the transconductance parameters of the output and the input devices, respectively, V_{GS} is the gate-source voltage of any transistors, V_{THo} and V_{DSo} are respectively the threshold voltage and the drain-source voltage of output devices, V_{THi} and V_{DSi} are respectively the threshold voltage and the drain-source voltage of input devices, and λ is the channel-length modulation parameter.

Assume that all of the physical parameters such as V_{TH}, μ, C_{ox}, etc., of current mirror are identical, Equation (16) can be written as

$$i_o = i_{in}\left(\frac{(W/L)_o}{(W/L)_i}\right)\left(\frac{1+\lambda V_{DSo}}{1+\lambda V_{DSi}}\right) \tag{17}$$

If $V_{DSi} = V_{DSo}$, then the current gain of the current mirror is $(W/L)_o/(W/L)_i$. Additionally, if the transistors are identical, $(W/L)_o = (W/L)_i$, and therefore $i_o = i_{in}$. The current gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. This current gain will effect to the amplitude of the output voltage signals and the DC output offsets of the circuit.

On the other hands, the channel-length modulation effect can be considered by assuming that $(W/L)_o = (W/L)_i$ and λ is the same of both transistors. From Equation (18), differences in drain-source voltages (V_{DSi}, V_{DSo}) of the two transistors can cause a deviation the ideal unity current mirroring. A good current mirror should have identical drain-source voltage and a high output resistance, which can be achieved using large channel length.

Mismatch between the parameter K and offset between the V_{TH} of the two transistors are considered. Let us assume that the *W*/*L* ratios of the two mirror transistors are equal but that K and V_{TH} may be mismatched. In this case, the relation of i_o and i_{in} of current mirror can be approximated as [1]

$$i_o \cong i_{in}\left(1+\frac{\Delta K}{K}-\frac{2\Delta V_{TH}}{V_{GS}-V_{TH}}\right) \tag{18}$$

where $\Delta V_{DS} = V_{DSo} - V_{DSi}$, $\Delta K = K_o - K_i$, $K = 0.5(K_o - K_i)$, $\Delta V_{TH} = V_{THo} - V_{THi}$ and $V_{TH} = 0.5(V_{THo} - V_{THi})$ given that $K_i = K - 0.5\Delta K$, $K_o = K + 0.5\Delta K$, $V_{THo} = V_{TH} - 0.5\Delta V_{TH}$ and $V_{THi} = V_{TH} + 0.5\Delta V_{TH}$. From Equations (18), two factors could deviate the current i_o of current mirror from ideal characteristics: the non-ideal effect of ΔV_{TH} and the non-ideal effect of ΔK. From the same equation, small ΔV_{TH} and ΔK

reduce the error of the current i_o. The effect of ΔV_{TH} is reduced if V_{GS} is several times larger than V_{TH}. The non-ideal effect of ΔK is the error in the aspect ratio of the transistor devices, which could be due to mask, photolithographic and/or out-diffusion variations. It is obvious from Equation (18) that high value of ΔK will result in high error current i_o of current mirror. The effect of ΔK can be minimized with a careful layout, i.e., the dimensions of the transistors should be designed much larger than the typical variation. In addition, the use of reference voltages for current mirrors can be obtained a very high precision of the proposed circuit.

3.3 Non-ideal effects of current rectifier cell

To determine the influence of class-AB rectifier cell non-idealities, the dual translinear loop (MD_1 to MD_4) will be analyzed. Ideally, characteristics of the transistors MD_1 to MD4 are required to be identical. A mismatch of the transistors MD_1 to MD_4 will result in asymmetry of output waveform, i.e., the amplitude of the first polarity signal may not be equal to that of the second polarity signal at output.

Let us assume that the proposed circuit is designed by standard CMOS technology version of p-substrate. Thus all PMOS devices are suitable for implementation in n-well and all NMOSs are suitable for implementation in p-substrate. Typically, for standard CMOS technology version of p-substrate, the substrate will be applied by V_{SS}, then the bodies of the transistors MD_1-MD_2 are connected to V_{SS} and those of the transistors MD_3-MD_4 are connected to their sources. Therefore, the body effect on transistors MD_1-MD_2 should be examined whereas the transistors MD_3-MD_4 are insensitive to the variation of the threshold voltage induced by the body effect. The threshold voltage with the body effect can be expressed as

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|V_{SB}| + 2\varphi_F} - \sqrt{2\varphi_F}\right) \tag{19}$$

where V_{SB} is the source-to-body substrate bias, $2\varphi_F$ the surface potential, V_{TH0} the threshold voltage for zero substrate bias, $\gamma = \left(t_{ox}/\varepsilon_{ox}\right)\sqrt{2q\varepsilon_{si}N_A}$ the body effect parameter, t_{ox} the oxide thickness, ε_{ox} the oxide permittivity, ε_{si} the permittivity of

silicon, N_A the doping concentration, and q the charge of an electron. The voltage V_{SB} directly affects the threshold voltage.

In Fig. 1, however, $V_{SG(MD3)}+V_{GS(MD1)}$ >0 and both M_{D2} and M_{D4} are biased to conduct nonzero drain current when V_D=0, which is a characteristic of a class-AB. If $V_{TH(MD1)}=V_{TH(MD2)}$, $V_{TH(MD3)}=V_{TH(MD4)}$, $I_1=I_2=I$, assuming M_{D1} to M_{D4} is operated in saturation region, $I_{D(MD3)}=-I_{D(MD1)}$, the currents $I_{D(MD1)}$ and $I_{D(M3)}$ can be given, respectively, as [3]

$$I_{D(MD1)} = I\frac{\left(\frac{1}{\mu_n C_{ox}\left(W/L\right)_{MD2}}+\frac{1}{\mu_p C_{ox}\left(W/L\right)_{MD4}}\right)}{\left(\frac{1}{\mu_n C_{ox}\left(W/L\right)_{MD1}}+\frac{1}{\mu_p C_{ox}\left(W/L\right)_{MD3}}\right)} \tag{20}$$

This equation shows that the quiescent current in the class-AB dual translinear loop rectifier cell is well controlled with respect to the bias current that flows in the diode-connected transistors (M_{D2} and M_{D4}) [3].

Using Equations (16) and (18), Equations (7), (10), (12) and (14) can be rewritten, respectively, as

$$V_{in}<0\ ;\ V_{H+}=+\frac{\alpha\beta R_{o1}V_{in}}{R_{in}+R_x}\left(\lambda_{effect}+K_{error}\right) \tag{21}$$

$$V_{in}>0\ ;\ V_{H-}=-\frac{\alpha\beta R_{o2}V_{in}}{R_{in}+R_x}\left(\lambda_{effect}+K_{error}\right) \tag{22}$$

$$\left.\begin{aligned} V_{in}<0\ &;\ V_{F+}=+\frac{\alpha\beta R_{o3}V_{in}}{R_{in}+R_x}\left(3\lambda_{effect}+3K_{error}\right)\\ V_{in}>0\ &;\ V_{F+}=-\frac{\alpha\beta R_{o3}V_{in}}{R_{in}+R_x}\left(2\lambda_{effect}+2K_{error}\right)\end{aligned}\right\} \tag{23}$$

$$\left.\begin{aligned} V_{in}<0\ &;\ V_{F-}=-\frac{\alpha\beta R_{o4}V_{in}}{R_{in}+R_x}\left(2\lambda_{effect}+2K_{error}\right)\\ V_{in}>0\ &;\ V_{F-}=+\frac{\alpha\beta R_{o4}V_{in}}{R_{in}+R_x}\left(3\lambda_{effect}+3K_{error}\right)\end{aligned}\right\} \tag{24}$$

where $\lambda_{effect}=\left(\frac{K_o}{K_i}\right)\left(\frac{V_{GS}-V_{THo}}{V_{GS}-V_{THi}}\right)^2\left(\frac{1+\lambda V_{DSo}}{1+\lambda V_{DSi}}\right)$, $K_{error}=\left(1+\frac{\Delta K}{K}-\frac{2\Delta V_{TH}}{V_{GS}-V_{TH}}\right)\left(1+\frac{\Delta V_{DS}}{V_A}\right)$

and assume that λ_{effect} and K_{error} of positive and negative current mirrors are identical for

Equations (23) and (24). It is evident from Equations (21) to (24) that the non-idealities of CCII and of current mirrors will attenuate the amplitude of the output voltage signals and may increase the DC output offsets. However, the amplitude error can be corrected by increasing the value of the output resistors (R_{o1}, R_{o2}, R_{o3} and R_{o4}) while the DC output offset can be compensated by adjusting the values of the currents I_5, I_6, I_7 and I_8. For high-frequency response, the major limitation of the rectifier is the internal poles of current mirrors. When the current i_z is applied into the current rectifier cell, the signal will be mirrored by only one current mirror to create the half-wave waveform; and to create full-wave waveform, the signal will be mirrored by two or three current mirrors. Therefore, the half-wave rectifier can operate in higher frequency than can the full-wave rectifier.

For the input range of the proposed rectifier, it can be obtained by assuming that the transistors M_1 to M_4 in Fig. 2 are biased in the saturation region. The minimum and maximum input voltage ranges of the proposed rectifier can be expressed as

$$V_{in(\min)} = V_{SS} + \left|V_{THP}\right| + \left|V_{TN}\right| + \left|V_{eff(M4)}\right| + \left|V_{eff(M8)}\right| \tag{25}$$

$$V_{in(\max)} = V_{DD} - \left|V_{THP}\right| - \left|V_{TN}\right| - \left|V_{eff(M2)}\right| + \left|V_{eff(M12)}\right| \tag{26}$$

where $V_{eff} = V_{GS} - V_{TH} = \sqrt{\dfrac{2I_D}{\mu C_{ox}(W/L)}}$ [44], where in turn V_{GS} is the gate to source voltage, V_{TH} the threshold voltage, I_D the drain current, μ the mobility of carriers, C_{ox} the gate capacitance per unit area, W and L are the width and length, respectively, of MOS transistor.

By consideration of the circuit in Fig. 1, it is seen that the minimum supply requirement is imposed by the dual translinear loop. The requirement of the supply voltages V_{DD} and $|V_{SS}|$ are given by

$$V_{DD} > V_{TH(MC1)} + V_{DS(MD1),sat} \tag{27}$$

$$\left|V_{SS}\right| > V_{DS(MD3),sat} + V_{TH(MC3)} \tag{28}$$

This equation is given to ensure that all transistors are saturated.

4. Simulation and experimental results

The scheme of the proposed versatile rectifier in Fig. 1 was simulated using the PSPICE simulation program. For the circuit simulation, TSMC 0.18 μm n-well CMOS process [45] was used. The transistor dimensions of Figs. 1 and 2 were tabulated as shown in Table 2. The supply voltage used is ±1.2V, and the bias currents used are $I_{C1} = I_{C2} = 20\mu A$ and $I_3 = I_4 = 100\mu A$. The currents I_3 and I_4 were implemented using current source with a single current reference. The current sources I_5 to I_8 are set to compensate the constant current sources. The aspect ratios of MR_1 and MR_2 are larger than those of MR_3 to MR_{10} used to compensate the non-ideal behavior of the current conveyor and the error of the current mirrors. The DC transfer characteristics of the proposed rectifier are shown in Fig. 3, which illustrates the operating voltage range from –200mV to 200mV of the input voltage. Three different currents were used for I_1 and I_2 ($I_2 = I_1$), i.e., 0.5, 1 and 3 μA. It is observed from Fig. 3 that the corner distortion regions of the half-wave and full-wave outputs reduce when the bias currents decrease from 3 μA to 0.5 μA. This means that the precision of the proposed rectifier can be achieved by selecting appropriate bias currents I_1 and I_2.

The next test was a test of time domain responses. By applying 100 mV_{peak} sine wave at the input of the proposed rectifier, the input and output signals at 10 MHz and 100 MHz frequencies are shown in Figs. 4 and 5, respectively. It is observed from both figures that the proposed rectifier performs both dual output half-wave rectifier and dual output full-wave rectifier from the same configuration. Moreover, undistorted half-wave rectified signals and full-wave rectified signals are produced for a high frequency up to 100MHz.

In order to examine the temperature stability of the proposed rectifier, the circuit was fed with an 100 mV_{peak}, 10 MHz signal while varying the simulation temperatures between 27°C and 100°C. Fig. 6 shows the output waveforms V_{H+} and V_{F+} of the proposed rectifier at temperatures of 27°C, 75°C and 100°C. The result indicates that the proposed rectifier provides good temperature stability as validated by Equations (7)-(10), (12) and (14). However, the output waveforms suffer from the DC offset even though they are free from distortion. These offset voltages can be easily improved by adjusting

the bias currents I_5 to I_8.

The proposed rectifier was again simulated to check the precision performance. The 10 MHz input signal frequency was applied and the amplitude set at 50 mV_{peak}. The input and output waveforms in this case are shown in Fig. 7. It is evident from these figures that the proposed rectifier can rectify low-level signal. More precision can be achieved by reducing the bias currents I_1 and I_2, but this is likely to affect the bandwidth of the system. To investigate the performance of the proposed circuit with the circuit operating in the higher than 100 MHz frequency, 400 MHz frequency for 100 mV_{peak} sine wave was applied at the input of the proposed circuit. Fig. 8 shows the operation of half-wave rectifier at frequency of 400 MHz, respectively. It is evident that the half-wave rectifier can rectify the high frequency up to 400 MHz as it utilizes the current-mode class-AB rectifier, which is biased just on, and the current conveyor of which response is fast. For high-frequency response, the full-wave rectifier suffers three internal poles of three current mirrors while the half-wave rectifier suffers only one internal pole of current mirror. This is the season why the half-wave rectifier can operate in higher frequency than the full-wave rectifier. However, the operation in high frequency of the circuit might be achievable only in simulation. If the proposed rectifier was fabricated as an IC, its capacity to operate in high frequency would be lessened by the effect of parasitic capacitance in the IC. The amplitude errors between the input and output signals in Fig. 8 results from the decrease of the gain of the proposed rectifier for the operation at high frequency. This problem can be solved by decreasing the W/L of MR_3 to MR_6 so as to increase the values of R_{o1} and R_{o2}.

It is widely acknowledged that periodic waveforms, such as half-wave symmetry and full-wave symmetry, can be transformed to the harmonic components using Fourier series analysis. In order to test the harmonic distortion of the proposed rectifier, the amplitudes of each harmonic of half-wave waveform and full-wave waveform are obtained with fast Fourier transform (FFT) analysis through PSPICE simulators. The total harmonic distortion (THD) is defined by [8], [9]

$$THD\ (\text{dB}) = 20\log_{10}(V_{THD}) \tag{26}$$

where $V_{THD} = \sqrt{\sum_{n=2}\left(V_n^2 / V_1^2\right)}$, where in turn V_1 is the fundamental frequency voltage

component, V_n is the n^{th} harmonic voltage component, and n is 1, 2, 3, …., etc. For the case of a full-wave rectifier, when a sinusoidal signal of frequency f is applied to the input, the steady-state response at the output consists of harmonic components at 2f, 4f, 6f, … etc (even harmonics) whereas odd harmonics which include fundamentals should be zero. The simulated THD versus frequency varying from 1 MHz to 100 MHz is shown in Fig. 9. In case of full-wave rectifier, the component 2f is used as a fundamental content and the others are harmonic contents. In case of half-wave rectifier, the THD of half-wave signals is obtained with FFT using PSPICE simulators. Compared with [8], [9], the THD of the proposed circuit is higher because this circuit was tested with lower level of input signal and higher frequency of input signal.

In order to examine the effect of mismatch on the proposed rectifier, the Monte Carlo analysis using 100 runs was performed. Fig. 10 shows the Monte Carlo analysis of the output waveforms with 10 % variations in threshold voltage of all PMOS transistors. The result in Figs. 10 confirms the reliability of the circuit.

The ripple voltage is an important parameter for testing a rectifier. According to the simulation, the ripple voltage versus frequency of the proposed rectifier is high. It is similar to the results of previous works, except the circuits in [8], [9]. The circuits in [8], [9] offer lower ripple voltage versus frequency when compared with the proposed rectifier. However, if a low ripple voltage output of the proposed rectifier or previous works with similar principles is needed, several techniques to achieve this requirement exist by adding to the output, for instance, additional filters, voltage regulator, RMS-to-DC converter, and peak detector circuit.

The proposed rectifier of Fig. 1 was also constructed on a prototype PCB, as shown in Fig. 11. The form of complementary MOS pairs (MC14007) is used for realizing all MOS devices. The available chip CFOA in an AD844 was chosen for realizing CCII. The bias currents I_1 and I_2 are replaced with the resistance of 1.5 MΩ ($I_1 = I_2 =$ 1μ A), the bias currents I_3 and I_4 with the resistance of 10 kΩ ($I_3 = I_4 =$ 488 μA), and the bias currents I_5 to I_8 with the variable resistors (500 kΩ). The resistor R_{in} is given as 1 kΩ. The supply voltage was set to ± 7.5 V. The experimental results in Figs. 12 (a)–(d) show the output waveform for the input signals in the form of sinusoidal with the peak amplitude of 100 mV_{peak} and with the frequency of 200 kHz. These results

demonstrate that the circuit can provide the clean positive/negative half-wave and positive/negative full-wave rectified signals, the finding of which is to confirm that this circuit is the precision rectifier. The higher frequency can be obtained if the bias currents I_1 and I_2 increase but the precision of the circuit may decrease.

5. Conclusions

The design of a versatile precision rectifier was presented in this paper. The proposed rectifier employs one CCII, six current mirrors, five grounded resistors, and eight current sources, and it possesses the features superior to the existing rectifiers as follows:

(1) The proposed circuit can realize a versatile current-mode rectifier. In other words, when the input single-phase signal is applied to the circuit, its outputs can be the function of positive half-wave, negative half-wave, positive full-wave, negative full-wave rectifications from the same configuration.

(2) The proposed rectifier is capable of operating in a frequency up to 100 MHz (simulated with TSMC 0.18 μm CMOS process).

(3) The proposed structure can be implemented as either a CMOS technology or a bipolar technology.

(4) The proposed rectifier exhibits good temperature stability.

In addition, the proposed rectifier is superior to the existing circuits with respect to suitability for IC fabrication as both CMOS and bipolar technologies. In the simulation, the parameter of TSMC 0.18 μm n-well CMOS process and the supply voltage of ±1.2 V are used. The PSPICE simulation results show the operating input of –300 to 300 mV. For the operating frequency of 100 MHz, the best positive/negative half-wave and positive/negative full-wave rectified signals can be achieved. The circuit half-wave rectifier can rectify high frequency up to 400 MHz. Moreover, the experimental results confirm workability of the proposed circuit. The findings show that the circuit can rectify the signal that has less amplitude than the threshold voltage of the diode (<0.3). **The comparison between the proposed circuits and some previously works is summarized in Table 3.** In fact, the circuit is suitable for a high impedance load. If a low impedance load is applied, the circuit needs voltage buffers at the outputs. If the proposed rectifier is loaded with low impedance loads, the loads could be connected directly to the

circuit without the need of the output resistors (R_{o1} , R_{o2} , R_{o3} and R_{o4}) but a high linearity resistor (high linear R_{in}) is imperative that may be achieved using external resistor or sheet resistor in integrated circuits.

Acknowledgments

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References

[1] P. E. Allen and D. R. Holberg, *CMOS analog circuit design*, Holt, Rinehart and Winston, New York, 1987.

[2] A. J. Peyton, V. Walsh, *Analog electronics with op amps: a source book of practical circuits*, New York, Cambridge University Press, 1993.

[3] P. Gray, P. J. Hurst, S. H. Lewis, R. G. Meyer, *Analysis and design of analog integrated circuit*, New York, John Wiley & Sons, 2001.

[4] Z. Wang, "Full-wave precision rectification that is performed in current domain and very suitable for CMOS implementation," *IEEE Transactions on Circuit and Systems-I*, vol. 39, pp. 456-462, 1992.

[5] S. J. G. Gift, "A high-performance full-wave rectifier circuit," International Journal of Electronics, vol. 89, pp. 467-476, 2000.

[6] S. J. G. Gift, "An improved precision full-wave rectifier," *International Journal of Electronics*, vol. 89, pp. 259-265, 2002.

[7] S. J. G. Gift, "Versatile precision full-wave rectifiers for instrumentation and measurements," *IEEE Transactions on Instrumentation and Measurements*, vol. 56, pp. 1703-1709, 2007.

[8] P. P. Sahu, M. Singh, A. Baishya, "A novel versatile precision full-wave rectifier," *IEEE Transactions on Instrumentation and Measurements*, vol. 59, pp. 2742-2746, 2010.

[9] P. P. Sahu, M. Singh, A. Baishya, "New low-voltage full wave rectification technique without a diode," *IET Circuits, Devices and Systems*, vol. 5, pp. 33-36, 2011.

[10] C. Toumazou, F. J. Lidgey, S. Chattong, "High frequency current conveyor precision full-wave rectifier," *Electronics Letters*, vol. 30, pp. 745-746, 1994.

[11] K. Hayatleh, S. Porta, F. J. Lidgey, "Temperature independent current conveyor," *Electronics Letters*, vol. 30, pp. 2091-2093, 1994.

[12] A. A. Khan, M. A. El-Ela, M. A. Al-Turaigi, "Current-mode precision rectification," *International Journal of Electronics*, vol. 79, pp. 853-859, 1995.

[13] B. Wilson, V. Mannama, "Current-mode rectifier with improved precision," *Electronics Letters*, vol. 31, pp. 247-248, 1995.

[14] K. Anuntahirunrat, W. Tangsrirat, V. Riewruja, W. Surakampontorn, "Sinusoidal frequency doubler and full-wave rectifier based on translinear current-controlled current conveyors," *International Journal of Electronics*, vol. 85, pp. 55-60, 1998.

[15] A. Monpapassorn, K. Dejhan, F. Cheevasuvit, "A full-wave rectifier using a current conveyor and current mirrors," *International Journal of Electronics*, vol. 88, pp. 751-758, 2001.

[16] S. J. G. Gift, "New precision rectifier circuits with high accuracy and wide bandwidth," *International Journal of Electronics*, vol. 92, pp. 601-617, 2005.

[17] E. Yuce, S. Minaei, O. Cicekoglu, "Full-wave rectifier realization using only two CCII+s and NMOS transistors," *International Journal of Electronics*, vol. 93, pp. 533-541, 2006.

[18] S. Maheshwari, "Current controlled precision rectifier circuits," *Journal of Circuit Systems, and Signal Components,* vol. 16, pp. 129-138, 2007.

[19] S. Minaei, E. Yuce, "A new full-wave rectifier circuit employing single dual-X current conveyors," *International Journal of Electronics*, vol. 95, pp. 777-784, 2008.

[20] D. Biolek, E. Hancioglu, A. U. Keskin, "High-performance current differencing transconductance amplifier and its application in precision current-mode rectification," *International Journal of Electronics and Communications*, vol. 62, pp. 92-96, 2008.

[21] F. Khateb, J. Vavra, D. Biolek, "A novel current-mode full-wave rectifier based on one CDTA and two diodes," *Radioengineering*, vol. 19, pp. 437-445, 2010.

[22] J. Koton, N. Herencsar, K. Vrba, "Current and voltage conveyors in current and voltage-mode precision full-wave rectifiers," *Radioengineering*, vol. 20, pp. 19-24, 2011.

[23] M. Kumngern, "Precision full-wave rectifier using only two DDCCs," *Circuits and Systems*, vol. 2, pp. 127-132, 2011.

[24] E. Sanchez-Sineccio, J. Ramirez-Angulo, B. Linares-Barranco, A. Rodriguez-Vazquez, "Operational transconductance amplifier-based nonlinear function syntheses," *IEEE Journal of Solid-State Circuits*, vol. 24, pp. 1576-1586, 1989.

[25] P. Heim, F. Krummenacher, E. Vittoz, "CMOS full-wave operational transconductance rectifier with improved DC transfer characteristic," *Electronics Letters*, vol. 28, pp. 333-334, 1992.

[26] J. Ramirez-Angulo, "High frequency low voltage CMOS diode," *Electronics Letters*, vol. 28, pp. 298-299, 1992.

[27] M. Kumngern, K. Dejhan, "High frequency and high precision CMOS full-wave rectifier," *International Journal of Electronics*, vol. 93, pp. 185-199, 2006.

[28] C. Jongkunstidchai, C. Fongsamut, K. Kumwachara, W. Surakampontorn, "Full-wave rectifiers based on operational transconductance amplifiers," *International Journal Electronics and Communications*, vol. 61, pp. 195-201, 2007.

[29] N. Minhaj, "OTA-based non-inverting and inverting precision full-wave rectifier circuits without diodes," *International Journal of Recent Trends in Engineering*, vol. 1, pp. 72-75, 2009.

[30] M. Kumngern, "High frequency and high precision CMOS full-wave rectifier," in *Proceedings of IEEE International Conference on Communication Systems (ICCS 2010)*, Singapore, 2010, pp. 5-8.

[31] V. Surakumpontorn, V. Riewruja, "Integrable CMOS sinusoidal frequency doubler and full-wave rectifier," *International Journal of Electronics*, vol. 73, pp. 627-632, 1992.

[32] J. Ramirez-Angulo, R. G. Carvajal, J. Tombs, A. Torralba, "Very low-voltage class-AB CMOS and bipolar precision current rectifiers," *Electronics Letters*, vol. 35, pp. 1904-1905, 1999.

[33] V. Riewruja, R. Guntapong, "A low-voltage wide-band CMOS precision full-wave rectifier," *International Journal of Electronics*, vol. 89, pp. 467-476, 2002.

[34] K. Kumngern, B. Knobnob, K. Dejhan, "High frequency and high **precision** CMOS half-wave rectifier," *Circuits, Systems and Signal Processing*, vol. 29, pp. 815-836, 2010.

[35] M. Samy Hosny, J. Hanson, "A wide-band, high-precision CMOS rectifier," *Analog Integrated Circuits and Signal Processing*, vol. 5, pp. 183-190, 1994.

[36] H. Chaoui, "CMOS high-frequency rectifier with unity voltage gain," *Electronics Letters*, vol. 31, pp. 717-718, 1995.

[37] A. Monpapassorn, K. Dejhan, F. Cheevasuvit, "CMOS dual output current mode half-wave rectifier," *International Journal of Electronics*, vol. 88, pp. 1073-1084, 2001.

[38] M. Kumngern, K. Dejhan, "Current conveyor-based versatile precision rectifier," *WSEAS Transactions on Circuits and Systems*, vol. 7, pp. 1070-1079, 2008.

[39] Z. Wang, "2-MOSFET transistor with extremely low distortion for output reaching supply voltage," *Electronics Letters*, vol. 26, pp. 951-952, 1990.

[40] A. Sedra, K Smith, "A second-generation current-conveyor and its applications," *IEEE Transactions on Circuit Theory*, vol. CT-17, pp. 132-134, 1970.

[41] W. Surakampontorn, V. Riewruja, K. Kumwachara, K. Dejhan, "Accurate CMOS-based current conveyors," *IEEE Transactions on Instrumentation and Measurement*, vol. 40, pp. 699-702, 1991.

[42] A. M. Ismail, A. M. Soliman, "Wideband CMOS current conveyor," *Electronics Letters*, vol. 34, pp. 2368-2369, 1998.

[43] G. Ferri, N. C. Guerrini, "*Low-voltage low-power CMOS current conveyors*," Kluwer Academic Publishers, New York, 2003.

[44] D. Johns, K. Martin, *Analog integrated circuit design*, John Wiley & Sons, New York, 1997.

[45] http://www.mosis.com/pages/Technical/Testdata/tsmc-018-prm

Figures

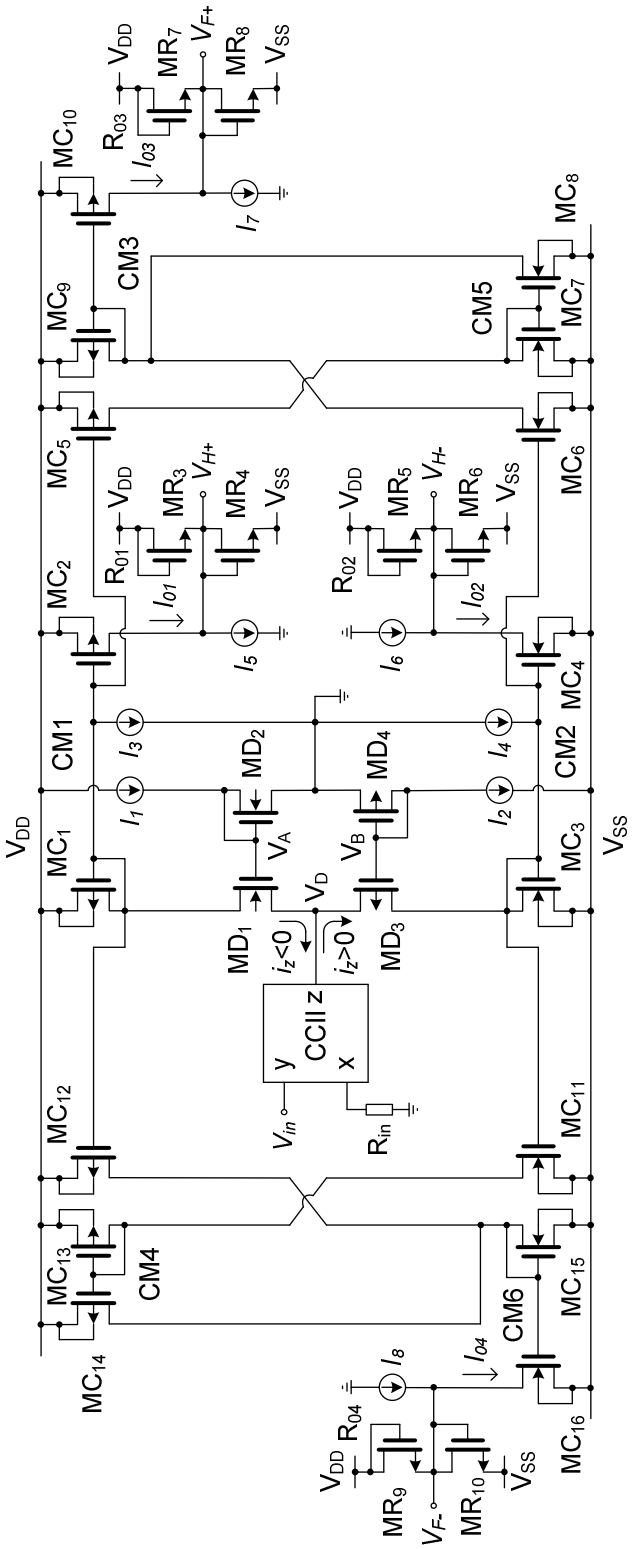
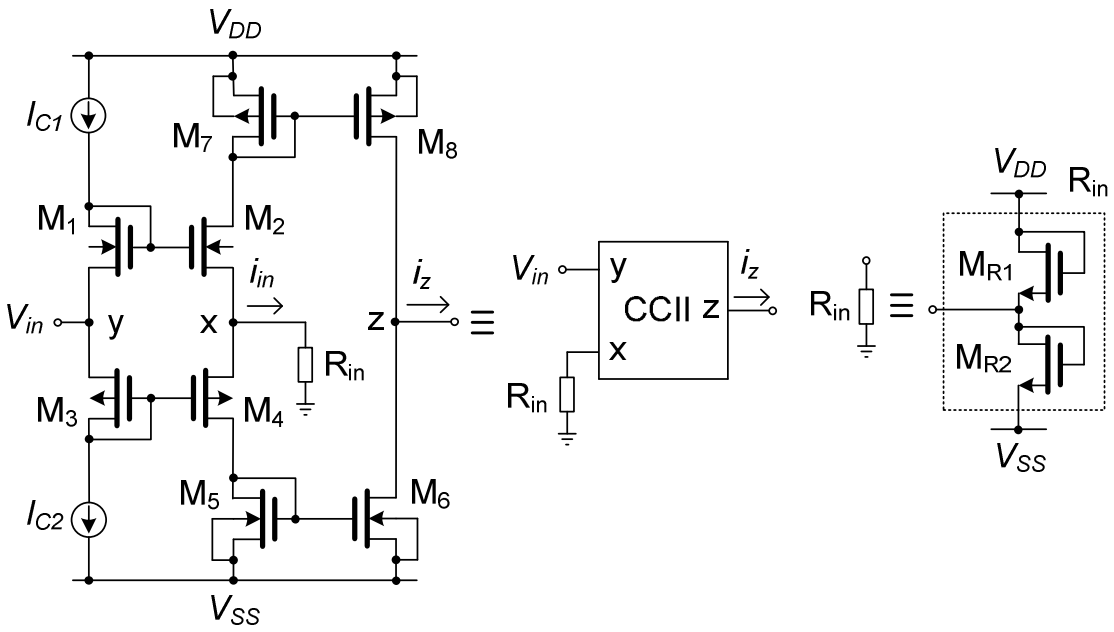
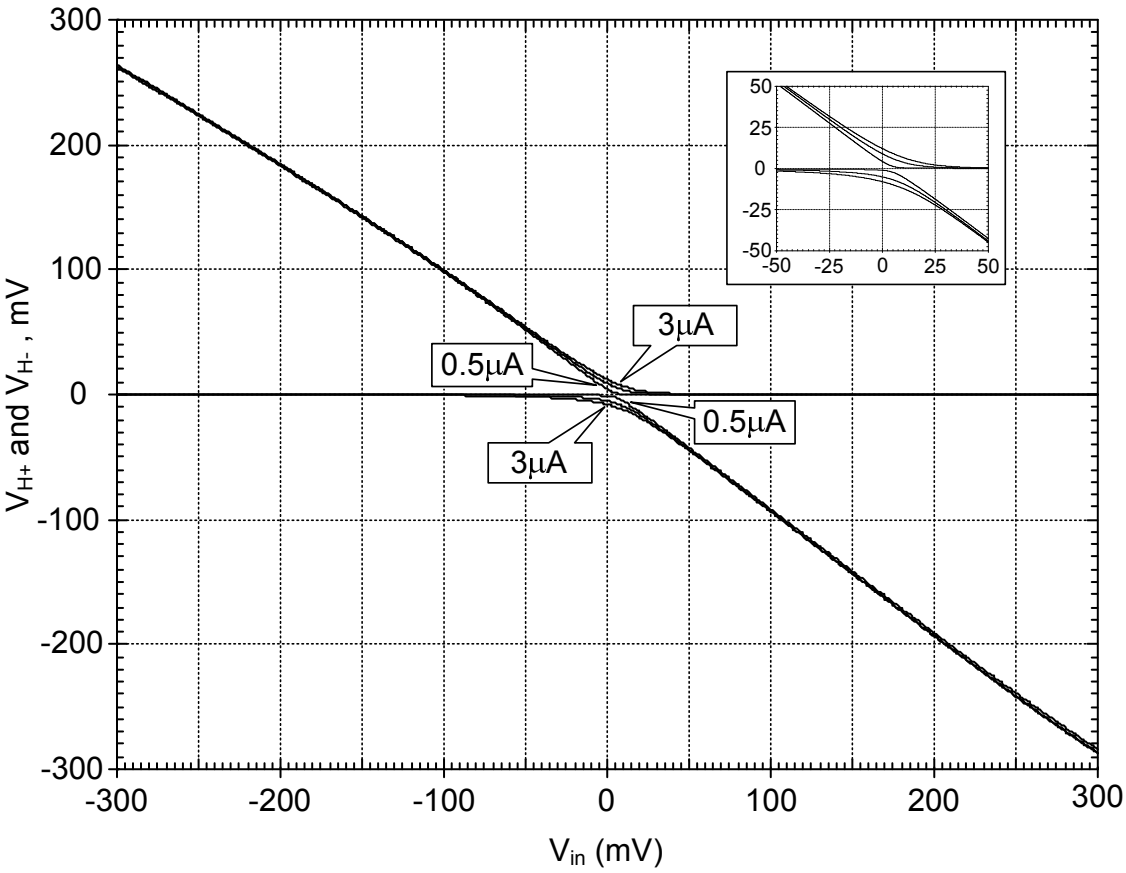


Figure 1. Proposed versatile precision rectifier.

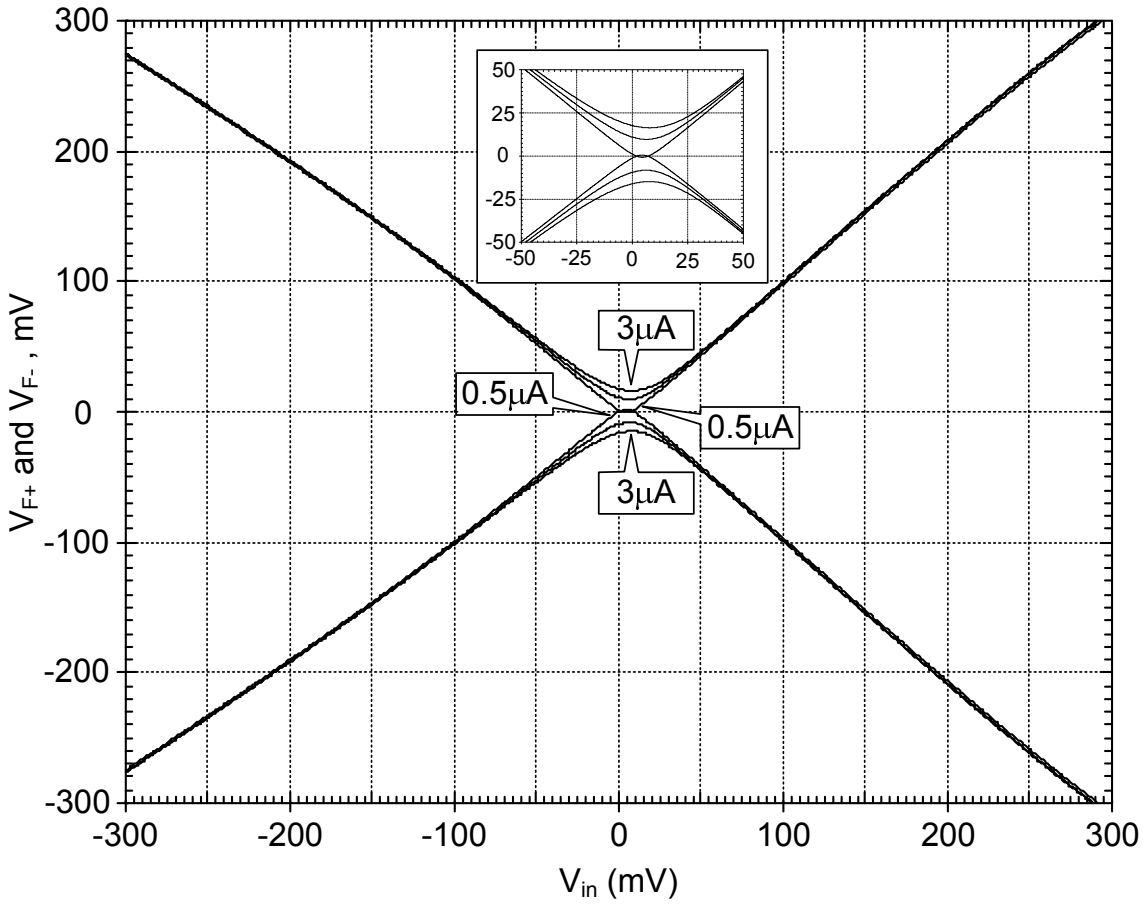


(a) (b)

Figure 2. (a) Voltage-to-current converter circuit, **(b) possible MOS implementation for resistor R_{in}.**



(a)



(b)

Figure 3. Simulated results for DC transfer characteristics: (a) half-wave rectifier, (b) full-wave rectifier.

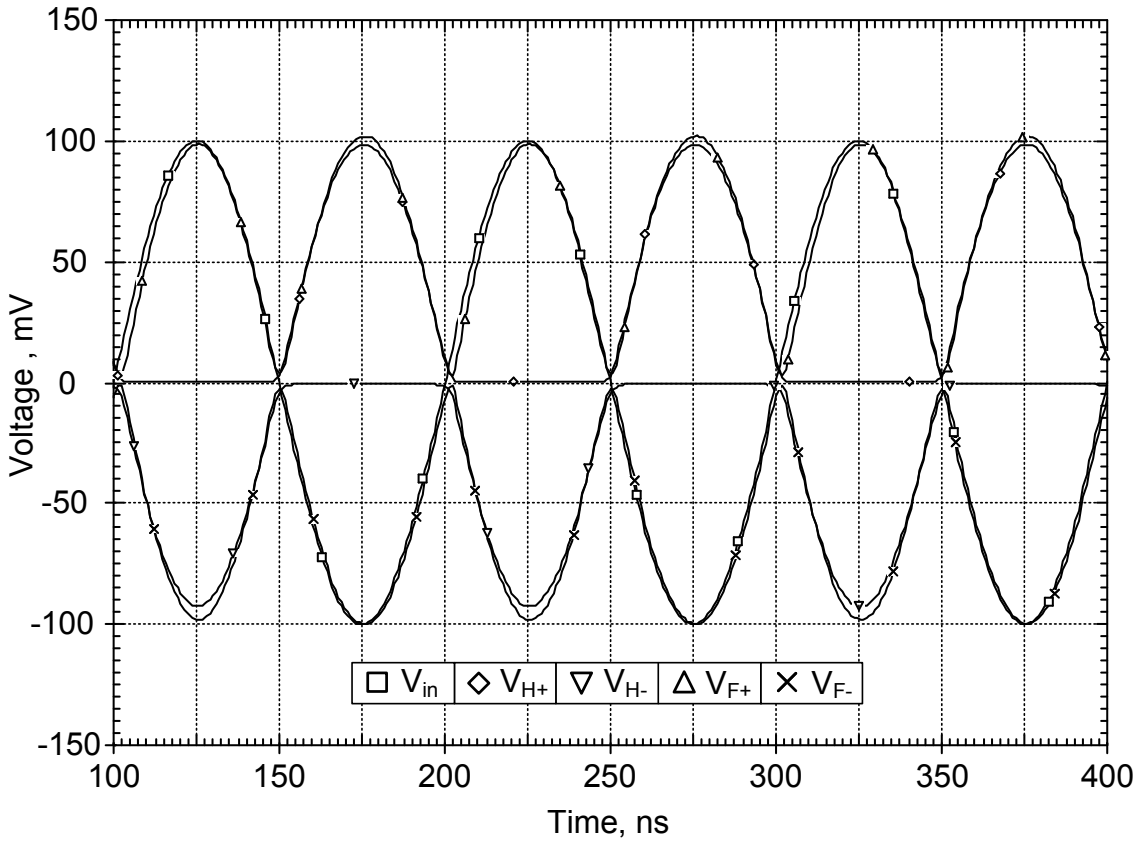


Figure 4. Operation of proposed rectifier at the input signal frequency 10 MHz.

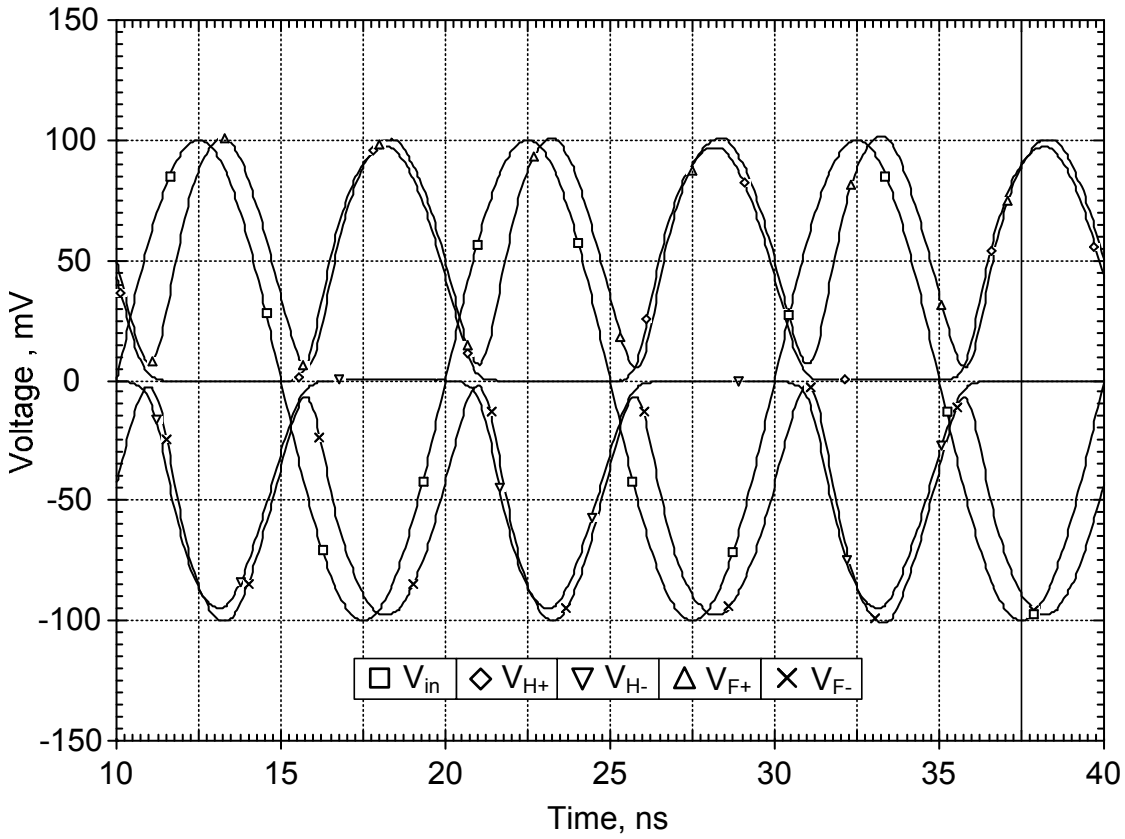
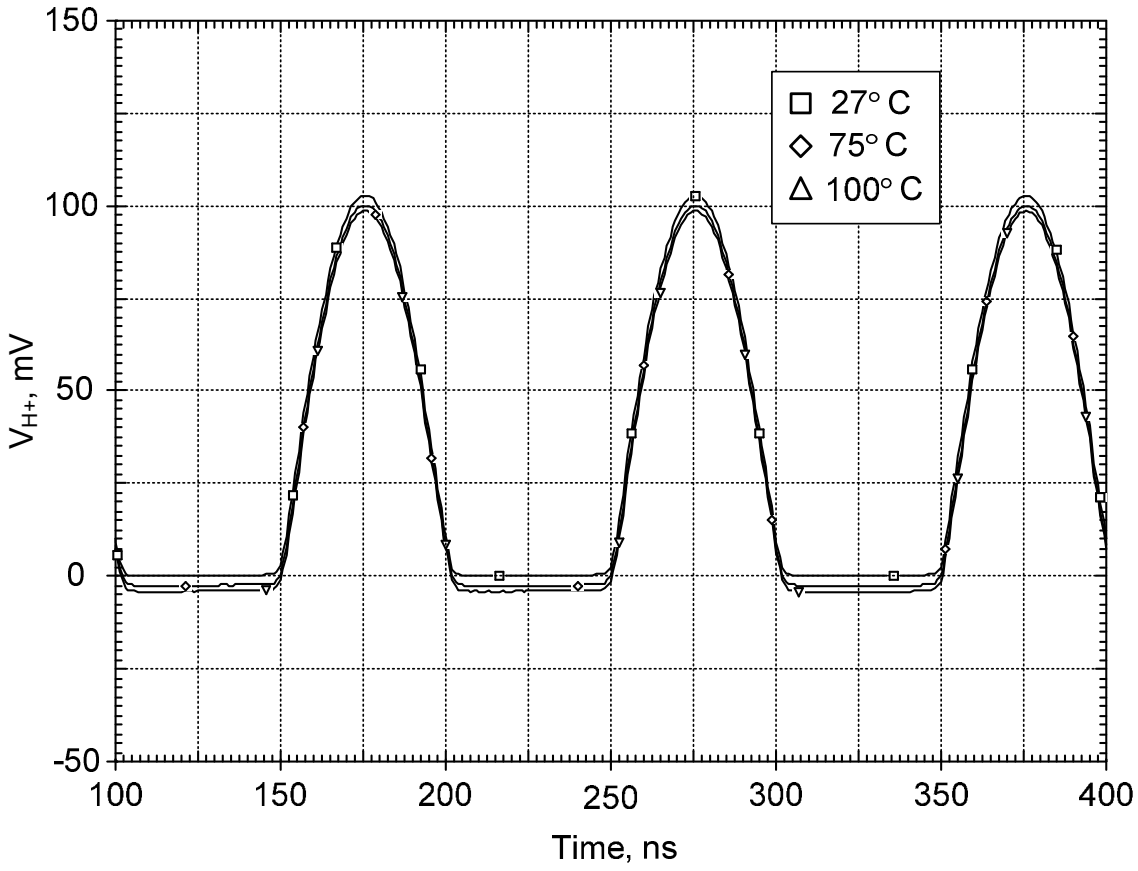
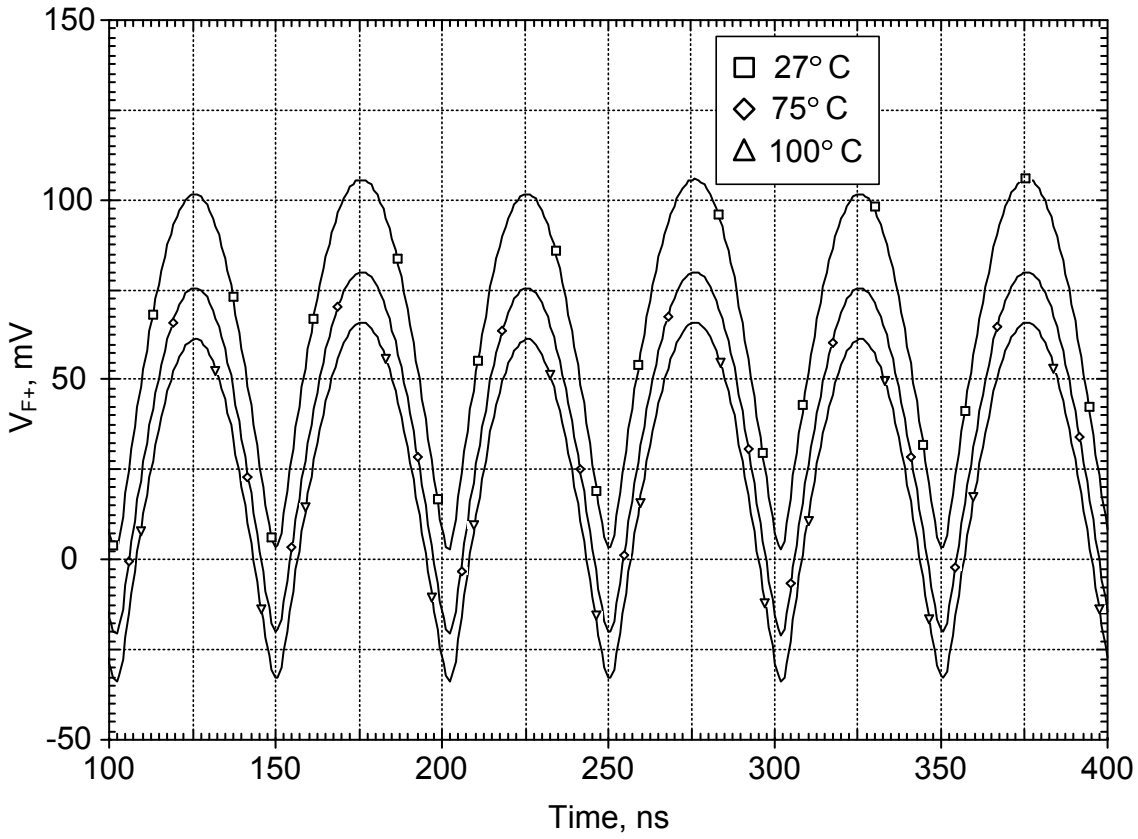


Figure 5. Operation of proposed rectifier at the input signal frequency 100 MHz.



(a)



(b)

Figure 6. Output waveforms at different temperatures at the input signal frequency 10 MHz: (a) positive half-wave rectifier; (b) positive full-wave rectifier.

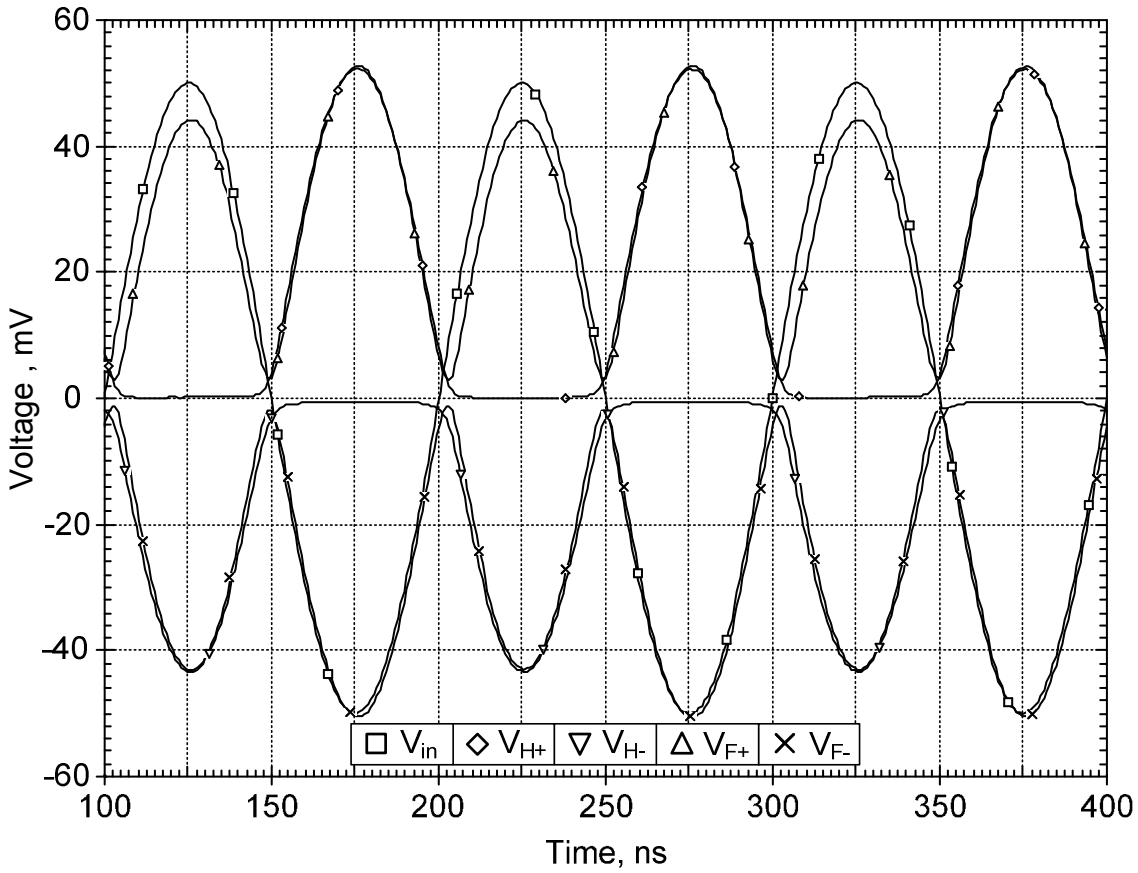


Figure 7. Rectified outputs at the input signal frequency 10 MHz for 50 mVpeak.

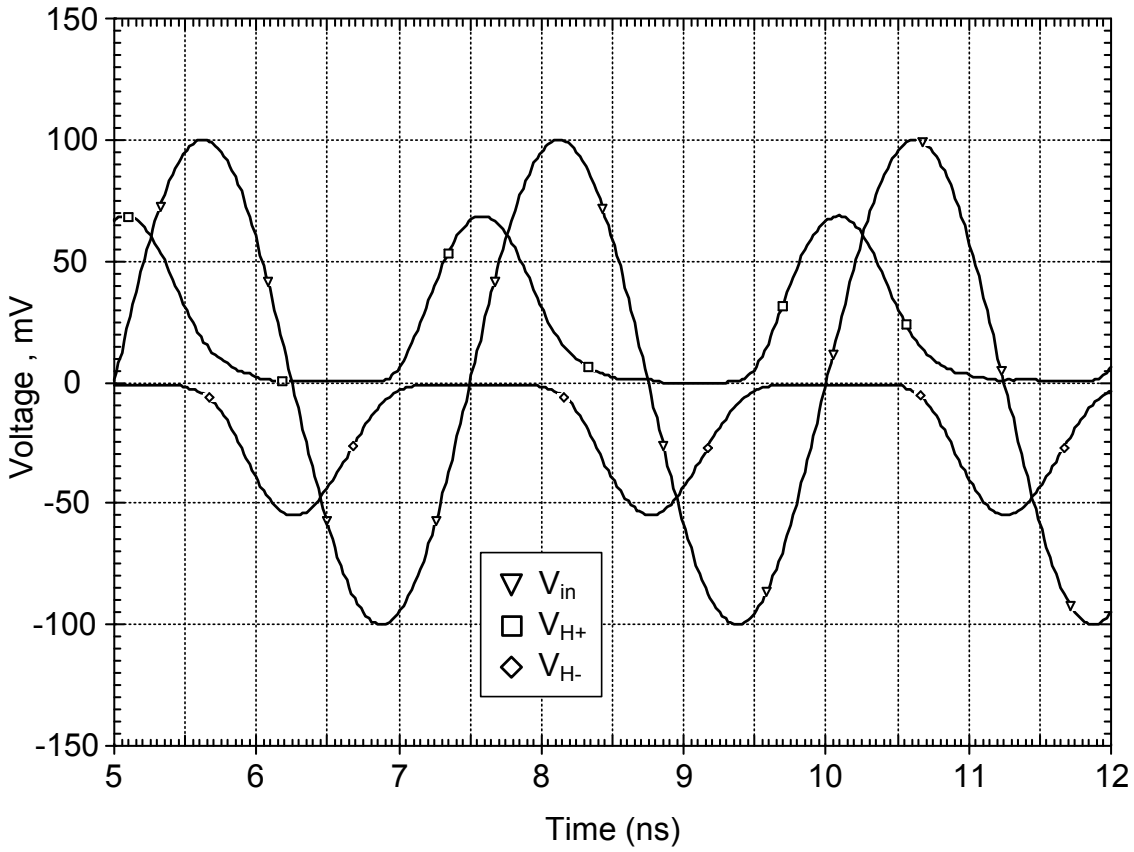


Figure 8. Operation of proposed rectifier at the input signal frequency 400 MHz for half-wave rectifier.

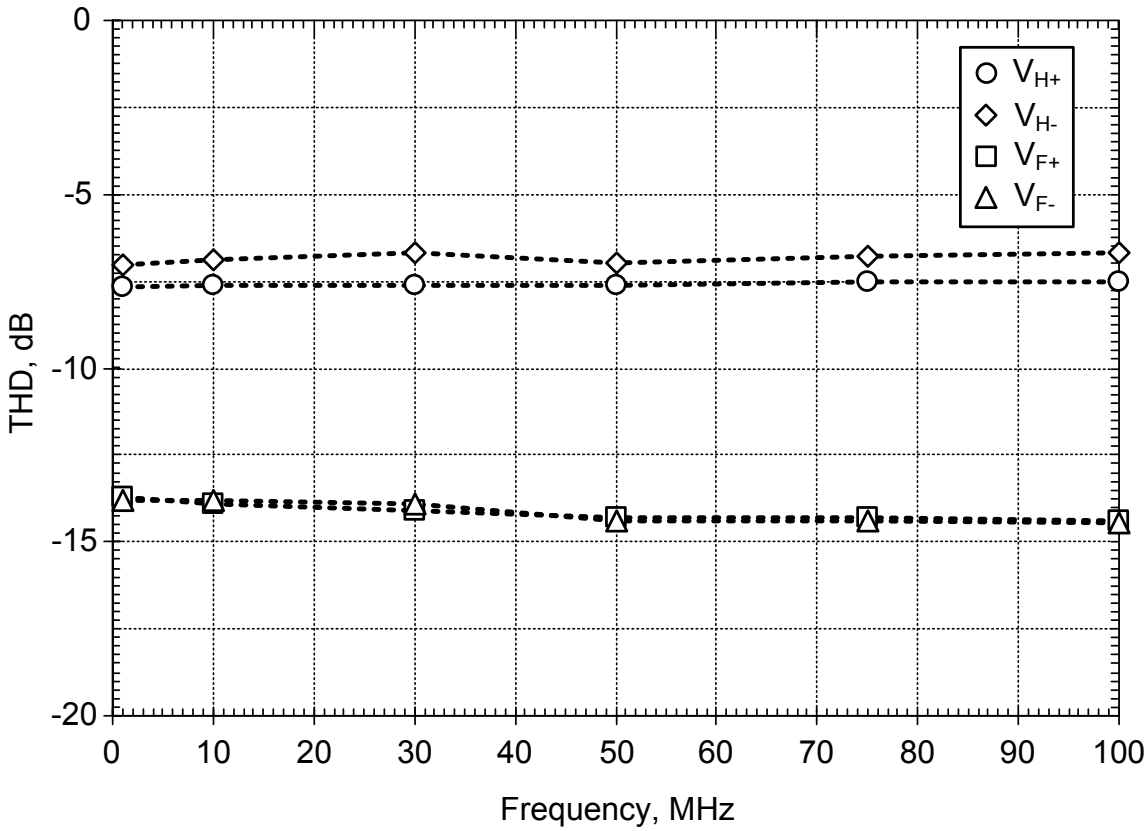


Figure 9. Simulated THD with frequencies.

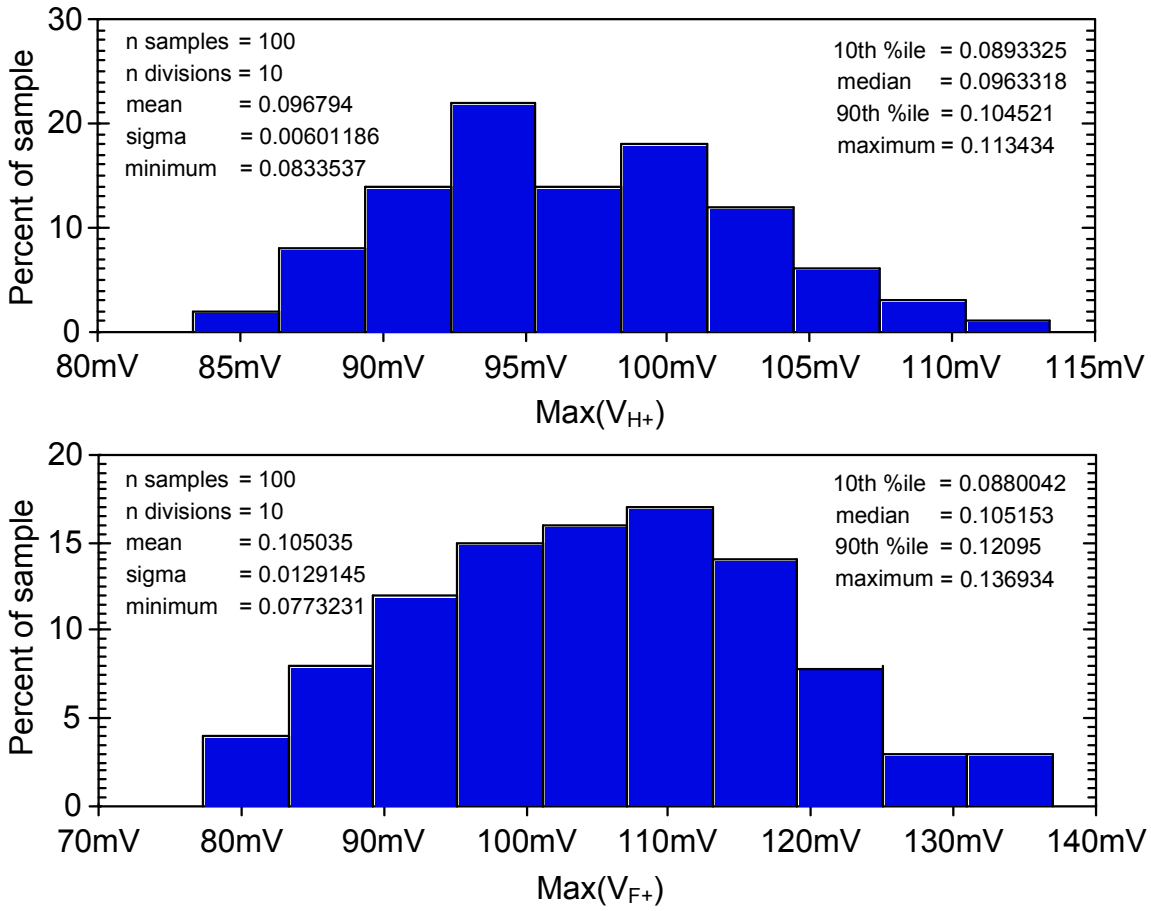


Figure 10. Monte-Carlo simulation with hundred runs to show the effect of threshold voltages variation on the output waveforms for: (upper) V_{H+}, (lower) V_{F+}.

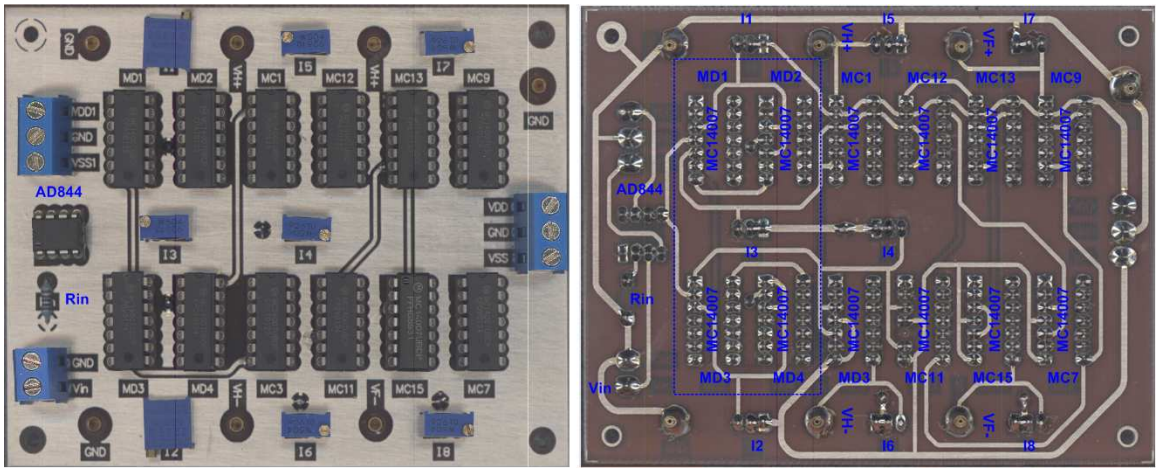
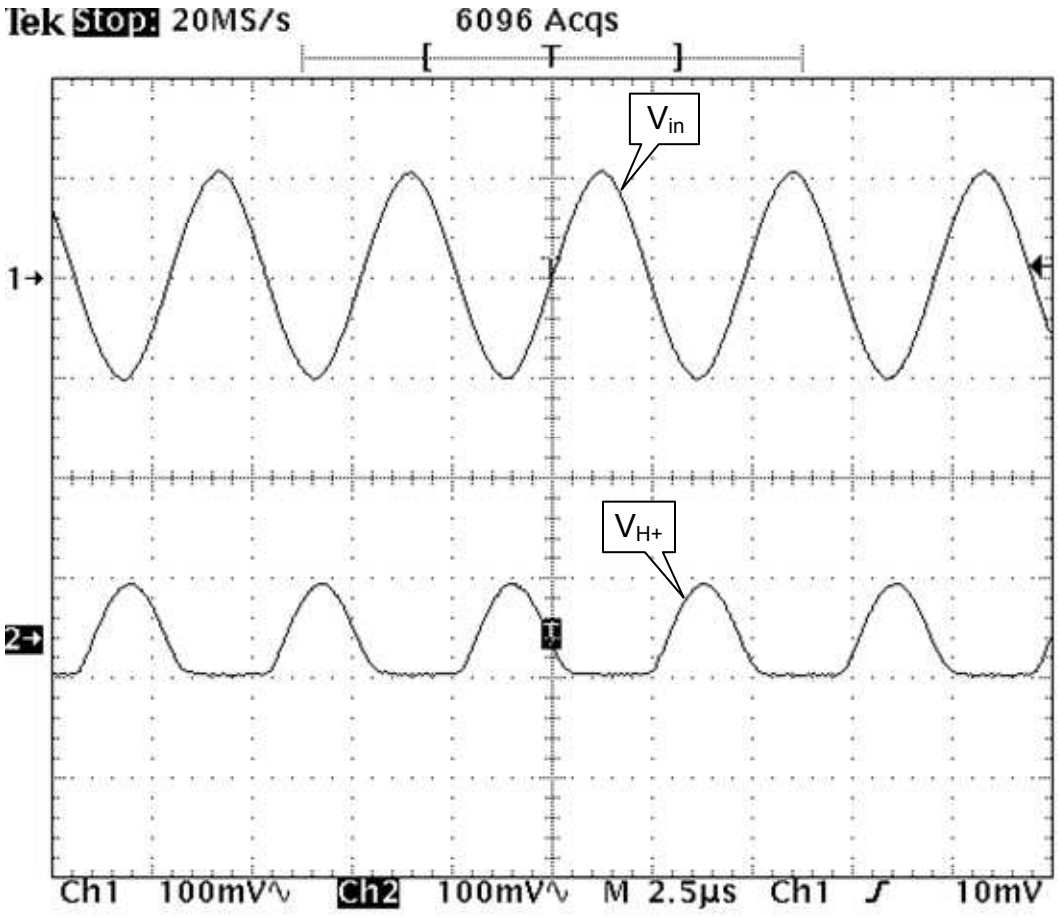
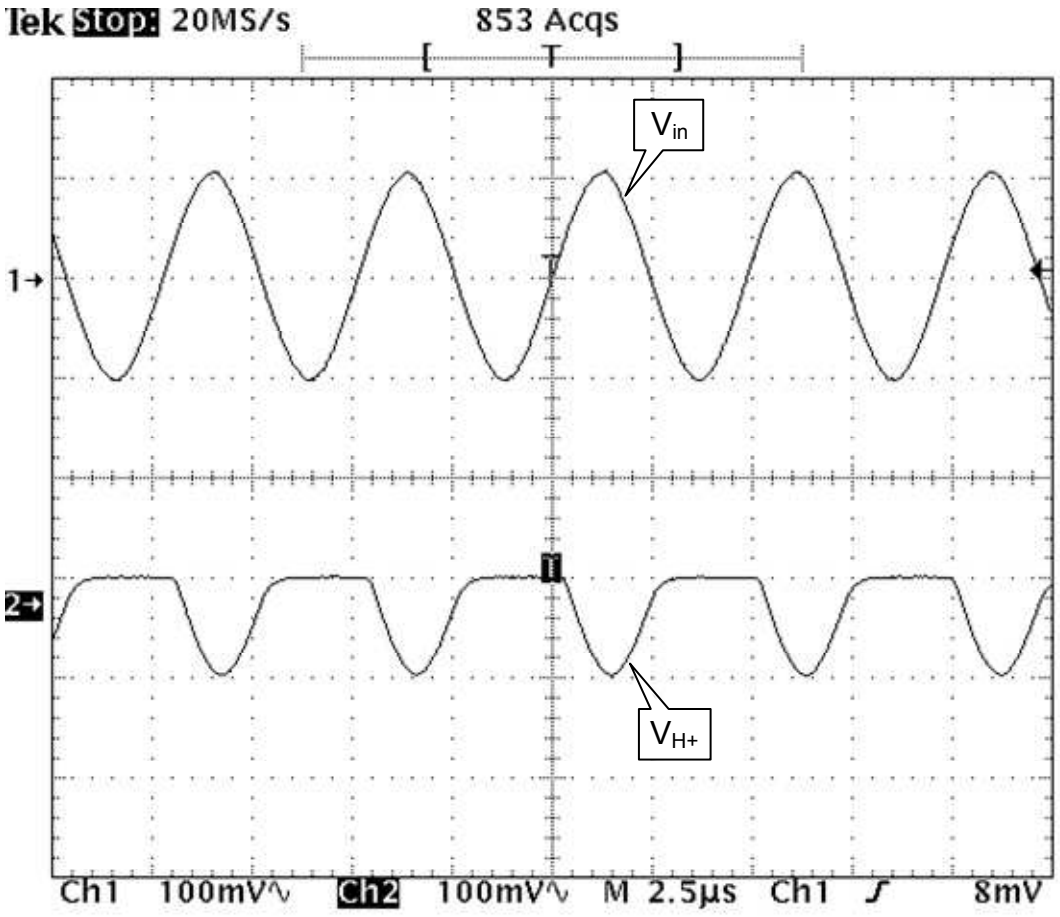


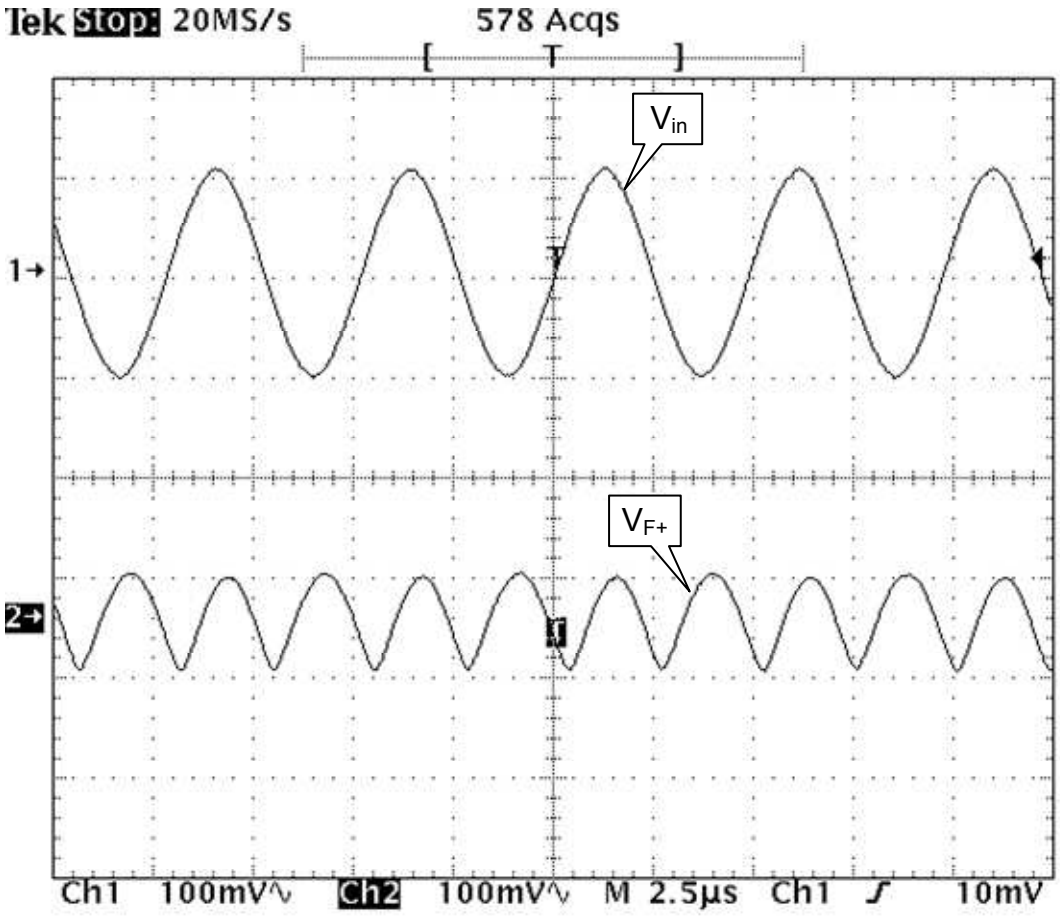
Figure 11. Measured prototype.



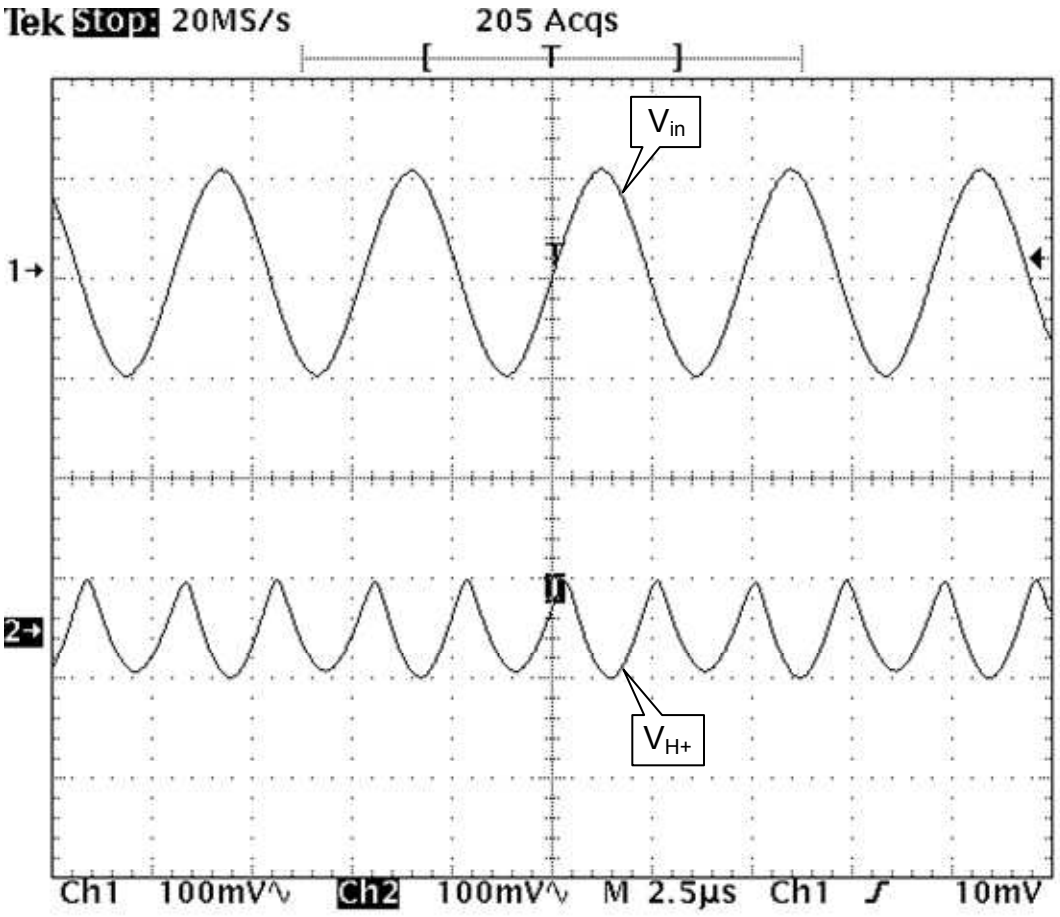
(a)



(b)



(c)



(d)

Figure 12. The experimental waveforms: (a) V_{in} and V_{H-}, (b) V_{in} and V_{H+}, (c) V_{in} and V_{F+}, (d) V_{in} and V_{F-}.

Table 1. Simulated specifications of CCII used.

Parameter	Value
Technology	0.18 μm
Power supply	± 1.2 V
Quiescent current	20 μA
Input voltage range	-200 to 200 mV
Voltage error range	5.7 mV
Input current range	-100 to 100 μA
Current error range	7.767 μA
Bandwidth (-3dB) Voltage follower (V_x/V_y) Current follower (I_z/I_x)	 800 MHz 1.1 GHz
Slew Rate (SR)	0.259 V/ns
R_X, L_X	1.1 kΩ, 38 nH
R_Y, C_Y	500 GΩ, 0.044 fF
R_Z, C_Z	152.67 kΩ, 0.48 fF

Table 2. The aspect ratios (W/L) and bias currents of the transistors in Figs. 1 and 2.

MOS Transistors	**W/L (μm/μm)**
M_1, M_2, M_5, M_6, MC_3, MC_4, MC_6, MC_7, MC_8, MC_{11}, MC_{15}, MC_{16} MD_3, MD_4	3/0.3
M_3, M_4, M_7, M_8, MC_1, MC_2, MC_5, MC_9, MC_{10}, MC_{12}, MC_{13}, MC_{14}	8/0.3
MD_1, MD_2	1/0.3
MR_1, MR_2	0.8/0.3
MR_3, MR_4	0.32/0.3
MR_5, MR_6, MR_7, MR_8	0.27/0.3
MR_3-MR_{10}	0.28/0.3
I_{C1}, I_{C2}	20 μA
I_3, I_4	100 μA

Table 3. Comparison of proposed circuit with some previous works.

Parameter	Proposed circuit	Gift [16] (Fig. 2)	Maheshwari [18]	Riewruja et al. [33]	Kumngern et al. [34]	Chaoui [36]	Monpapassorn et al. [37]
Component	47 MOSs, 9 current sources	12 BJTs, 1 CFA, 4 current sources 2 resistors	21 BJTs 2 MOSs 2 resistors 1 current source	7 MOSs, 3 current sources	31 MOSs, 7 current sources	14 MOSs,	44 MOSs, 4 current sources
Rectify type	half-wave and full-wave	full-wave	full-wave	full-wave	half-wave	half-wave	half-wave
Output type	positive and negative	positive	positive	positive	positive and negative	negative	positive and negative
Supply voltage	±1.2 V	± 15V	±2.5 V	+1.5V	±1.2 V	±2.5 V	±1.2 V
Operation frequency	250 MHz (half-wave) 100 MHz (full-wave)	1 MHz	100 kHz	100MHz	300 MHz	5 MHz	100 MHz
Power consumption	5.2 mW	-	-	-	1.76 mW	1.9 mW	1.8 mW
Input dynamic range	±250 mV	-	±30 mV	±80µA	±250 mV	±1 V	±300 mV
Temperature stability	good	good	fair	good	good	-	good
Zero-crossing	good	good	good	good	good	fair	good
Suitable for IC	yes	no	no	yes	yes	yes	yes