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Studies were conducted on fabrication processes of MOS capacitors and MOS transistors, in order to obtain the know-how which could be used in fabricating MOS IC's. Si wafers (p-type), polished on one side, and with specific resistivity of $18-24~\Omega$ -cm, were used as substrates for making both MOS capacitors and transistors on the same chips. Best conditions were determined on how to i) fabricate MOS capacitors with good gate-oxide quality ii) make good diffusion layers. MOS transistors fabricated with different geometries were characterized electrically.

The research results showed that in order to get good MOS capacitors, great care must be taken in the fabrication process which had to be done on a continuous fashion from start to finish. Another factor which improved yield considerably was the abrupt cooling of samples after gate-oxidation. Drains and sources on MOS transistors were made by phosphorus-diffusion. Junction depth of diffused layers were time-dependent.

Electrical characteristics of MOS transistors varied according to their structures, with threshold voltage in the neighborhood of -1.81 V. The yield of these transistors was found to be about 82% (based on 33 transistors).