C216820 : MAJOR COMPUTER SCIENCE
KEY WORD : VLSI DESIGN / QUEUING DATA MANAGEMENT
SUMET ANGKASIRIKUL : VLSI DESIGN FOR QUEUE MANAGEMENT ,
THESIS ADVISOR : ASST. PROF. SUYUT SATAYAPRAKORB, THESIS CO-ADVISOR :
ASST.PROF.BOONCHAI SOWANWANICHAKUL 153 pp. ISBN 974-584-401-2

The objectives of this project are to study the principle of the integrated circuit (IC) and the integrated circuit theory, design the electronic circuit for building the queuing data structure management algorithm instead of using software process, implement the algorithm on application specific IC and test the algorithm on the computer simulation process.

The research designs the electronic circuit for managing the queuing data. The experimental test is done by using the ORCAD program to build the logic simulation model. The circuit is implemented into 3 categories, gate array, semi-custom and full custom. First, the gate array is designed by using XILINX field programable gate array. Second, The semi-custom IC is designed by using the Harris SC 3000 standard cell and lastly, the full-custom IC is designed by using CIRCAD II software under the CMOS 1.5 micron double metal technology. The simulations of the operations for each category under the same conditions are tested. The semi-custom IC which is used Harris SC 3000 standard cell is sent to be fabricated in Australia. The research is also applied the algorithm to use as printer spooler.

The results from the research are as expected. The comparisons of the complexity of the design, time needed for designing and prototype building, cost of building the prototype and concluding remarks are also commented in the paper.