

Auttaphud Seubnaung 2009: Prototype of Vector Symbol Decoder for a (3, 2, 2) Convolutional Code with Two Alternative Choices on an FPGA Board. Master of Engineering (Electrical Engineering), Major Field: Electrical Engineering, Department of Electrical Engineering. Thesis Advisor: Assistant Professor Usana Tuntoolavest, Ph.D. 140 pages.

Vector symbol decoding (VSD) for convolutional codes that use large nonbinary symbols can correct burst errors well. The benefit of using large nonbinary symbols is that correcting each error symbol means correcting all error bits in that symbol. This makes the decoding technique suitable for channels with low quality at times such as wireless channels without the need to use interleaving as in the case of binary codes.

The purpose of this research was to design and implement the prototype of channel decoder called Vector symbol decoding that can decode a (3, 2, 2) convolutional code that uses 32-bit symbols with 2 alternative choices. The implementation was done on an FPGA board to show that the theory of Vector symbol decoding for convolutional codes can be applied to hardware. The development of this decoder was done in 3 steps: Decode with one syndrome, the Correct with second choice and the Correct with null combination. The result shows that the prototype can work exactly as designed. It can correct all error patterns indicated in the theory of VSD.

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Thesis Advisor's signature

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