Abstract

This research applies the DMAIC methodology to electronics devices assembly process at the mounting machine. The studied factory mainly produces discrete semiconductor equipments. The aim of this research is to reduce cost and increase Yield of TO-3P(N) Package. The data from 2008B period (October 2007 to March 2008) is used to create the Pareto chart and the result shows that the Mounting process has the highest defect rate at 0.54%. In the define phase, we identify the void under the pallet (DVDS(0)+ DVDS(1)) as our main problem with 0.13% defect rate. This void prevents the heat to transfer quickly enough and results in the pallet burn. In the measure phase, we apply flow chart diagram to detect the value-added processes which are solder preform and die bonding processes. In the analyze phase, we perform a hypothesis testing to figure out which key process input variables (KPIVs) actually contribute to key process output variables (KPOVs). In the improve phase, we use the obtained KPIV to perform a design of experiment (DOE) to achieve a mathematical model equation which can help alleviate the defects from DVDS(0)+ DVDS(1) problem. The defect rate is lower to 0.0741% which reduces from the initial target of 0.08% by 0.0059% by setting die bond type to ball baring, scrub time to 0.5 second and scrub speed to 10 m/s. In the control phase, we monitor the results from October 2008 to February 2009 and the defect rate varies between 0.0738% and 0.0767%. These results confirm that we can control the DVDS(0)+ DVDS(1) problem and accomplish the defect target rate.